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Effect of Crystallinity and Morphology on the Electrical Properties of Y_2O_3 Thin Films Prepared by Pulsed Laser Deposition for MOSFET

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ABSTRACT

The paper focuses on the effect of the crystalline structure and surface morphology on the electrical properties of Yttrium oxide (Y_2O_3) thin films. The impact on the change in substrate temperature from ambient to 650°C in low oxygen pressure (0.0034mbar) was realized by change in crystallinity and morphology. The XRD result shows the preferred orientation along the (400) plane. The effect of substrate temperature on the crystal structure has been studied and the same impact has been observed in film morphology using scanning electron microscopy. The higher dielectric constant of 21 was observed at room temperature deposition. The transfer characteristic of Y_2O_3 gate dielectric based Si-MOSFET gives current ratio I_{ON}/I_{OFF} of 10^7 and threshold voltage of -2.8V. Furthermore, from output characteristics, the obtained I_{dss} is 0.415 mA. The high I_{ON}/I_{OFF}, makes it suitable for digital gates, optical electronics, SMPS and portable electronic applications.

Keywords: Yttrium oxide, Pulsed Laser Deposition, Crystalline Structure, Field Effect Transistor, High-K Gate Dielectric.

1. INTRODUCTION

Silicon dioxide (SiO_2), a prominent dielectric material in semiconductor devices exhibits a dielectric constant of only 3.5 [1- 3]. It has been reported that rare earth oxide films such as Eu_2O_3, Y_2O_3 etc., are found to exhibit excellent dielectric properties with reproducible results [4]. These high-k dielectric materials unlike SiO_2 could help in tuning the thickness of gate dielectric to prevent tunnelling, resulting in reduced leakage current [5-7] Among these, Y_2O_3 being the most available rare earth oxide deposited on Si substrate have gained much attention in recent years [4,6]. The significant properties of Y_2O_3 include its thermal & chemical stability, low leakage current, wide band gap (5eV) and relatively high dielectric constant (14 ~ 18) with respect to SiO_2 [8-11].

Several deposition techniques have been reported to fabricate Y_2O_3 thin films, which includes sputtering [12], molecular beam epitaxy [13], electron beam deposition [14], chemical vapour deposition [15] and pulsed laser deposition (PLD). Among these PLD is reported to have excellent stoichiometry transfer with low cost and high deposition rate [16-18]. It has been reported that the texture of film varies with the change in oxygen pressure and/or temperature of the substrate [19-20]. It has to be noted that when the substrate temperature is higher, the atoms get enough time to arrange in the low energy stable structure due to the increase in mobility of adatoms [21]. This is again supported by the low oxygen pressure, where the

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collision between the ablated species and oxygen atom is less probable and so the ablated species get enough time to form the low energy structure [21].

Several oxide materials deposited by PLD at different substrate temperatures and oxygen partial pressure have been tested for its properties [22, 23]. For TiO_2 it has been reported that the films deposited below $1X10^{-4}$ mbar oxygen pressure exhibited an amorphous nature, whereas for the pressure between $1X10^{-4}$ to $1X10^{-2}$ mbar these films were of crystalline nature [22-24]. For CoO film two oxidation processes have been reported to take place during the film growth in PLD. Direct oxidation takes place during film deposition for O_2 pressure higher than $1X10^{-3}$ mbar. This was followed by surface oxidation which occurred after the deposition. In order to avoid the formation of CO_3O_4 and protect the film a Pt over layer has been used [23]. Therefore from the previous literature we observe that the oxygen partial pressure is material dependant and it plays a significant role is determining the properties of the deposited film.

Y_2O_3 thin films deposited by PLD Shaoqiang Zhang *et al*. [25] have observed the formation of amorphous film with the increase in oxygen pressure from (0.0001mbar to 0.1 mbar) at a fixed temperature of 650°C. Similar observation has been made by Mishra *et al*. [21], where they have reported a decrease in crystalline size of pulsed laser deposited Y_2O_3 thin films with the increase in oxygen pressure from 0.00002 mbar to 0.02 mbar. Also they have observed an increase in crystallinity with the increase in substrate temperature.

It is clear from the above reports that Y_2O_3 can be deposited both in crystalline and amorphous form by tuning the partial pressure and substrate temperature. At the same time as discussed above in order to attain stable low energy structure we have to maintain high temperature and low pressure. Based on the previous reports in the present work, we have focused on the deposition of Y_2O_3 at a wide range of substrate temperature from room temperature to 650°C and low oxygen partial pressure of 0.0034mbar, which is within the range reported in previous literature [21,24]. We have reported the effect of these parameters on the structure, morphology and dielectric properties of the Pulsed Laser Deposited Y_2O_3 films [26-28]. Further the previous reports were based on the crystallinity of the deposited films, here we have also focussed on the difference in morphology of the film which had an impact on its electrical properties. The film deposited with low resistivity and high dielectric constant has been used in the fabrication of FET and the device characteristics were studied.

2. EXPERIMENTAL

Yttrium Oxide (Y_2O_3) source material with 99.9% purity has been used for the depositions. The high power pulsed laser (Nd-YAG laser) is focused to Y_2O_3 pellet target which is placed inside the vacuum chamber. The PLD system consists of 8 target rotating holder in one side of the chamber and on the other side it consists of substrate holder with a controlled heater. Various quartz windows are mounted to check the position of target and substrate. The laser beam passed through quartz window and hit the target. The chamber was evacuated by rotary and turbo pumps and then oxygen was supplied from the cylinder to maintain the required oxygen partial pressure.

N-Type Silicon substrate with (110) orientation, resistivity of 0.001 ohms-cm and dimension of 1cm X 1cm been used for the deposition of Y_2O_3 [28]. The deposition has been carried out with a fixed and low oxygen pressure (0.0034 mbar) and different substrate temperatures. The temperature was noted by setting temperature of substrate heater, which is in built system controlled by PID controller. (Room temperature, 250°C, 450°C and 650°C).

Various characterization techniques have been employed to study the properties of the deposited Y_2O_3 films. The characterization techniques include X-ray diffraction (XRD-

SHIMADZU model XRD-6000) to study the crystalline structure, Scanning Electron Microscope (SEM-JOEL model JSM-6390) for the study of film morphology. The surface continuity of the film has been studied using AFM (Multiview 2000 – Nanonics). The dielectric constant has been measured using Solatron 1260 impedance analyser. The thickness of the film was measured by using dekta-kXT stylus profilometer from Bruker. The output characterization of the fabricated FET was measured using National Instrument PXI-4100 I-V source meter.

3. RESULTS AND DISCUSSION

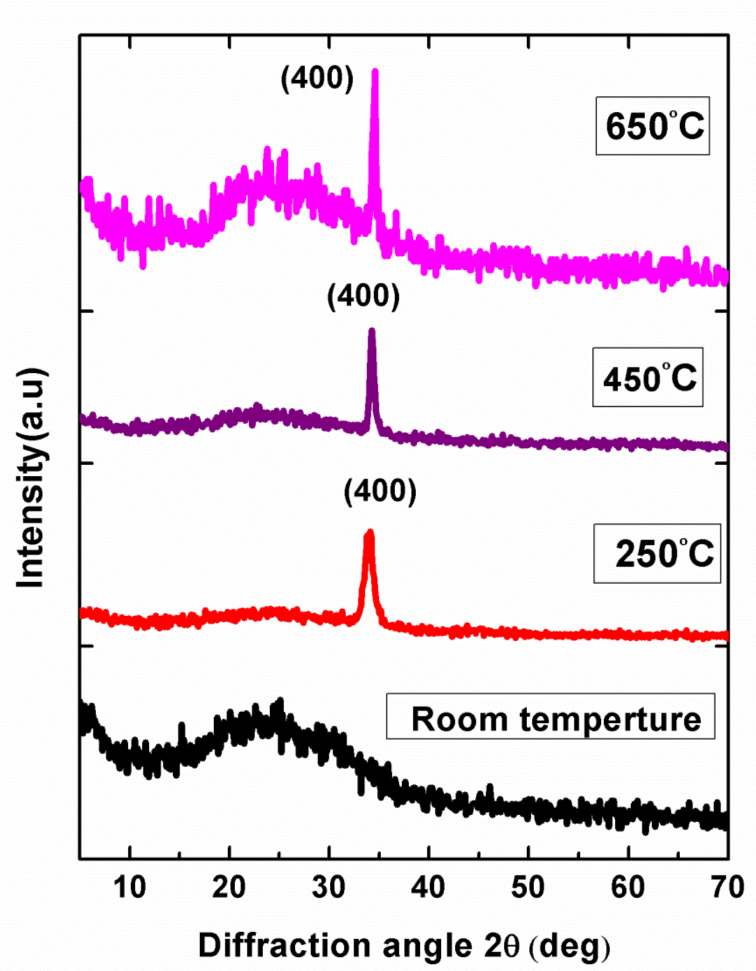

Figure 1. XRD pattern of Y_2O_3 deposited thin films at various deposition temperatures in PLD chamber.

The XRD patterns of Y_2O_3 films deposited with different substrate temperatures (Ts) as Room temperature, 250°C, 450°C & 650°C are shown in Figure 1. The deposited film at room temperature shows a broad diffraction pattern without any preferential orientation, which indicates the amorphous or nano-crystalline nature of the films.

With the increase in substrate temperature from 250°C, 450°C and 650°C, the films exhibited a diffraction peak with preferential orientation along the (400) plane according to (ICDD file no. 44-0399) [29], the crystal structure has been identified to be monoclinic, which is in agreement with the reported results [29]. These results are in agreement with the previous reports by Shaoqiang Zhang etal. [24]. They have reported a preferential orientation along (222) plane with a relatively high O_2 partial pressure maintained at 0.01mbar. Also they have reported the emergence of (400) peak with a further increase in oxygen partial pressure from 0.05mbar to 0.1mbar. In the present work, we have attained similar orientation along (400) plane under low oxygen partial pressure condition of 0.0034mbar, which ensures the formation of stable structure of Y_2O_3 at low pressure.

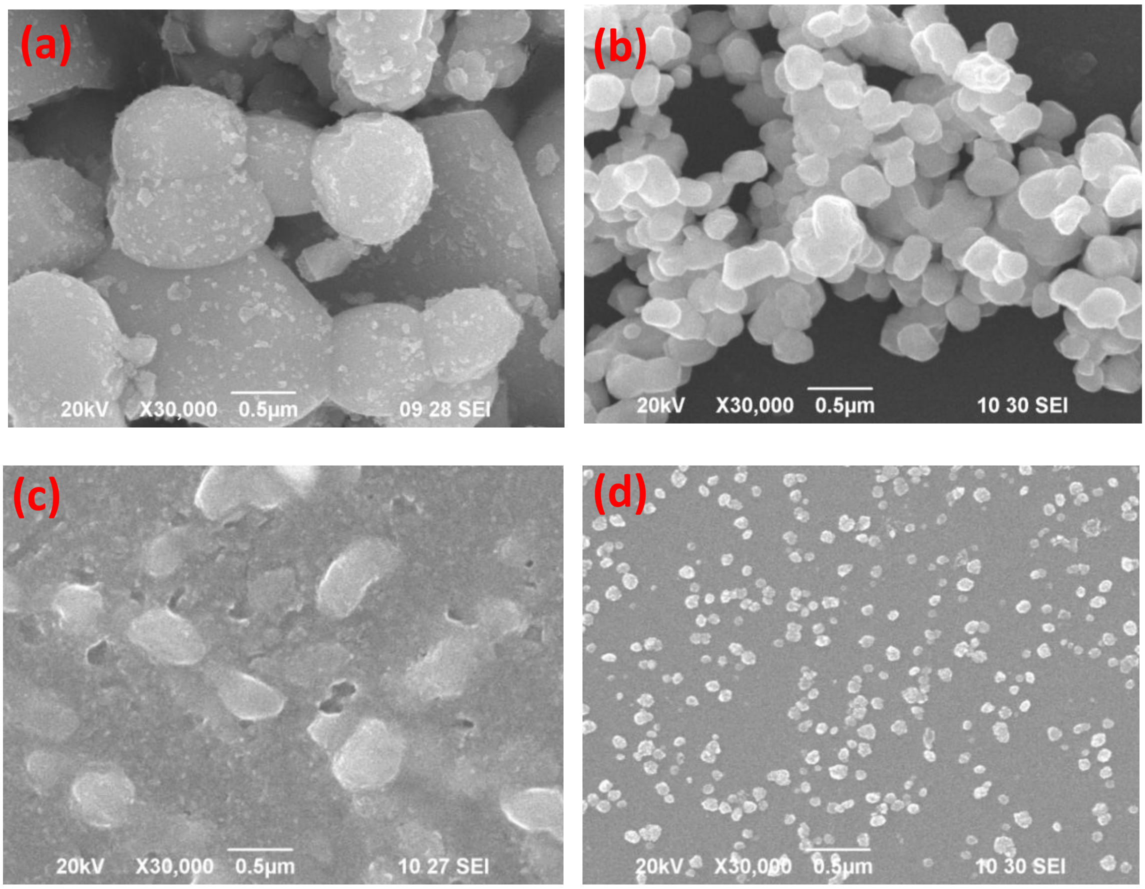

Figure 2. SEM image of Y_2O_3 at various deposition temperature (a) Room temperature (b) 250°C (c) 450°C and (d) 650°C.

The SEM image obtained for the films deposited at various substrate temperatures is shown in Figure 2. It is clear from the image that Y_2O_3 thin film deposited at room temperature showed slightly porous nature with loosely packed particles, which could have been the reason for the broad XRD pattern as well. With the increase in substrate temperature it is evident that the particles started to coalesce and merge with each other, as evident in Figure 2 C, where two particles are connected to each other. With further increase in temperature to 450°C the particles have further decreased in size and some widely distributed nucleation sites are evident. For the substrate-temperature of 650°C many new crystallites with nano size are evident, which would be the reason for broad peak in XRD of this film, but the particles are still determined to have a preferential growth along the (400) plane

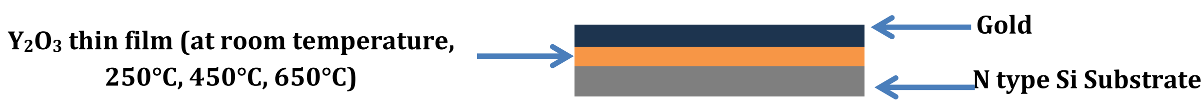

Figure 3. Capacitor structure with Y_2O_3 thin film.

Using solatron 1260, the capacitance study was carried out for the Metal Oxide Semiconductor (MOS) structure of Y_2O_3 films at various substrate temperatures which is shown in Figure 3. The capacitance(C) equals 312nf, 267nf, 264nf and 265nf were obtained for various substrate temperatures of room temperature, 250°C, 450°C and 650°C respectively at 50HZ to 1MHZ of applied frequency. The dielectric constant (k) of the films was calculated from the parallel plate capacitance equation 1 which is shown below [25][30]. By rearranging equation 1, the dielectric constant k has been obtained from the equation 2 [25]

Where ε is the constant dielectric permittivity at vacuum, area (A) of film was 1cm X 1cm and the thickness (d) of the deposited Y_2O_3 film was 61 nm. Thickness of the Y_2O_3 thin film was measured as 61nm by using stylus profilometer.

Where ε is the constant dielectric permittivity at vacuum, area (A) of film was 1cm X 1cm and the thickness (d) of the gate dielectric was measured by stylus profilometer as 61nm. The dielectric constant for various substrate temperature of the film was calculated and tabulated in Table 1 below.

$$C = \frac{k.\varepsilon.A}{d} \quad (1)$$

$$k = \frac{c.d}{\varepsilon.A} \quad (2)$$

Table1 Dielectric constant values of Y_2O_3 thin film at various temperatures

Substrate Temperature	Dielectric Constant (k)
Room temperature	21
250°C	19
450 °C	17
650°C	18

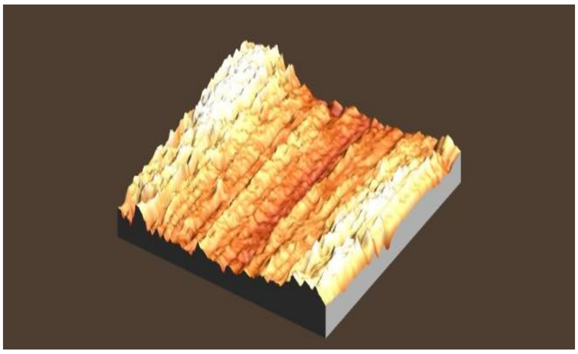

Figure 4. AFM image of pulsed laser deposited Y_2O_3 film at room temperature.

From these results, it is observed that the dielectric constant of Y_2O_3 film gradually decreases with the increase in substrate temperature and also there is a sudden increase in the dielectric constant for the film deposited at substrate temperature of 650°C which is in accordance with the results observed in XRD and SEM of various substrate temperature deposited films. Among these high orders dielectric constant was observed at room temperature. With these XRD, SEM and electrical studies; Y_2O_3 film deposited at room temperature can be used preferably for field effect transistor as gate dielectric layer due to its high value of dielectric constant than the other deposited films. In order to further ensure the continuity of the film, AFM images were taken for the room temperature deposited film as shown in figure 4, before it could be used in the fabrication of FET.

4. MOSFET FABRICATION AND ELECTRICAL CHARACTERISTICS

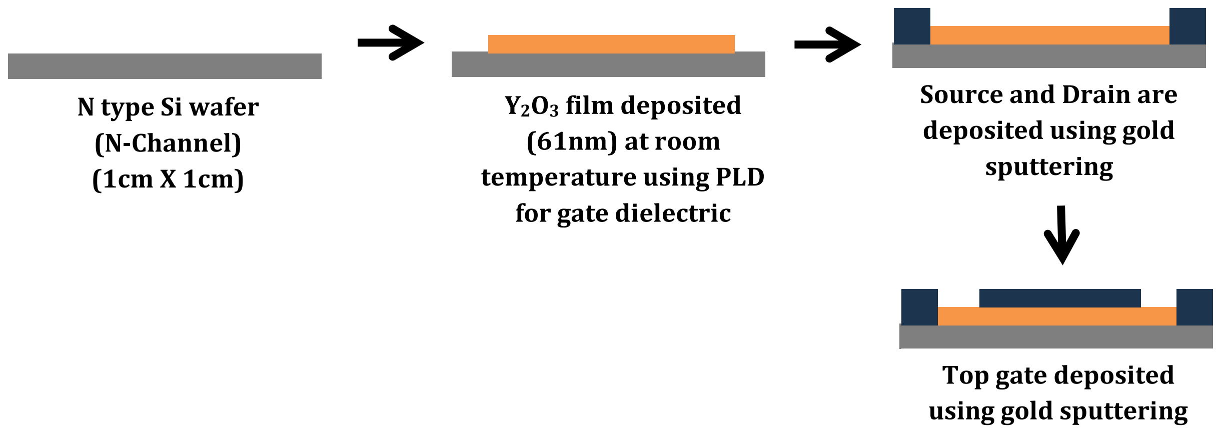

Figure 5. Fabrication steps involved for the proposed Y_2O_3 gate dielectric Si-MOSFET.

The step by step fabrication process of MOSFET is shown in Figure 5. The device fabrication starts up by taking a well cleaned and processed N-type Silicon (Si) wafer chosen as channel and also a base layer of FET.

The Y_2O_3 film was deposited as the gate dielectric 61nm at room temperature over silicon by using PLD. This deposition was carried out with fixed O_2 pressure (0.0034mbar) and pulse laser repetition rate at 10Hz. Using the prepared mask the drain, source & gate electrode are deposited using gold (Au) by DC sputtering. The electrical characterization of the film has been carried out using National Instruments PXI 4110.

The output I-V characteristics of the Y_2O_3 based gate dielectric of MOSFET is shown in Figure 6. I-V characteristic were analysed by varying the drain source voltage (V_{DS}) between 0 to 6 volts with constant increment of -2 volts of gate source voltages (V_{GS}) between 0V to -6V. The output current I_D is obtained in the range of milliamps.

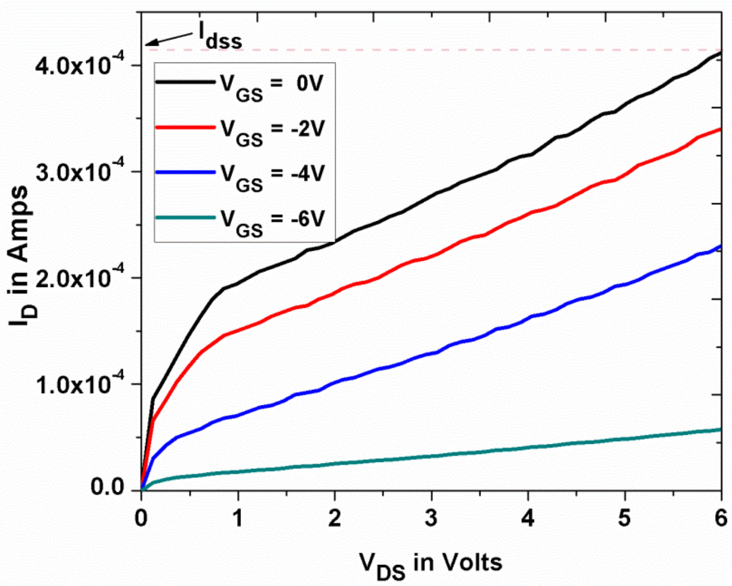

Figure 6. Output characteristics of n-channel MOSFET with Y_2O_3 used as a gate dielectric.

This output response shows n-channel FET with ohmic and saturation region in the characteristics curve. The output current drain current (I_D) is reduced with the increase in the negative gate voltage, which is observed in the principle of depletion FET. These results clearly show the output current is controlled by input gate voltage (V_G). From Figure 6 we observed Idss (drain current at V_{GS}=0V) as 0.415 mA. This Idss is the maximum drain current which reaches without the restricted breakdown region. It is also referred as the drain current for zero biasing voltage.

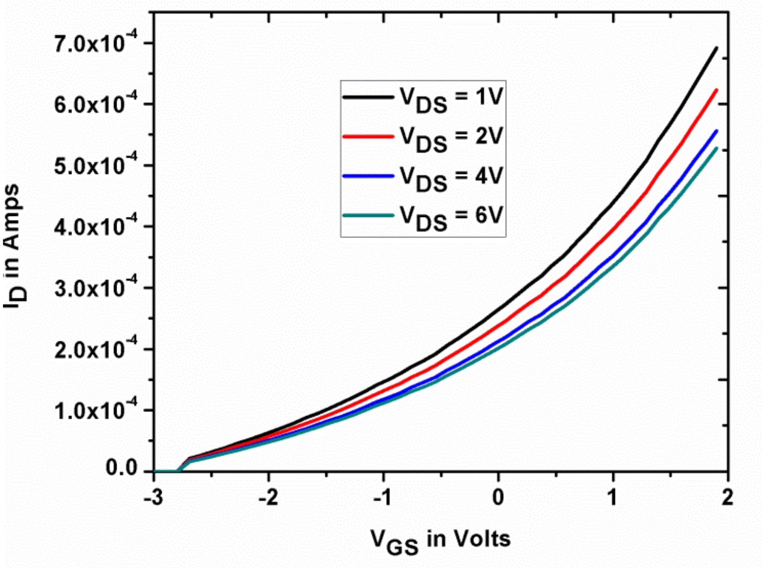

Figure 7. Transfer characteristics of n-channel MOSFET with Y_2O_3 used as a gate dielectric.

Transfer characteristics of Y_2O_3 thin film transistor is shown in Figure 7, the obtained output drain current for the applied input by gate voltage (V_{GS}) ranging between -3 to 2V at different constant voltages V_{DS} (1V, 2V, 4V and 6V). The result clearly shows output drain current gradually increases with the increase in gate voltage as per the depletion N-channel MOSFET principle with control of applied V_{DS}.

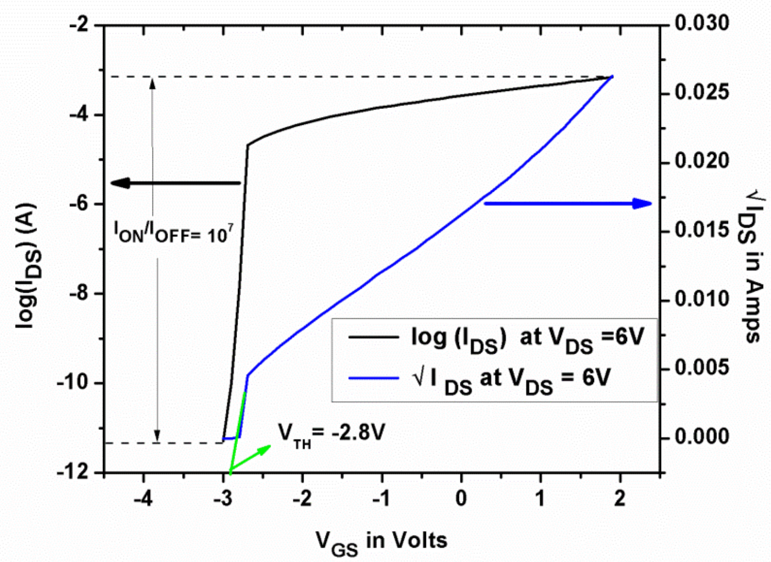

Figure 8. Logarithmic and square root of output drain current Vs gate voltage at V_{DS}=6v.

The various electrical parameters like Idss, threshold voltage and I_{ON}/I_{OFF} calculations analysed for the V_{DS} at 6V is shown in Figure 8. The threshold voltage -2.8 V was attained from the extrapolation of the square root of drain current (I_D) to the gate voltage (V_{GS}) [32] and I_{ON}/I_{OFF} ratio is obtained from the logarithmic value of drain current to gate voltage as 10^7 [31]. This value has been reported as 10^6 Liu A *et al.*[32] and Song K *et al.* [33]. The obtained results show that less leakage current was achieved in the fabricated MOSFET.

5. CONCLUSION

In this paper Y_2O_3 thin films were deposited at different substrate temperatures using pulsed laser deposition and their characterization studies have been carried out. These studies show that the Y_2O_3 thin film exhibits amorphous nature when there is no substrate temperature. But it exhibits crystalline peak when the temperature is applied from 250°C to 650°C and also it observed that at 650°C film exhibited a diffraction peak resembling the room temperature deposited film but with the preferential orientation maintained along (400) plane. In I-V characterization of films, the high resistance effect was observed at room temperature deposited film with a high dielectric constant of 21. The fabrication of FET has been carried out with N-Channel silicon with Y_2O_3 film (room temperature deposited) as a gate dielectric material of FET. Idss of 0.415 mA, threshold voltage (V_{TH}) of -2.8V and I_{ON}/I_{OFF} ratio of 10^7 were obtained for fabricated device.

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