A Survey on Emerging Technologies and Architectures of Low Power Preamplifiers for Biomedical Applications

Sanna Mairaj, Suhaib Ahmed* and Vipan Kakkar

Department of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, India.

ABSTRACT

Unlike other commercial devices, developing implantable microsystems for biomedical applications requires critical analyses in terms of specifications, technologies, and design techniques because of the devices' safety and efficacy. As the industry of medical implantable devices develops, lowering the power consumption as much as possible is essential in improving the service time of the battery, which cannot be replaced frequently. Hence, low power design has become the main concern for battery-powered implants. Biosignals such as EEG and ECG are weak signals, typically ranging from 0.5µV to 5mV with high source impedance and superimposed high level interference and noise. Hence, there is a need of a pre-amplification stage in the analog front end of a biomedical acquisition system so that these biosignals can be amplified for measurement and testing purposes, without degrading the signal-to-noise ratio. The purpose is to provide amplification that is selective to physiological signal, reject noise, and other sources of interference. In this paper, an in-depth study of various low power pre-amplifiers proposed for different biomedical applications were made, along with performance comparison in terms of various amplification-related specifications such as gain, bandwidth, signal-to-noise ratio, CMRR, and slew rate among other specifications.

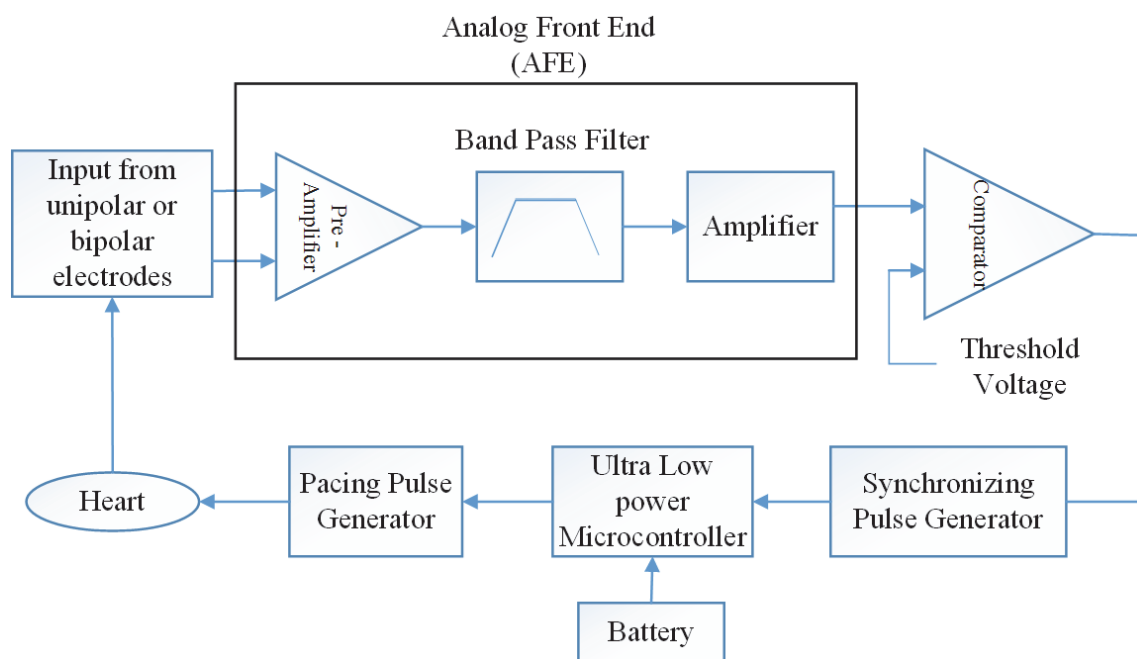**Keywords:** Biomedical Implants, Preamplifier, Low Power Electronics, Analog Front End.

1. INTRODUCTION

The term implant represents a medical device that acts as a part of the whole biological system or can be used to provide support to a damaged biological structure [1,2]. Currently, biomedical implants are used for various applications including cardiac pacemakers, defibrillators, and cardiovascular stents. The monitoring of biomedical signals provides us information about the vital health of the body and thus the data can be of prime importance to medical practitioners [3]. With the rapid development in microelectronics towards medical therapies and diagnostic aids, there is a need for lowering the power consumption in active implantable devices that are battery powered so that the device lifetime increases. One such example of active implantable devices in terms of its widespread application is the Cardiac Pacemaker [4]. A Cardiac Pacemaker is a device that uses electrical pulses to recover the normal heartbeat of a diseased heart. The major building blocks of the pacemaker, shown in Figure 1, are an analog front end (AFE) circuit, a microcontroller with ultra-low power consumption, a battery, and an output circuit that stimulates the heart.

The AFE comprises of a preamplifier, low-pass filter, level shifter and synchronizing circuit [5]. The cardiac signal is given to a low noise preamplifier for amplification purposes and is then filtered. This filtered signal is then given to a comparator that produces a pulse, which depends upon the threshold voltage level. The output stage of a pacemaker is called a charge pump that uses a pulse generator to stimulate the activity of the heart. Thus, the preamplifier is a critical block that is used for the detection of small level signals especially for the biomedical applications [3].

Figure 1. Block diagram of a typical implantable cardiac pacemaker system.

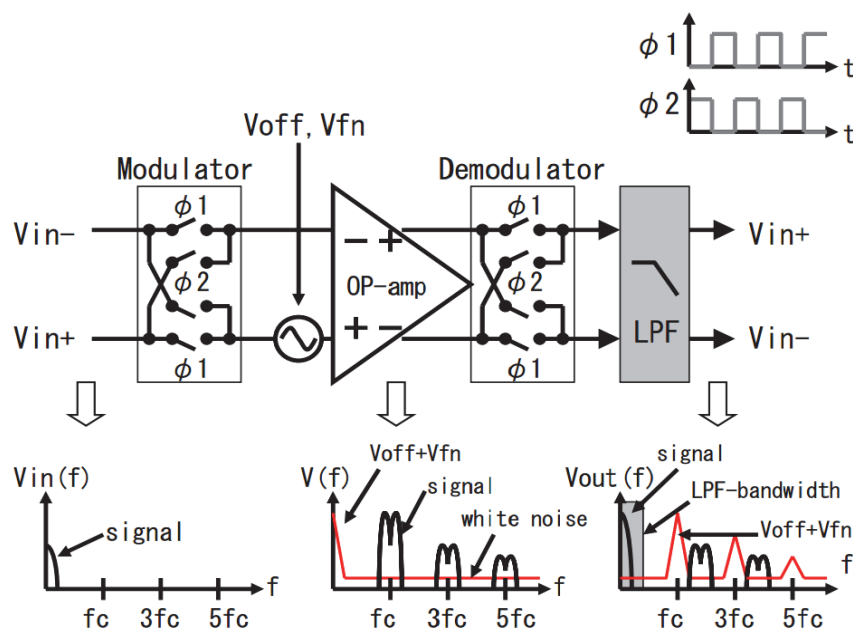## 2. NEED FOR PRE-AMPLIFICATION

Biosignals like EEG, ECG, EMG, and EOG are weak signals with input amplitude typically ranging from 0.5uV to 5mV [5,6] and are highly susceptible to noise and power line interference at 50Hz to 60Hz. Nowadays, there is a demand for a low noise, low power bio acquisition system so as to avoid bulky connectivity and reduce patients' mobility and discomfort [7]. A Preamplifier is one of the important components of the analog front end as it determines the SNR of the entire biomedical signal acquisition system and is required for reliable monitoring of the physiological signal [8]. The weak biosignal needs to be amplified so that it is compatible with devices like displays, recorders, A/D converters, etc., and for measurement and testing purposes [9]. This paper presents a comprehensive study of different preamplifier topologies along with their performance comparison in terms of the various amplification related specifications such as gain, power consumption, common mode rejection ratio (CMRR), and input referred noise among specifications.

3. LOW POWER PREAMPLIFIERS IN BIOMEDICAL APPLICATIONS

Much of the current research work is done on neural implantable devices, cochlear implants, etc. For neural applications, parameters such as low noise and low power are critical mainly because the $1/f$ or flicker noise is more predominant at low frequencies [5] and some other sources of noise such as from electrode tissue interface and EMG (generated by muscles) cause interference with the neural signal (ENG) of amplitude (10μV-500μV) and frequency (10Hz –

10kHz) [10]. The ENG signal has similar frequency band as that of the $1/f$ noise, and this in turn causes the degradation of SNR. Therefore, it becomes important that the input referred noise of the amplifier should be minimized so as to boost the SNR. Low power operation is also considered important in order to minimize the area and to increase the battery lifetime. The amplifier should dissipate less power so that there are less chances of damaging the surrounding tissue by the heat produced.

R. Reiger *et al.* proposed a BiCMOS Neural preamplifier [10], which has been compared with CMOS when operating in weak and strong inversion and it has been shown that the BiCMOS has the best $1/f$ noise performance. If the same performance is to be obtained from the CMOS process, then power consumption will be larger and there will be an increase in device size, but the main disadvantage of using BiCMOS is its greater cost. Previously, techniques such as chopper stabilization, shown in Figure 2, were used to eliminate the $1/f$ noise [11, 12].

Figure 2. Chopper stabilization technique [12].

The main disadvantage of this technique is that there is a need for an amplifier operating at higher frequencies with higher power consumption (not desirable for the implant). Therefore, improved techniques have been described, taking advantage of the high g_m/I_d ratio of devices operating in sub-threshold [13] so as to achieve low noise, low power, and best noise efficiency factor (NEF), which describes noise power trade-off. The MOSFET operating in the sub-threshold region has smaller current interference (trapping and detrapping of charge carriers) because carrier transfer mechanism is mainly due to the diffusion current that is directed away from the SiO_2 interface, hence flicker noise is smaller in the sub-threshold region. There are some stability concerns associated with these closed loop amplifiers that limit power noise efficiency. Hence, open loop amplifiers have been proposed, which have better noise performance but at the expense of linearity and reduced power supply rejection [14]. A pseudo-open loop energy efficient amplifier, shown in Figure 3, with programmable bandpass that retains high linearity and stability has been designed [15].
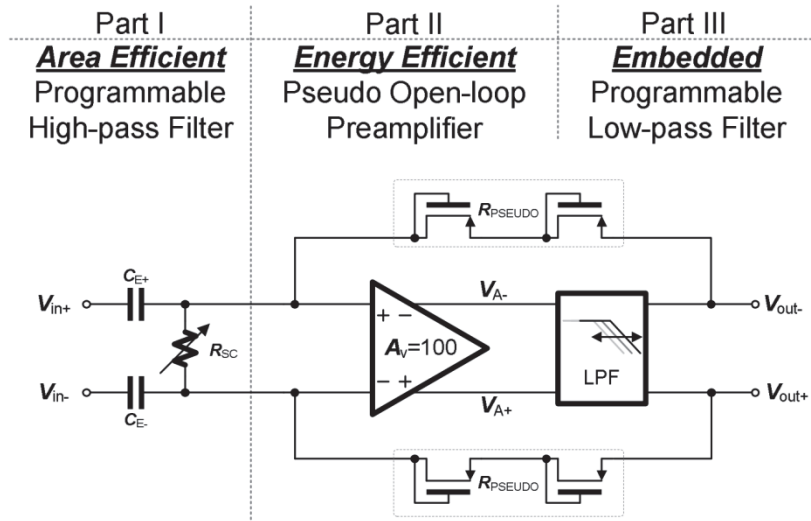
Figure 3. Pseudo-open loop energy efficient preamplifier [15].

The current trend in the design of neural amplifiers aims at amplifying the local field potentials (LFP) (<100Hz) instead of spikes (100Hz-7kHz). Spikes convey information about the extracellular neural activity of a single neuron unit. In contrast, LFPs convey information about the neural activity recorded from an ensemble of neurons. LFPs are useful in neuroprosthetic amplifiers and they also help in interpreting specific motor activities in understanding neurodegenerative pathologies. The main advantage of using LFPs is that it can be obtained directly from the raw signal. Also, it can be measured in the absence of spikes. The major constraints in LFP recording are power and area. In some applications, these spikes and LFPs are separated to be analyzed separately. Haddad *et al.* [16] proposed a true logarithmic amplifier (TLA), shown in Figure 4, that amplifies low amplitude spikes with a suitable gain (64.6 dB) in order to avoid the separation of the LFPs and spikes, while consuming less power (around 11μW). Dwivedi *et al.* presented a Single Ended OTA [17] with a DC shifting technique with ultra-low power consumption for LFP recording applications. It exhibits a wide dynamic range of 68dB and consumes a chip area of less than 0.10mm^2 [17]. Presently, the reduction in technology from 180nm to 45nm has also been reported in the literature for neural amplifiers. With the use of current mode amplifiers [18] shown in Figure 5, there is substantial improvement in parameter values such as reduction in power consumption, supply voltage and noise at 45nm as compared to 180nm.
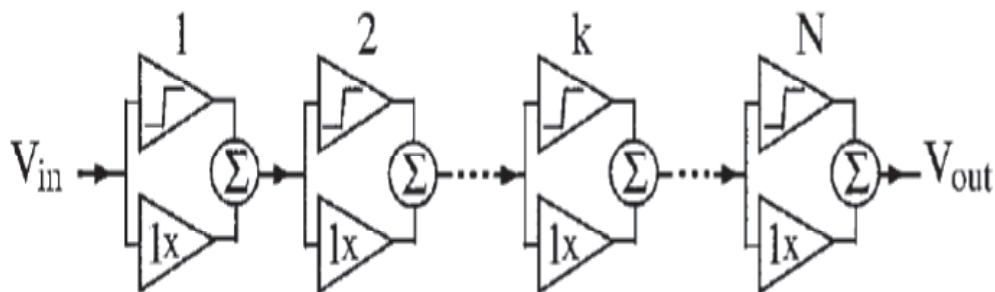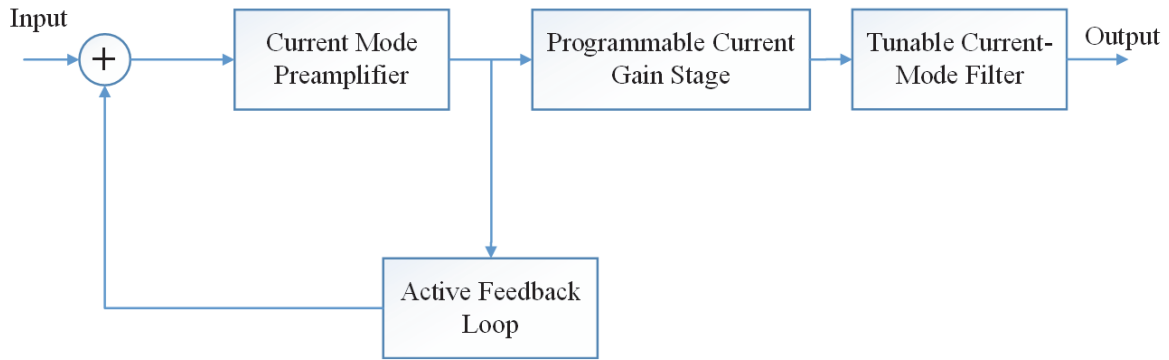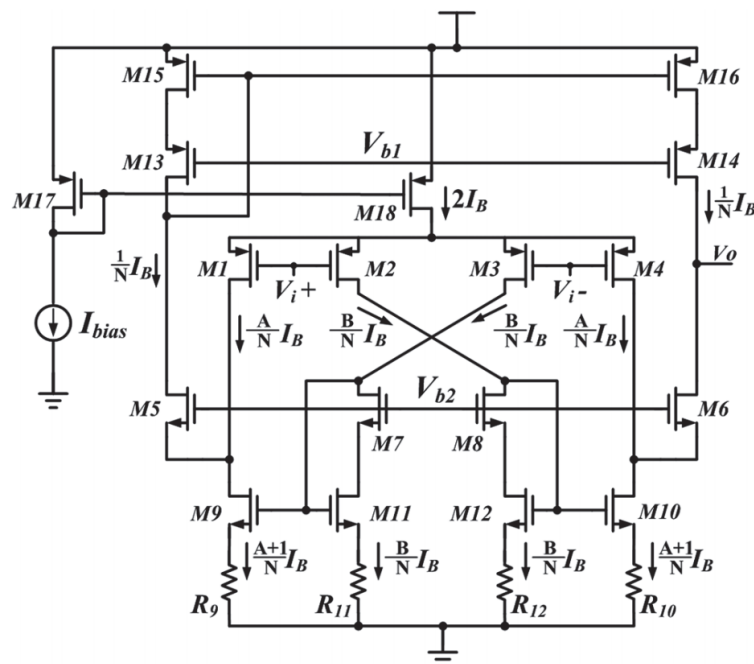

Figure 4. TLA structure with cascaded dual gain stages [16].

Figure 5. Current Mode preamplifier.

Recently, the analog front end for the treatment of epilepsy through the technique of deep brain stimulation (DBS) has been reported [19]. One of the important characteristics of the front end for this particular application is that it must be able to monitor the prolonged periods of epileptic seizures while consuming ultra-low power. Also, the noise power trade off must be maintained throughout the design. A folded cascode technique [19] that achieves a good noise-power tradeoff has also been used. To achieve low noise, the quiescent current that does not contribute to the overall transconductance of the amplifier is minimized. The drawback is reduced slew rate, which is not that important for this particular application. Qian *et al.* [19] proposed the technique of combining current splitting and output current scaling, as shown in Figure 6, in order to get low OTA noise. Another technique of folded cascode with current stealing [8] is used to achieve lower power consumption and has achieved one of the best NEF 2.60 (lowest so far).

Figure 6. Low Noise OTA with combined current scaling and splitting technique suitable for Epileptic seizure detection [19].

For general biomedical applications, which include multi-biosignals such as (EEG, ECG, EMG, EOG), parameters like high CMRR, tunable gain, and bandwidth are desirable for amplifying different biomedical signals besides low noise and low power. Huang *et al.* [20] proposed a novel analog front end integrated circuit (AFEIC) that has a current balancing instrumentation

amplifier (CBIA) for biomedical applications that achieves low noise, low power, high CMRR, high gain, and high PSRR simultaneously. The gain is programmable from 52.6dB – 80.4dB so as to amplify the various biosignals and the bandwidth is selectable. The advantage of using CBIA is improved CMRR because a high swing cascade current mirror is used instead of a simple current mirror. Other techniques such as the current mode instrumentation amplifier, shown in Figure 7 [21], have been used to amplify biomedical signals with high CMRR and configurable gain.

The main advantage of this topology is that CMRR remains almost constant in spite of the changing differential gain. The major drawback of using the instrumentation amplifier is that it has high power consumption and also requires too many resistors due to which the battery operating time is reduced and the area cost is increased. Thus, Chebli *et al*. [7] proposed a technique of chopped logarithmic programmable gain amplifier (CPLGA), as shown in Figure 8, dedicated for EEG acquisition systems, which has several advantages over conventional instrumentation amplifiers (IA), such as high CMRR, PSRR, low noise, wide bandwidth, non-cross distortion, etc.

Figure 7. Current Mode Instrumentation Amplifier (CMIA) [21].

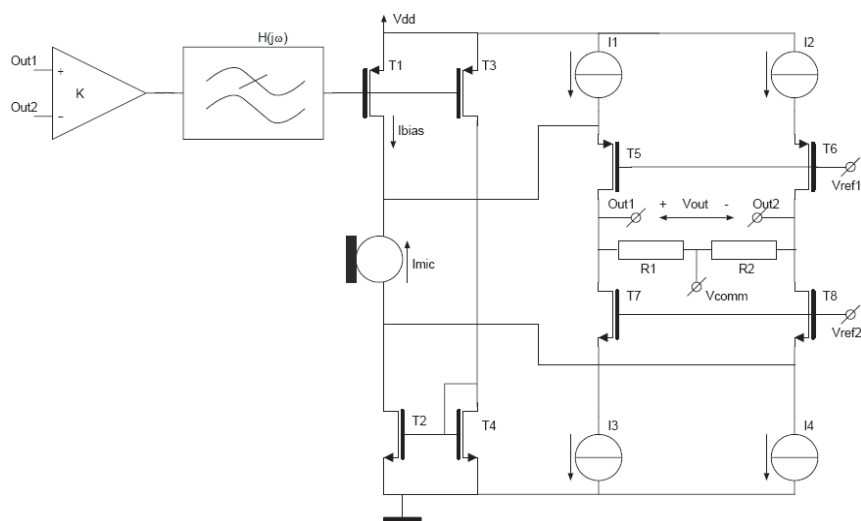**Figure 8.** Chopped Programmable Logarithmic Gain Amplifier (CPLGA) [7].

Much of the research is also done on cochlear implants. These bionic implants require a front end with a wide dynamic range, minimum external components, low power, and good PSRR. A high PSRR ensures that the analog-to-digital converter is not exposed to distortion errors and effects of aliasing that are mainly caused by high frequency supply noise. The designs used previously had a custom external electret structure [22]. A technique of non-custom JFET buffered microphone has been proposed in [23], as shown in Figure 9, where the output current instead of output voltage is transduced by using a sense amplifier topology, thus achieving a good PSRR. FET amplifiers reduce flicker noise but have several disadvantages like higher power consumption, limitations on SNR, and need for external components.

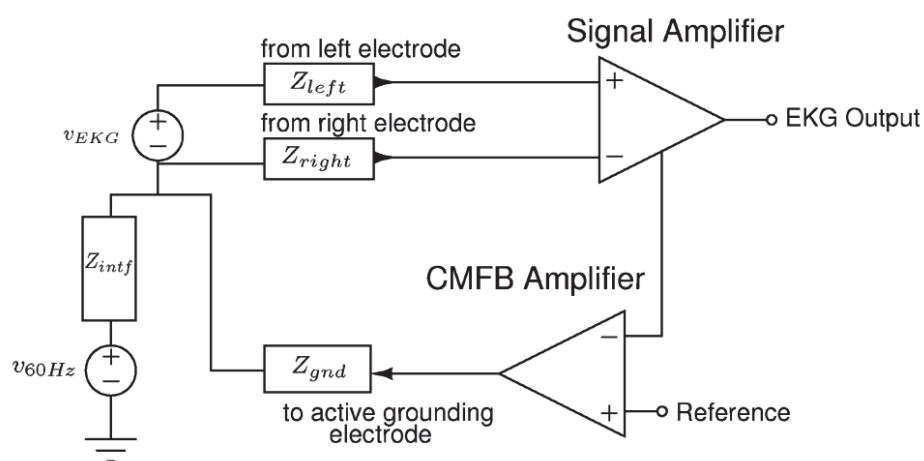**Figure 9.** Sense Amplifier Topology with Split frequency feedback [23].

Therefore, a preamplifier has been described [24] with improved biasing technique suitable for use in cochlear implants. A differential circuit with current mirroring as shown in Figure 10 has also been used; it achieves SNR of > 80dB in a frequency band of 100Hz-10kHz and a total harmonic distortion better than -55dB, is better than the FET preamplifier with SNR of around 60-65dB. It does not require any external components; it only requires two input pins.

Figure 10. Differential amplifier with Current Mirror [24].

For implantable ECG applications, some parameters such as size, weight, battery, and power consumption are of prime importance. Burke *et al*. [25] described an instrumentation amplifier with a low power consumption of $30\mu W$ from 3.3V for heart rate monitoring based on dry electrode recording; it is used for applications where long term monitoring of ECG is required. An analog front end for QRS detection [26] is presented with a current consumption of 600nA, a programmable gain of 36dB - 56dB, and a supply voltage ranging from 1.8 to 2.8V using 0.35um CMOS technology. Further, an instrumentation amplifier with an added Common mode feedback as shown in Figure11 [27] for electrocardiogram applications has been reported to have less power consumption and achieve a CMRR of 90dB, which is suitable for this particular application. CMRR becomes an important parameter here because of the large amount of 60Hz hum in biopotential recording.

Figure 11. Electrocardiogram amplifier with CMFB [27].

4. DISCUSSION

Neural implantable devices, EEG, and Cochlear Implants are covered by a major portion of the survey, while Cardiac Pacemaker, Deep Brain stimulation, Retinal Prostheses being the less explored applications. The key design parameters of an amplifier are its Gain, stability, power consumption, CMRR, PSRR, Noise, THD, Dynamic range, etc. Different applications demand different parameters that are critical to those particular applications. Some applications like Neural Implantable devices require a low noise, low power analog front end while others like cochlear require a high PSRR, good SNR, etc. The main parameters explored so far in the survey are the Input referred noise and power consumption for neural implantable devices. The less explored parameters are the Input referred noise, output swing, THD, and Dynamic range for ECG applications. The Input referred noise represents how much the input signal is affected by the circuit's noise. Thus, it can be said for the ECG signal that 60Hz hum can cause interference with the ECG signal (0.05Hz-250Hz). Also, Output swing becomes an important metric while we are considering reduced supply voltage. A large output swing allows input and output to be short circuited, which makes it easier for the selection of input common mode level.

The trends and various parameters obtained along with the comparison for the different applications are shown graphically in figures 12-15.
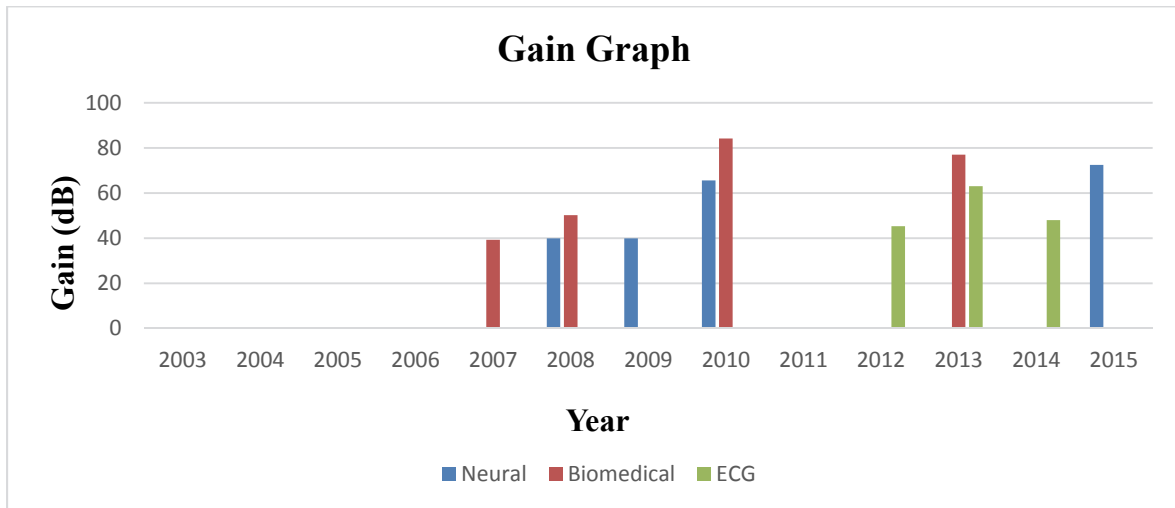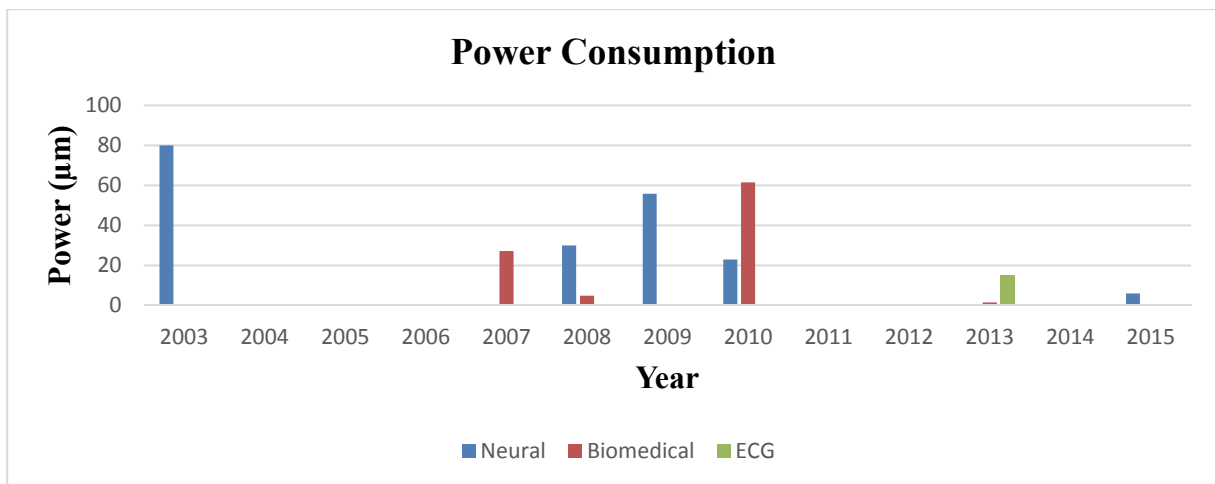
Figure 12. Gain trend for various applications.

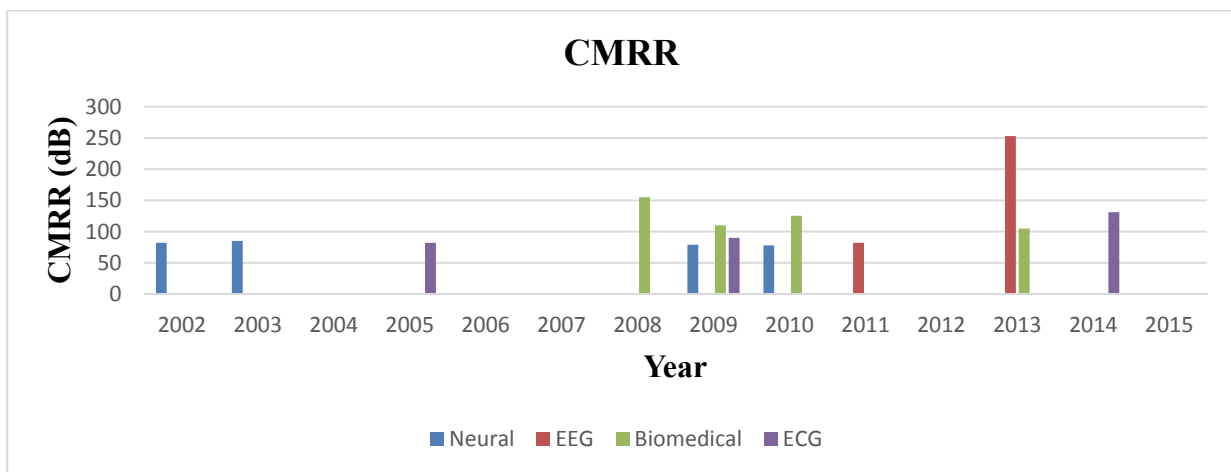**Figure 13.** Power Consumption trend for various biomedical applications.

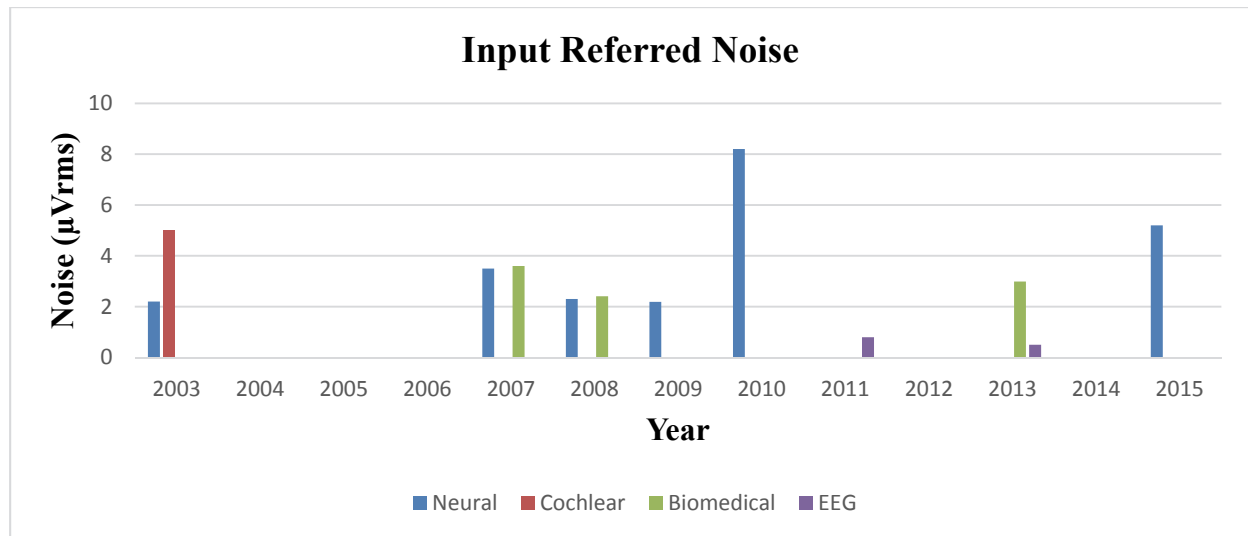**Figure 14.** CMRR performance trend for various biomedical applications.

Figure 15. Input Referred Noise performance trend for various biomedical applications.

Table 1 Performance comparison of some recently reported low power preamplifiers

Paper	Application	Technique used	Input Amplitude	Input frequency	Power Supply (V)	Gain (dB)	Band width	CMRR (dB)	PSRR (dB)	Noise (Vrms)	Power (W)
[10]	Nerve Cuff Recording	OTA	50µV-500µV	0.1Hz-10kHz	±2.5	40	14KHz	82	-	290n	1.3m
[28]	Neural Recording application	OTA	50µV-500µV	0.1Hz-10kHz	±2.5	-	7.2KHz	≥85	≥83	2.2µ	80µ
[29]	QRS detection	Pseudo differential preamplifier	-	-	1.0-1.8	59	8Hz-30Hz	82	-	-	-
[30]	Neural applications	OTA with CMFB	50µV-500µV	0.1Hz-10Hz	3	39.9	0.1-20KHz	-	-	2.3µ	30µ
[9]	ECG	Two stage Instrumentation amplifier	5µV-5mV	0.05Hz-250Hz	-	45.3	290Hz	90	-	8.1µ	2.8µ
[16]	Neural Recording application	True Logarithmic Amplifier	50µV-500µV	0.1Hz-10kHz	1.2	64.6	0.1Hz-20KHz	-	-	6.7µ	11µ
[31]	Biomedical (EEG,ECG,PCG)	PMOS instrumentation amplifier	-	-	1.8	84.2	-	125	125.3	-	61.5043µ
[19]	DBS	FCSOTA	-	-	2.8	39.4	0.36Hz-1.3KHz	66	80	3.07µ	2.4µ
[7]	EEG	Chopped Logarithmic amplifier(CPLGA)	0.5µV-100µV	0.5Hz-40Hz	1.8	40	-	253	235	500n	99µ
[32]	Biomedical (EEG,ECG,PCG)	OTA with folded cascode	2.5mVpp	-	1V	67.81	-	104.95	-	9µv/√Hz	7.24µ

The graphical analysis shows that the previous gain of 30 dB increases to a maximum of 84.2dB for biomedical applications, and power consumption as low as 2.4 μW is achieved. The CMRR trend shows improvement, from 50dB to 253dB. The input referred noise is reduced to around

2.2μVrms from a maximum of 8.1μVrms. The various bio-amplifiers were compared on the basis of performance related parameters like gain, Power consumption, CMRR and noise, and the comparison is provided in Table 1.

5. CONCLUSION

This paper presents a review of various preamplifier topologies for different biomedical applications. The comparison was done based on some performance parameters like gain, power, CMRR, PSRR, and Noise. The amplitude and frequency ranges for the various applications are also evident from the comparison table. Here, various methods were employed to reduce the power consumption and minimize the effects of flicker noise that are dominant at low frequencies. Thus, future work will consider further optimization, to ultra-low power level. Also, different applications such as retinal prostheses and DBS can be considered since much of the work was done on neural implantable devices. Further improvement in gain and CMRR using a new technique can also be considered but with an optimized design trade-off between the various parameters.

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