

UNIVERSITI MALAYSIA PERLIS
SCHOOL OF MICROELECTRONIC ENGINEERING

**ANALOGUE DIGITAL CONVERTER for E-TONGUE
APPLICATION**

by

AMIN JAMAIN BIN MOHD KHAIRY

©

Thesis for the degree of Microelectronic Engineering

June 2011

DECLARATION OF AUTHORSHIP

This project report titled Analogue Digital Converter for E-tongue Application was prepared and submitted by Amin Jamain B. Mohd Khairy (Matrix Number: 071010053) and has been found satisfactory in terms of scope, quality and presentation as partial fulfilment of the requirement for the Bachelor of Engineering (Electronic Engineering) in Universiti Malaysia Perlis (UniMAP).

Checked and Approved by

(RAZAIDI BIN HUSSIN)
Project Supervisor

ANALOGUE DIGITAL CONVERTER for E-TONGUE APPLICATION

ABSTRACT

This work presents a report on designing analogue digital converter (ADC) for e-tongue application. In work for convert an analogue signal from the measurement subject to digital signal which is will be process by another device. In a standard 0.35 μ m CMOS technology, 3-bits flash ADC is design in Mentor Graphic software. This device are consists of 8 comparator, 1 priority encoder and 3 flip-flop circuit. The proposed ADC is used 2.5V and -2.5V power supply to full operating speed. Minimum output of ADC is 0.0V, while the maximum output is 2.5V.

PENUKAR ANALOG-DIGIT BAGI APLIKASI E-LIDAH

ABSTRAK

Kajian ini mengenai laporan kepada rekabentuk penukar analog-digit (ADC) untuk aplikasi e-lidah. Di dalam peranti ini ia menukar isyarat analog daripada sumber menjadi isyarat digital yang akan diproses oleh peranti lain menjadi satu sistem. Dengan menggunakan teknologi CMOS standard 0.35um, 3-bit flash ADC direka menggunakan perisian ‘Mentor Graphic’. Peranti ini terdiri daripada 8 pembanding, 1 pengekod keutamaan dan 3 litar flip-flop. ADC yang direka ini menggunakan 2.5V dan -2.5V power supply untuk membolehkan ia beroperasi penuh. Voltan keluaran minimum ADC adalah 0.0V, manakala voltan keluaran maksimum adalah 2.5V.

ACKNOWLEDGEMENT

First of all, I would like to praise God Almighty for giving me the strength and faith to always stay strong through the heavy storm and the sunny sky while doing my Final Year Project (FYP). My most gratitude goes to my Supervisor, Mr. Razaidi Bin Hussin, who has dedicated his heart and mind to ensure that my project will be completed on time. I would also like to express my full appreciation towards my Mentor, Pn. Norina Bt Idris, which both has guided me in my project, providing me with technical knowledge and shaping my skills as a future engineer throughout my final year. In this little moment I would also like to all PLV and technicians for support that you gave us. In additional my thanks also go to the each and every student of Microelectronic and Electronic, who has helped me beyond the expression of words in allowing me to be a part of the family. Not to forget all lecturers from School of Microelectronic, UniMAP and my friends who are also under supervision of Mr. Razaidi Bin Hussin. The support and encouragement from the people above will always be pleasant memory throughout my life.

TABLE OF CONTENTS

DECLARATION OF AUTHORSHIP	ii
ABSTRACT	iii
ABSTRAK	iv
ACKNOWLEDGEMENT	v
TABLE OF CONTENTS	vi
LIST OF TABLE	ix
LIST OF FIGURE	x
ABBREVIATIONS	xii
1. Introduction	
1.1 Introduction.....	1
1.2 Research background.....	1
1.3 Research statement.....	2
1.4 Research objective.....	3
1.5 Thesis structure.....	3
2. Literature review	
2.1 Introduction.....	4
2.2 ADC architecture.....	5
2.2.1 Flash converter.....	5
2.2.2 Successive approximate ADC.....	5
2.2.3 Integrated ADC.....	6
2.2.4 Delta sigma ADC.....	7
2.3 Introduction of comparator.....	8
2.3.1 Static characteristic.....	8
2.3.2 Dynamic characteristic.....	9
2.4 Introduction to current mirror.....	10
2.5 Introduction to CMOS.....	13

2.6 Introduction to analogue design.....	14
2.7 Basic MOS device physical.....	15
2.8 Schematic design.....	18
2.9 Summary.....	18
3. Methodology	
3.1 Introduction.....	20
3.2 Design methodology.....	21
3.3 Process detail.....	22
3.3.1 Design architect software (DA)	23
3.4 Analogue digital converter circuit design	24
3.4.1 Design a comparator.....	25
3.4.2 Design a priority encoder.....	28
3.4.2.1 AND gate.....	28
3.4.2.2 OR gate.....	29
3.4.2.3 NOT gate.....	31
3.4.2.4 NAND gate.....	32
3.4.2.5 Combination of gate logic.....	33
3.4.3 Design a D-latch.....	34
3.4.4 Combination of circuit block.....	35
3.5 Summary.....	36
4. Result and discussion	
4.1 Introduction.....	37
4.2 Comparator analysis.....	37
4.2.1 Current mirror.....	37
4.2.2 Comparator circuit analysis.....	39
4.2.3 Minimize slew rate.....	41
4.3 Priority encoder analysis.....	43
4.3.1 Gate logic analysis.....	43
4.3.1.1 AND gate.....	43

4.3.1.2 OR gate.....	48
4.3.1.3 NOT gate.....	50
4.3.1.4 NAND gate.....	52
4.3.2 Combination of logic gate analysis.....	56
4.4 D-latch analysis.....	59
4.5 Combination of circuit block analysis.....	61
4.6 Summary.....	66
5. Conclusion	
5.1 Summary.....	67
5.2 Recommendation.....	68
5.3 Commercialization.....	68
Reference.....	69
Overview of Analogue-to-Digital Converter for E-Tongue.....	
82	
Technical paper ADC for E-Tongue Application.....	
89	
Appendix	
A.1 Circuit design.....	95
A.2 Test bench diagram.....	102

LIST OF TABLES

Table 1: AND gate truth table	41
Table 2 : OR gate truth table	42
Table 3: Truth table for NOT gate	43
Table 4: truth table of NAND gate	45
Table 5: Truth table of priority encoder	45
Table 6: Truth table for D-latch.....	46
Table 7: V_{bias} Vs Current	50
Table 8: Voltage gain	52
Table 10: Slew rate.....	53
Table 10: Binary converter decimal.....	68

© This item is protected by original copyright

LIST OF FIGURES

Figure 1: Block diagram of ADC	16
Figure 2: Flash converter	17
Figure 3: Successive approximate ADC	18
Figure 4 : Integrated ADC	19
Figure 5: Delta sigma ADC.....	20
Figure 6: Ideal transfer curve of a comparator.....	21
Figure 7: Transfer curve of comparator with finite gain.....	21
Figure 8: n-channel current mirror.....	22
Figure 9: Definition current by voltage resistive	23
Figure 10: Diode connected device providing an inverse function	25
Figure 11: Basic current mirror	25
Figure 12: MOS symbol	28
Figure 13: Four terminals with the substrate denoted by “B” (bulk).....	28
Figure 14: CMOS circuit	29
Figure 15: I-V characteristic	30
Figure 16 : Flow Chart.....	34
Figure 17 : Process step by using DA software	35
Figure 18 : Schematic diagram.....	36
Figure 19: Block diagram of ADC.....	37
Figure 20: Comparator circuit design	39
Figure 21: Symbol AND gate 2 input, AND gate 3 input, AND gate 4 input.....	40
Figure 22: OR gate	42
Figure 23: NOT gate.....	43
Figure 24:NAND gate 2-input, NAND gate 3-input, NAND gate 4- input symbol	44
Figure 25: D-latch symbol	47
Figure 26: Current mirror.....	50
Figure 27: Graph Current Vs Bias voltage	51
Figure 28: Transfer function	52
Figure 29: Graph capacitor vs slew rate	53

Figure 30: Output of comparator with $C_{II}=500\text{fF}$	54
Figure 31: Output of comparator with $C_{II}=1000\text{fF}$	54
Figure 32: Output of comparator with $C_{II}=2500\text{fF}$	55
Figure 33: AND gate with 2-inputs	57
Figure 34: AND gate with 3-inputs	58
Figure 35: AND gate with 4-inputs	59
Figure 36: OR gate	61
Figure 37: NOT gate	63
Figure 38: NAND gate with 2-inputs	65
Figure 39: NAND gate with 3-inputs	66
Figure 40: NAND gate with 4-inputs	67
Figure 41: Priority encoder	70
Figure 42: D-latch	72
Figure 43	74
Figure 43: Data signal after through the comparator (ADC)	75
Figure 44: 3-bits output binary (ADC)	76
Figure 45: Output after D-latch	77
Figure 47: AND gate with 2-inputs	95
Figure 48: AND gate with 3-inputs	96
Figure 49: AND gate with 4-inputs	96
Figure 50: OR gate with 4-inputs	97
Figure 51: NOT gate	98
Figure 52: NAND gate with 2-inputs	98
Figure 53: NAND gate with 3-inputs	99
Figure 54: NAND gate with 4-inputs	99
Figure 55: Priority encoder	100
Figure 56: D-latch	100
Figure 57: Analogue digital converter	101
Figure 58: Gate logic	102
Figure 59: Priority encoder	102
Figure 60: D-latch	103

ABBREVIATIONS

<i>ADC</i>	Analogue-to-digital converter
<i>MOSFET</i>	Metal oxide semiconductor field effect transistor
<i>CMOS</i>	Complementary metal oxide semiconductor
<i>nMOS</i>	n-channel metal oxide semiconductor
<i>pMOS</i>	p-channel metal oxide semiconductor
<i>SAR</i>	Successive-approximation Register
<i>DAC</i>	Digital-to-analogue converter
$T_{\text{discharge}}$	Time discharged
V_{ref}	Reference voltage
V_{bias}	Bias voltage
I_{ref}	Reference current
V_{OH}	High output voltage
V_{OL}	Low output voltage
ΔV	Voltage difference
V_{DS}	Drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_{TH}	Threshold voltage
W/L	Ratio of width and length
K'	transconductance
λ	lambda
μm	micrometre
nm	Nanometre
<i>PVT</i>	Pressure, Volume, Temperature
A_v	Voltage gain