Linearity improvement of 5.2-GHz CMOS up-conversion mixer for wireless applications

Abstract

This letter presents linearity improvement up-conversion mixer at 5.2 GHz for wireless applications. The design is based on Gilbert-cell active double-balanced mixer using derivative superposition method for linearity improvement. The design improvement is proposed in TSMC 0.18-μm CMOS process. The linearity of the designed mixer is further improved using source degeneration inductors at transconductors stage. The measurement results indicate that the proposed method shows the third-order intercept point (IIP3) of 13.5-dBm, which is higher than previously published mixers. The mixer achieves the conversion gain of 2 dBm, and consumes 3.0 mA at 1.8 V power supply. The size of the whole chip is 0.56 mm^2.