CHAPTER 3

METHODOLOGY

3.1 Introduction

IC manufacturing involves many process steps. This chapter describes the integration of these process steps in NMOS and PMOS fabrication. It takes up to 5 masks and several process steps to finish. Every step is related to other steps. For MOS transistor processes, the steps can be classified as well formation, isolation and interconnection. Well formation and isolation are front end processes, whereas interconnection are back end process.

3.2 Project Strategy & Timeline

Table 3.0: Gantt chart

Month	Aug				Sept	Dec		Jan				Feb				March				April		
week	5	6	7	8	9	24	25	1	2	3	4	5	6	7	8	9	10	11	12	13	15	16
Phase 1 (Sem 1)	*SEMESTER I*																					
Redefine the strategy																						
1.Identify the transistor (NMOS & PMOS)																						
2.Revise the current leakage																						
3.Identify the technique and process flow																						
4.Design the transistor's mask																						
Phase 2 (Sem 2)	*SEMESTER II*																					
1.Presentation Part 1																						
2.Fabricated the transistor																						
3.Measure the leakage current																						
4.Monitor the characterization																						
5.Report writing																						
6.Final Draft Report																						
7.Log Book																						
8.Presentation Part 2																						
10.Final Report Submission																						

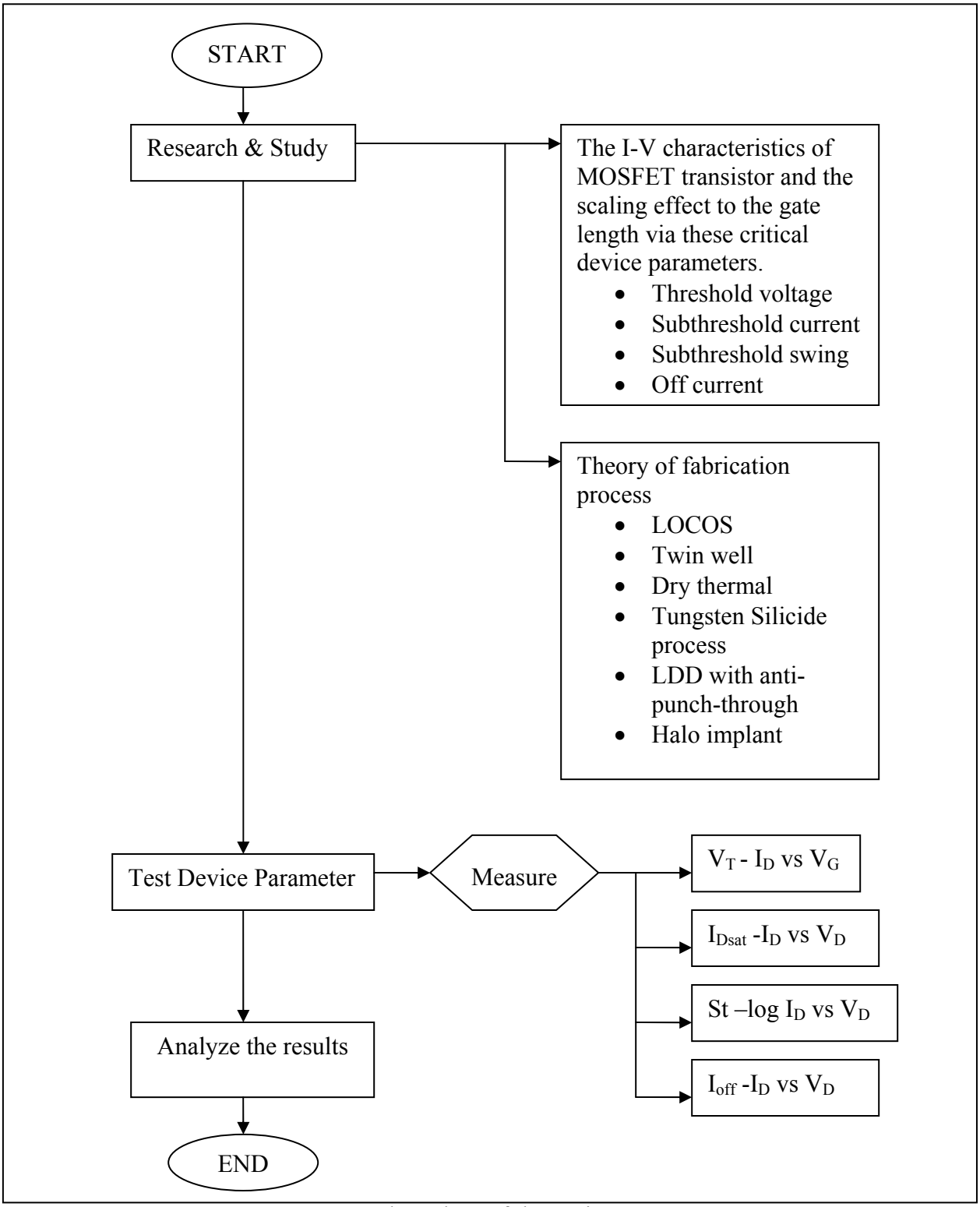

Figure 3.0: Flow chart of the project strategy

3.3 MOSFET Fabrication Process Flow

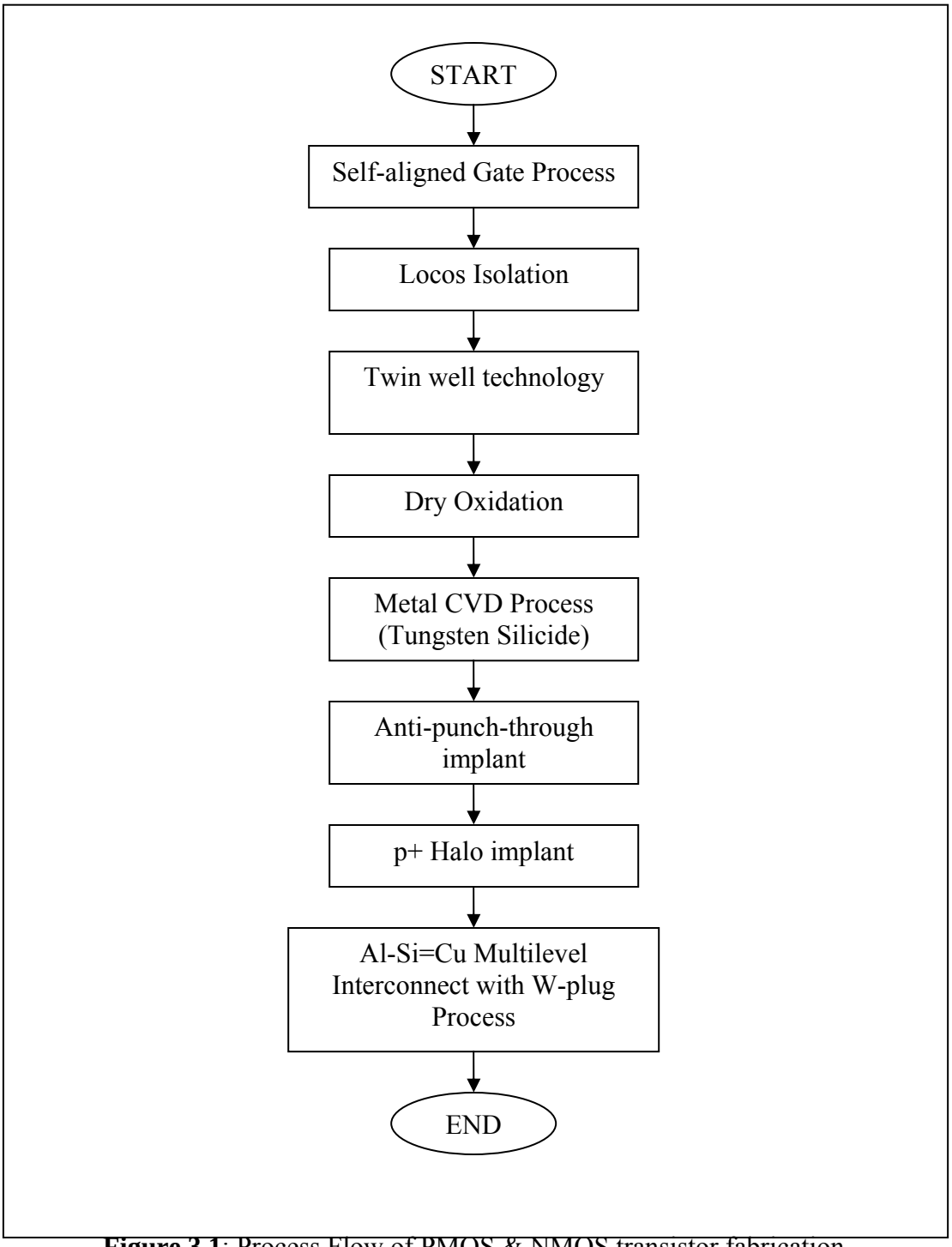

Figure 3.1: Process Flow of PMOS & NMOS transistor fabrication

3.4 MOSFET Fabrication Process Technology

Sample wafer from MIMOS (M) BHD had been used in this project. It is an 8 inch wafer with single poly double metal 0.5µm CMOS technology that consist the test structure for NMOS and PMOS transistor. Each of the test structure is distinguishable of their gate lengths which are 0.3µm, 0.35µm, 0.4µm, 0.45µm, 0.5µm and 10µm whereas their width is 20µm.

The main technology features in this 0.5µm CMOS are Self aligned gate process by using single Poly Double Metal 0.5µm which is normally deposited with the LPCVD process, either SiH_4 or SiH_2Cl_2 can be used as the silicon precursor.Next, Local Isolation of Silicon (LOCOS), a process that uses a thin layer of oxide (200 to 500Å) as the pad layer to buffer the strong tensile stress of the LPCVD nitride. The thickness of the LOCOS oxide is 5000 to 10, 000 Å. Then, in twin well technology process, double photo twin well is common in advanced IC chip manufacturing. Both well implantation processes use high energy, low current implanters. The dry oxidation process which is normally operates at about 980°C will produces gate oxide with the thickness of 110Å. For dry oxidation, high purity oxygen gas (O_2) is used to oxidize silicon. The most commonly used metal CVD processes is tungsten silicide. Tungsten silicide deposition normally is used for the gate and local interconnection applications. Anti-punch-through implantation, which is a medium-energy, low-current implantation process, protects transistors against this effect. Anti-punch-through implantation is normally performed with well implantation. Lastly, Al-Si-Cu multilevel interconnects with tungsten plug process. Tungsten CVD process has been introduced to fill the narrow contact and via holes. The basic interconnection process steps are dielectric CVD, dielectric planarization, dielectric etch; tungsten PVD, bulk tungsten removal, metal stack PVD, and metal etch. The most commonly used dielectric is silicate glass, both doped such as PSG or BPSG for PMD, and undoped (USG) for IMD. Dielectric planarization can be achieved with thermal flow (only for PMD), etch back, and CMP. The detailed of the fabrication process have been explained in Appendix A. **Table 3.1** below shows the process step for this 0.5µm CMOS technology.

Table 3.1: Process step of 0.5µm CMOS technology

No	Step	Process Description	Parameter
1.	Pad oxidation	Used as pad buffer buffer layer for silicon nitride layer in both LOCOS and STI formation to buffer the stress tensile.	200Å
2.	Nitride deposition PECVD	Nitride layer is used as an oxidation mask layer which allows only the thick silicon dioxide (LOCOS) layer to grow at designated area.	1500Å
3.	Active pattern etch	To open area for N-well regions	
4.	LOCOS oxidation	Isolation between active devices	4000Å
5.	Nitride strip	To remove nitride layer	
6.	P-well pattern and P-well implant	The formation of P-well for NMOS	Boron 180keV
7.	BFI Implant	Boron implantation used to increase the threshold voltage of the parasitic PMOSFET in the field region of p-wells	Boron 100keV

8.	NMOS Vt. adjust	Process of controlling the Vt of transistor using low energy and low current implantation process.	BF +70keV
9.	N-well pattern and N-well implant	The formation of N-well for PMOS	P+ 526keV
10.	Anti punchthrough implant	Medium energy and low current implantation process to protect transistor against anti punchthrough effect	P+ 230keV
11.	Vt. adjust (PMOS)	Process of controlling the Vt of transistor using low energy and low current implantation process	BF +70keV
12.	Annealing	Restructure of silicon damaged lattice	800°C
13.	Gate oxidation	To growth the gate oxide	110Å
14.	Undoped Poly deposition	Formation of gate	
15.	Polysilicon implantation	The gate is doped with phosphorus by ion implantation.	P+ 15keV

16.	Polysilicon deposition (WSix)	Polycide deposition to reduce the sheet resistance	1500Å
17.	SiON deposition	SiON is formed by reacting SiH4 with N20 and NH3.It is used to improve thermal stability, low stress and crack resistance.	
18.	Gate pattern and etch	Etch the unwanted area to pattern the gate	
19.	Poly-oxidation	Poly reox process	
20.	N-LDD implant	LDD implant at the P-well underneath the gate oxide layer	
21.	P-LDD pattern	Designated area for P-LDD implant is patterned	
22.	Halo implant	Low energy and low current implantation process with 45°C incident angle	P+ 110keV
23.	P-LDD implant	LDD implant at the n well underneath the gate oxide layer	BF2 +55keV

24.	LDD annealing	Restructure the silicon damaged lattice due to LDD process.	
25.	Spacer oxide deposition	A conformal layer of dielectric silicon dioxide is deposited over the entire wafer	
26.	Spacer etch	An isotropic etch process is used to clear the oxide in the flat areas while leaving sidewall spacers on the side walls of the poly gates.	
27.	N+ S/D pattern and implant	N+ is implanted into the open patterned area.	
28.	P+ S/D pattern and implant	P+ is implanted into the open patterned area	
29.	PMD	Deposition of premetal dielectric layer	11kA
30.	BPSG reflow	BPSG reflow used to completely stabilize the BPSG films which would otherwise be prone to blistering	

31.	Contact pattern and etch	Contact windows are opened in this dielectric layer to allow electrical connection to be made	
32.	Metal-1 deposition pattern and etch	Metallization layer is deposited	
33.	IMD-1 deposition	Electrically isolation of metal-1 from metal-2	
34.	Via pattern and etch	To establish connection between metal-1 and metal-2	
35.	Metal deposition, pattern and etch	Deposition and patterning Metal-2 layer	
36.	Passivation	Passivation layer is deposited on the wafer surface to prevent from moisture	
37.	Pad etch	Openings are etched into this layer so that a set of special metallization patterns under layer is exposed. These metal are called bonding pad	

3.5 Measurement process

3.5.1 Sample wafer

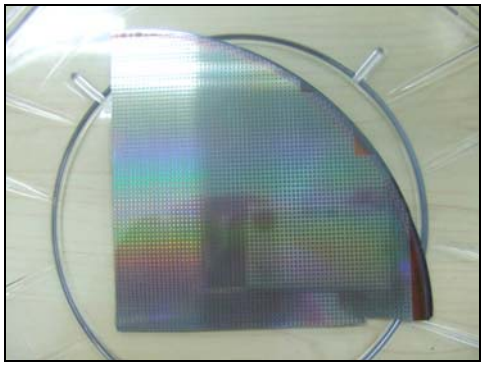

Figure 3.2: Sample wafer for measurement

The sample than have been used in this measurement process was a quadrant or ¼ from 8 inches wafer as depicted in **Figure 3.2**. The NMOS and PMOS transistor have been fabricated including their test structure. The measurements have been done according to their specific I-V measurement.

3.5.2 The MOSFET terminals

The MOSFET becomes a four-terminal device with the terminals designated respectively as the gate G, body B, source S, and drain D. The source and drain terminals of the MOSFET allow a bias V_{DS} to be applied across the ends of the channel region. It's giving rise to a drain current. The inversion layer can be established by applying an appropriate bias to the gate. The induced charge in the channel inversion layer is n-type and the device is known as an n-channel MOSFET or simply an NMOS transistor. A p-channel MOSFET or PMOS is obtained by

interchanging the n and p regions. It is assumed that current in the gate oxide or gate current, I_G is negligible. The MOSFET is a symmetrical device which is the drain current should remain the same if the two terminals are interchanged. Regardless of the way a MOSFET is connected, in NMOS circuits, the terminal tied to the more positive voltage, is defined to be the drain and the other is the source.

3.5.3 Test Information

During the measurement process, the most important part that I must consider was the test information for both, NMOS and PMOS transistors. The test's part is respectively based on drain, source, gate and sub (bulk) pads arrangement on the wafer. The significant of this part is to make sure that the probe will placed and test at the right position The MTC00AZ and MTC00BZ code was represent the NMOS and PMOS transistor respectively. The details of the information as mentioned below:

MTC007X Test information							
	Type	Component	Dimension	Drain (High)	Source (Low)	Gate (-)	Sub (Bulk)
MTC00AZ	NMOS	Tr.	W:20/L:10	1	2	13	14
	NMOS	Tr.	W:20/L:0.50	2	3	13	14
	NMOS	Tr.	W:20/L:0.45	3	4	13	14
	NMOS	Tr.	W:20/L:0.40	4	5	13	14
	NMOS	Tr.	W:20/L:0.35	5	6	13	14
	NMOS	Tr.	W:20/L:0.30	6	7	13	14
MTC00BZ	PMOS	Tr.	W:20/L:10	1	2	13	14
	PMOS	Tr.	W:20/L:0.50	2	3	13	14
	PMOS	Tr.	W:20/L:0.45	3	4	13	14
	PMOS	Tr.	W:20/L:0.40	4	5	13	14
	PMOS	Tr.	W:20/L:0.35	5	6	13	14
	PMOS	Tr.	W:20/L:0.30	6	7	13	14

Table 3.2: Table shows the test information for NMOS and PMOS transistor

3.5.4 Test Configuration

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	PARAMETER	UNIT	SPEC.	MEASUREMENT CONDITION
MTC00AZ	Vt	V	0.75+/-0.05	Vd=0.1V, Vs=Vsub=0V, Vg=0 to 4v, Maximum Slope
	Idsat	mA	8.5+/-1.5	Vd=Vg=5.0, Vs=Vsub=0v, Measure ID
	Ioff	pA/um	<5	Vd=5.5, Vg=Vs=Vsub=0v, Measure ID
	SubVt	mV/dec	70-100	Vd bias = 0.1V, Vg = 2V, Vsub=0V, Measure log ID
MTC00BZ	Vt	V	-0.8+/-0.1	Vd=-0.1V, Vs=Vsub=0V, Vg=0 to -4v, Maximum Slope
	Idsat	mA	-4.5+/-1.0	Vd=Vg=-5.0, Vs=Vsub=0v, Measure ID
	Ioff	pA/um	>-5	Vd=-5.5, Vg=Vs=Vsub=0v, Measure ID
	SubVt	mV/dec	70-100	Vd bias = 0.1V, Vg = 2V, Vsub=0V, Measure log ID

Table 3.3: Table shows the test configuration for NMOS and PMOS transistor

When devices are fabricated, they must be tested to ensure that the desired characteristics have been produced. **Table 3.3** above shows the test configuration that must be applied to the Semiconductor Parametric Analyzer (SPA) according to the type of parameter.

In this project, the extrapolated- V_T was selected as a method to determine the V_T. The extrapolated- V_T is determined by measuring the drain current as a function of gate voltage. If I_D is plotted vs. V_{GS} and the linear portion of the curve is extrapolated to intercept the voltage axis, the extrapolated-V_T value is yielded.
An important device characteristic in the subthreshold swing, St is the inverse of the slope log I_D versus V_{GS}. In MOSFETs with uniformly doped substrates, St is expressed in units of mV per decade. The output characteristics plot of the I_{Dsat} was measured by using the test parameter, I_D versus V_{DS} with V_{GS} as the parameter on an axis with linear I_D and V_{DS} scales. While for the output characteristics plot of I_{off} was measured by using the test parameter, I_D versus V_{DS} with V_{GS} as the parameter on an axis with linear I_D and V_{DS} scales. The off current can be obtained by giving the drain voltage, V_{DS} = 5.5V, V_{GS}= V_S = 0V.

3.5.5 Equipment

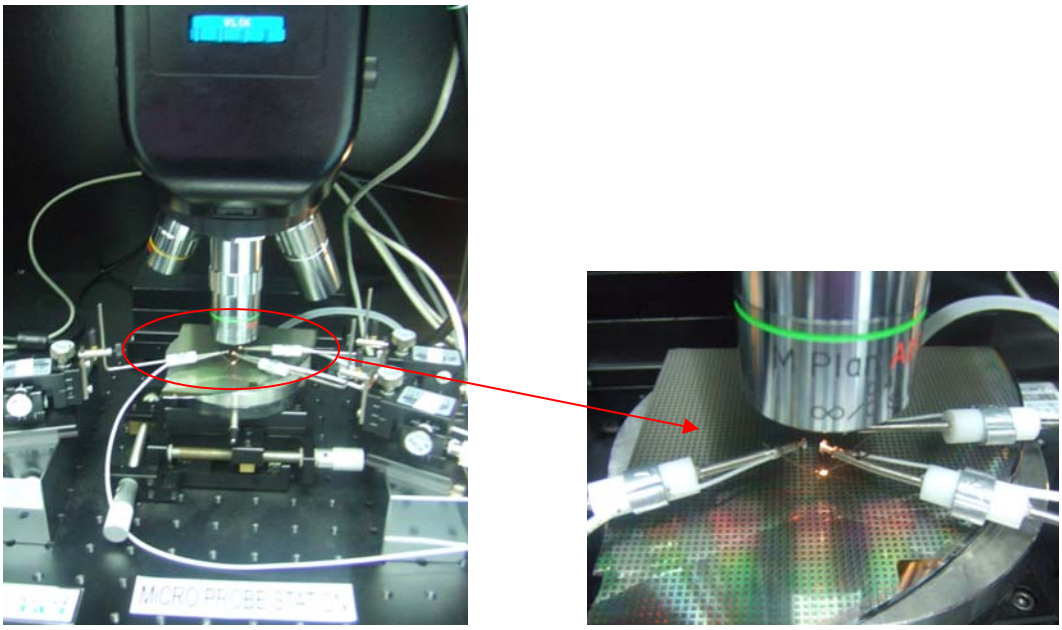

Figure 3.3: The Micro Probe Station

Figure 3.3 above shows the Micro Probe Station which is used as the important equipment in the measurement process. It has four probes that delegate as SMU1, SMU2, SMU3 and GND. This equipment is manually handling instead of the automatic machine that commonly used in the industry. The process is getting started as the wafer was put on a vacuum chuck that holds and can keep the wafer static. Then, the probes will be placed according to the information in **Table 3.2** and it only can be done by looking the test parameter through the high power microscope that have been connected in this micro probe machine. However, precaution steps should be taken while measurement and probing to avoid from wafer scratch or wafer damage.

3.5.6 Software

Figure 3.4: Semiconductor Parametric Analyzer (SPA)

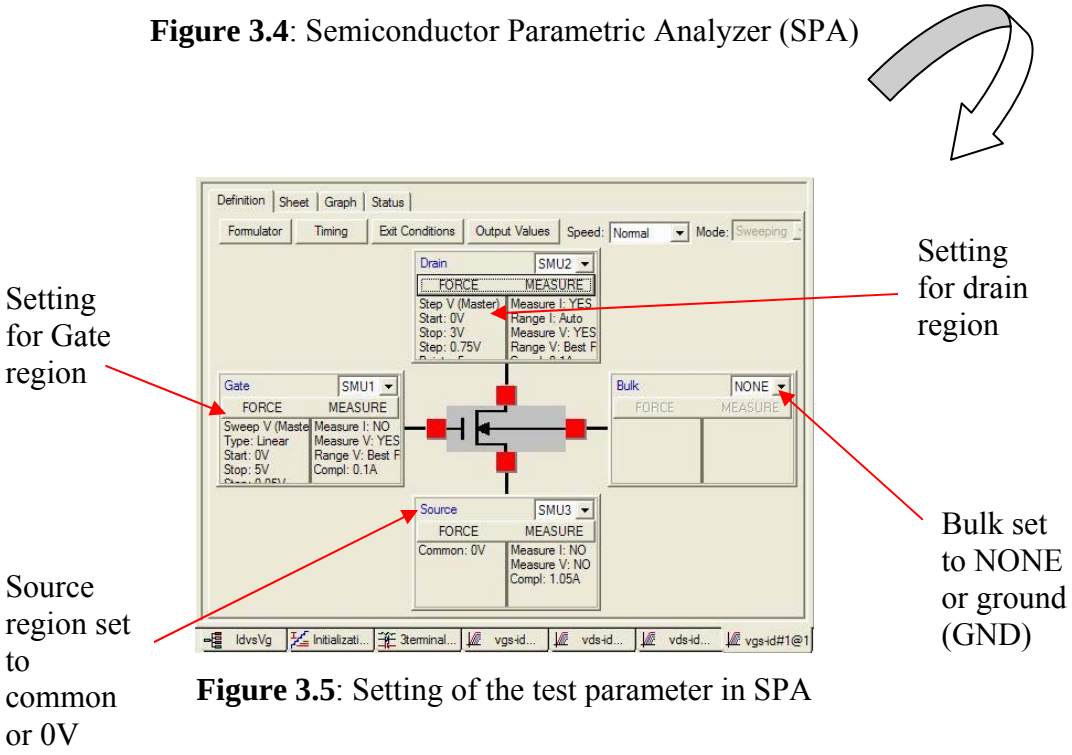

Figure 3.5: Setting of the test parameter in SPA

Figure 3.4 above shows the Semiconductor Characterization System model SCS-4200 from Keithley Instrument while **Figure 3.5** is the setting of the test parameter in Semiconductor Parametric Analyzer. This machine is connected with the Micro probe Station as a function to give the output of the I-V characteristics measurements test. The test is executed by using the Keithley Interactive Test

Environment (KITE) software. Typically the V_T, I_{Dsat}, St and I_{off} measurement can be achieved with this automated parametric test system. The main instruments used in this SPA are source measure units (SMUs).The instruments need to be configured properly as indicate in **Table 3.2** and **Table 3.3** to obtain the accurate current-voltage measure performance.

3.5.7 Testing the test structure

Figure 3.6 shows one of the example of the dimensions of gate length, Lg for NMOS (width =20µm, gate length = 0.45µm) transistor channel under high power microscope. In this process, the width of the gate was not considered. Only the gate length was varied .As shown in **Figure 3.7**, the probe was placed at the source and drain pad and it is variable based on its gate length position. Meanwhile, at the pad number 13, as indicated in **Figure 3.8,** one of the probes was placed to complete and make the device GND. These probes will not lifting from the pad during measurement for every different gate length, Lg until the measurement process finished.

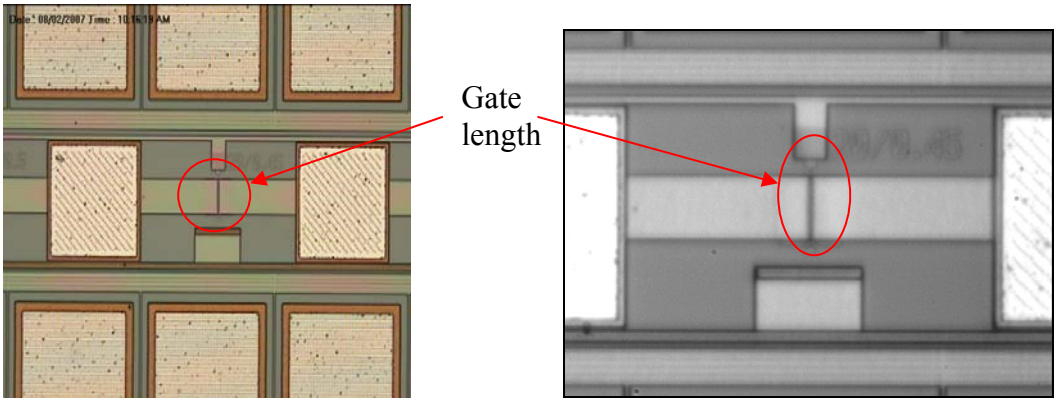

Figure 3.6: The dimension of the NMOS transistor channel

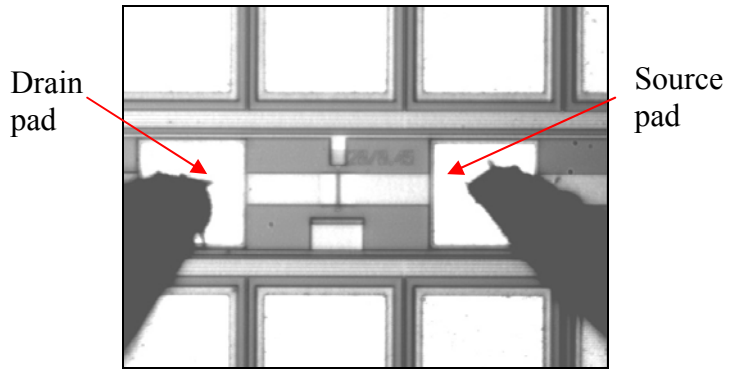

Figure 3.7: The probe was attached on the source and drain pad

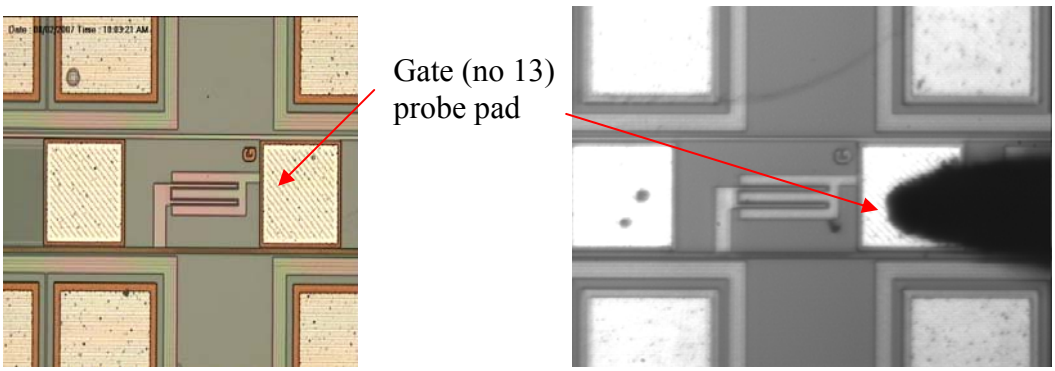

Figure 3.8: The probe was attached on the gate pad under high power microscope