CHAPTER 1

INTRODUCTION

1.1 Background

For more than 30 years, MOS device technologies have been improving at a dramatic rate [1, 2].MOS devices have been scaled down aggressively in each technology generations to achieve higher integration density and performance. For digital integrated circuit, ICs, the main performance criteria are speed, power dissipation and device packing density. Smaller devices also produce the twin benefits of decreased die size which exert downward pressure on die cost. The goal is to produces short channel MOSFETs with long channel behavior. Reduction in device size has been the chief vehicle for achieving these goals. However, the mere reduction of all device dimensions by a constant factor, for example, without paying attention to other processing parameters can adversely impact IC performance.

The scaling of MOS transistor channel length is a subject that has recently attracted great interest. The effect of scaling the gate length is discussed in detail. Fundamental tradeoff and scaling trends in engineering these effects are analyzed through experimental data. The increasing statistical variation in the process parameters has emerged as a serious problem in the circuit design and can cause significant effect in the MOS transistor. Because of small MOSFET geometries, the voltage that can be applied to the gate must be reduced to maintain reliability. The impact of these trends associated with circuit requirements including threshold voltage and off-state leakage on transistor design is also explored. Three of the most important scaling methodologies are constant electric-field scaling and its derivatives, scaling based on subthreshold behavior and scaling to achieve a desired value of subthreshold current, Ioff. Because subthreshold conduction is the dominant short-channel performance issue that limits MOSFET scaling. Much work has

been done approaching this problem from both the experimental and theoretical points of view.

In the case of MOSFETs, the aim of such scaling guidelines is to provide a design path to short channel devices which continue to exhibit the ideal characteristics of long channel devices. The scaling of MOSFET devices and a new generation of technology will continue to be developed every three years [3]. The MOSFET accurately describe many other device characteristics of long channel MOSFETs, including threshold voltage, subthreshold current and the I_D-V_{DS} characteristics in strong inversion. As process technology improved to the point where devices could be fabricated with gate length smaller than ~2µm, it turned out that MOSFETs began to exhibit phenomena not predicted by the long channel MOSFET. The scaling of transistors to smaller dimensions has therefore profound effect on the manufacturing yield and reliability of integrated circuit [4]. They eventually become prone to short channel effects [5]. In most cases however, these effects are considered detrimental. That is, power dissipation may worsen because of increased device leakage currents, or circuit speed may be degraded. Reliability problems which afflict submicron MOSFETs might also be exacerbated including hot carrier degradation, gate-oxide wearout and electromigration.

Short channel effects are caused by the lateral electric fields from the source to channel and drain to channel. The short channel effect arises from the fact that the charge under the gate is to some extent controlled by the source and drains junctions [6].Hot carrier cause the transconductance of transistor to slowly degrade and may cause harmful threshold variation [7]. They also lead to degrade output resistance in analog circuits. This short channel effects can be classified into two groups:

1. Increased leakage current when the MOSFET is “off “.It is due to several phenomena, including lowering of the threshold voltage V_T as L is decreased and/or V_{DS} is increased, the onset of punchthrough at smaller drain biases as L is decreased and an increase in isolation leakage current as the isolation spacing is decreased.

2. Reliability problems that arise in short channel MOSFET include a thin gate oxide breakdown, device degradation due to hot carrier effects and reliability problems associated with the interconnects between MOSFETs.

As a result, it is necessary to employ more sophisticated scaling guidelines for device design to ensure that the shrunken devices exhibit electrical behavior comparable to that of previous generations of larger devices.

1.2 Objectives

The aim of this project was to observe the effect of MOS transistor scaling based on their I-V characteristics. The main objectives were to investigate what are the threshold voltage,$V_{T,}$ subthreshold swing,St, drain current saturation, I_{Dsat} and off current, I_{off} for NMOS and PMOS transistor. These device parameters give the high impact to the device performance as it has been scaling for the requirement of speed and density in integrated circuit technology.

To analyze the graph that had been obtained from the measurement of NMOS and PMOS transistors based on its roll-up and roll-down characteristics. From this, the difference between the short channel and long channel values will be known as the gate length, Lg varied. Thus, the short channel effect will be known as it shows the short channel MOSFET behavior.

To identify the various factors that affect the device parameters, I-V characteristics based on the NMOS and PMOS different gate length.

1.3 Scope of study

This study was designed to understand the use of the I-V characteristics as the critical parameter in the NMOS and PMOS transistor and the effect according to the MOS transistor scaling. An analysis was done by using Semiconductor Parameter Analyzer as the machine that can provide the I-V graph and Micro Probe Station which is workings as a probe tester on the sample wafer. The result of the graph had been examined and an analysis is done according to its different gate length. Then, the result had to be compared with other established sources where similar work has been done.

1.4 Expected finding

The two major goals of MOSFET scaling are to increase the density and speed of the digital ICs. Increasing density obviously means using smaller channel lengths and widths. To increase the speed of the digital ICs, the MOSFET saturation drain current, I_{Dsat} must be increased. From the long channel MOSFET, a decrease in either the channel length Lg or gate oxide thickness t_{ox} will lead to an increase in I_{Dsat}. However, when the devices have been fabricated with gate lengths smaller than 2µm, I_{Dsat} shows far less increase as Lg is decreased. This phenomenon was thus termed as short channel effect. As the dimensions of the Lg are reduced, threshold voltage V_T will decrease. Less gate charge and a smaller vertical field is needed to cause inversion. This makes it appear that a smaller V_T is needed to turn on a short channel device.

The subthreshold swing, St indicates how effectively a MOSFET can be turned OFF as V_{GS} is decreased below V_T. The St will increases as the Lg decrease. Reduction of the gate length causes severe short channel effect in which a degradation in the subthreshold characteristics and arises due to drain induced barrier lowering and punchthrough between the source and drain junction. Whereas, the I_{off} will increases as Lg is decrease. It is because as the gate length is reduced in off mode, the current will prone to become leakage.

1.5 Organization of Work

Project will become success as we can achieve and finish them at the right time if it was organized properly. By achieving this purpose, this study was divided into three phase. The first phase was do the measurement and characterized the I-V characteristics. Then, make the data collection to choose the best result among them. While, for the second phase, all the data and result was analyzed and find out the solutions. The last phase was determined the effect of MOS transistor scaling through the analyzed data and conclude the result that had been obtained.