CHAPTER 5

CONCLUSION

5.1 Summary

After going through all the hard work and facing the problems, this project managed to complete its objective that was to study the Wallace Tree multiplier as one of the high speed multiplier designs between all types of multiplier.

It took a couple of weeks to search through the internet to learn about the types of multiplier and their characteristic before the best multiplier for this final year project (FYP) objective could be chose. Next, it took even more time to understand the function and the operation of the Wallace Tree multiplier to produce the best design to complete the objective to be the high speed multiplier. Other than that, familiarization back with the Verilog hardware description language (HDL) programming has to be done after a year has been left.

There are three advantages of using HDL design entry compared to traditional schematic-based design [2].

- Designs can be described at a very abstract level by use of HDLs. Designers can write their register transfer logic (RTL) description without choosing a specific fabrication technology. Logic synthesis tools can automatically convert the design to any fabrication technology. If a new technology emerges, designers do not need

to redesign their circuit. They simply input the RTL description to the logic synthesis tool and create a new gate-level netlist, using the new fabrication technology. The logic synthesis tool will optimize the circuit in area and timing for the new technology [2].

- By describing designs in HDLs, functional verification of the design can be done early in the design cycle. Since designers work at the RTL level, they can optimize and modify the RTL description until it meets the desired functionality. Most design bugs are eliminated at this point. This cuts down design cycle time significantly because the probability of hitting a functional bug at a later time in the gate- level netlist or physical layout is minimized [2].

- Designing with HDLs analogue to compute programming. A textual description with comments is an easier way to develop and debug circuit. This also provides a concise representation of the design compared to gate-level schematic. Gate-level schematics are almost incomprehensible for very complex design [2].

Once the characteristic of Wallace Tree multiplier has been understood and after familiarized with Verilog HDL, the project proceed smoothly as planned except it could not be finish until the field-programmable gate array (FPGA) implementation because of the time constraint.

From the results, it showed that the conventional circuit produces the maximum speed of 14.99 MHz or maximum delay of 66.7 nanoseconds to complete one process of 8-bits x 8-bits multiplication. After upgrading the conventional Wallace Tree into pipelined, by adding D flip-flop stages, the speed has increased to 54.05 MHz and the maximum delay has decreased to 18.3 nanoseconds. Finally, after completed the analysis of the Wallace Tree multiplier, it has been proven that the pipelining method could increased the speed of the multiplier.

Overall, it is satisfied that this project has completed the objective that was to study an 8-bits x 8-bits Wallace Tree multiplier as one of the high speed multiplier among the other types of multiplier in multiplication area.

5.2 Recommendation for Future Project

As the title is high speed 8-bits x 8-bits Wallace Tree multiplier, therefore there will definitely be a continuation of the project's progress. For future development of this project, it is recommended that an upgrade of the speed of the Wallace Tree multiplier by using another method such as reducing partial products or using fast adder, and at perhaps, it could be implementing on the FPGA. It is also suggested that a modification of the multiplier could be made to make it simpler to design its layout. As been state that the Wallace Tree multiplier is difficult to layout because of its irregularity. These improvements will make the Wallace Tree multiplier more acceptable in the multiplication system and presentable to the market.

5.3 Commercialization Potential

High-speed multiplication has become the users' choice nowadays due to its advantages. With the high demand from the users, vast research activities are done in the multiplication system. Competition rises as every products released tends to get more faster. The high speed 8-bits x 8-bits Wallace Tree multiplier produced in this project is only a beginning and not suited to be commercialized yet. However, after a few increment of the project such as upgrading the bits to 32-bits x 32-bits, it is sure that this project will be able to make it to the market especially in digital signal processing (DSP) field as a microprocessor and will have a big reception from the users and the industrial field.