

HIGH SPEED 8-BITS X 8-BITS WALLACE TREE MULTIPLIER

by

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Report submitted in partial fulfillment
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APPROVAL AND DECLARATION SHEET

This project report titled High Speed 8-Bits x 8-Bits Wallace Tree Multiplier was prepared and submitted by Tajul Hamimi Harun (Matrix Number: 041030774) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in Universiti Malaysia Perlis (UniMAP).

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PENDARAB BERKELAJUAN TINGGI 8-BIT X 8-BIT JENIS CABANG WALLACE

Projek tahun akhir (PTA) ini adalah untuk menganalisis pendarab 8-bit x 8-bit jenis Cabang Wallace. Pada masa kini, pendarab-pendarab banyak digunakan di dalam bidang komunikasi dan perkomputeran. Jika dahulu, pendarab yang menggunakan bekalan kuasa yang rendah atau yang melesapkan kadar kuasa yang kecil sering menjadi pilihan untuk digunakan dalam kedua-dua bidang ini. Akan tetapi, kini, satu lagi ciri penting yang dikehendaki oleh kedua-dua bidang ini yang perlu ada pada setiap pendarab, iaitu pendarab yang pantas dapat menyelesaikan pendaraban. Oleh itu, PTA ini mengkaji bahawa pendarab 8-bit x 8-bit jenis Cabang Wallace adalah salah satu pendarab yang pantas di antara jenis-jenis pendarab yang lain. Analisis yang dijalankan adalah daripada tahap litar skematik hingga ke tahap kod pengaturcaraannya menggunakan perisian Altera Quartus II. Daripada keputusan yang diperolehi, terbukti bahawa pendarab 8-bit x 8-bit jenis Cabang Wallace adalah salah satu pendarab yang pantas di antara jenis-jenis pendarab yang lain.

ABSTRACT

This final year project (FYP) is to analyze the design of Wallace Tree multiplier. For simplicity, unsigned operands are chosen and main focus on the short word widths commonly used in most applications: an 8-bit multiplier. Before this era, multiplier that used low power supply or multiplier that has low power dissipation is always being the choice to be used. However, now, there is one more important feature that a multiplier should have that is high-speed to solve multiplication problems. Therefore, this FYP studied that an 8-bits x 8-bits Wallace Tree multiplier is one of the high speed multiplier among the other types of multiplier. The analysis covers from the schematic design until the source code design of the multiplier. Design entry that is used for this project is the Verilog hardware description language (HDL) using the Altera Quartus II software. From the results achieved, it shows that the conventional circuit produces the maximum speed of 14.99 MHz or maximum delay of 66.7 nanoseconds to complete one process of 8-bits x 8-bits multiplication. After upgrading the conventional Wallace Tree into pipelined, by adding D flip-flop stages, the speed has increased to 54.05 MHz and the maximum delay has decreased to 18.3 nanoseconds. Finally, after completed the analysis of the Wallace Tree multiplier, it has been proven that the pipelining method could increased the speed of the multiplier.

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