CHAPTER 5

CONCLUSION

5.1 Summary

The objective of this project is to improve a 16-bit carry save adder in terms of its speed. This is done by modified the basic carry save adder with adding a pipeline. The design method is by using Quartus II Software. Overall achievement, this project has met its objectives.

The carry save adder is based on full adder circuit. To make comparison of this type of adder, five designs has been made using different type of logic gates. These designs as explained in Chapter 2 are:

1. Full adder using XOR, OR and AND gate
2. Full adder using AND and XOR gate
3. Full adder using XOR, NAND and negative OR gate
4. Full adder using XOR and NAND gate
5. Full adder using XOR gate and 2 to 1 multiplexer

Based on observation, full adder No.1 has the most speed compared to others. This circuit has the shortest delay among all of other circuits being made. For all these designs, its delay has being analyzed in the simulation process. Note that the delay can only be seen for a bigger circuit, which may means that each of the designs is being made for six operands.

The bigger the circuit design, the complex the design being, the higher chances careless may be made. Instead of avoiding any connection error, waveform built at the

low-level circuit design to the high-level circuit design as confirmation the design is precisely connected. It is observed that the more complex the design, the bigger delay it produce.

To modify the basic design, a pipeline approach has been made. This is used by D flip-flop; the objective is to give synchronization of the circuit. This results that the inputs will only act at the positive-edge of clock cycle. By using pipeline, the speed of 16.84MHz has been increased to 90.09 MHz using EPF10K70RC240-4 device. The speed is measured using Timing Analyzer Tool.

5.2 Recommendation for future project

Other than using Quartus II software, this design can be made using a transistor level approach using Mentor Graphic software. The design of three level six operands of 16-bits CSA is too complex and detail, therefore the operand value should be decrease for the ease to design in Mentor Graphic. The idea of this CSA design is based or depends on the design of full adder. The smallest area, the high-speed and the stabilize output waveform of full adder needed to get while designing the full adder transistor level design [27] [28]. Also, a keeper is needed in the design to keep the signal higher for the ease of analyze and will produce a smoother waveform [30]. This is the important step for getting the faster speed than using the Quartus II software.

5.3 Commercialize Potential

Instead of being a product that can be commercial, high speed six operands 16-bits carry save adder can be introduce as an intellectual properties, where it have the potential of being an element as a sub product for a software. This project is not a stand-alone equipment, it may be completed with another programs to make it work. For example, this adder is being used in a CPU, and the advantage is to enhance the speed of CPU.