CHAPTER 4

RESULTS & DISCUSSION

4.1 Discussion

From this project, the result achieved do not meet the expected values from calculation that be expected. Some of the values that have been declared do not fulfill the desired value. Apparently, parameters that influence the increase of performance of an amplifier are related to each other.

At the beginning of the design, the circuit need to be tune-up so it can reach the stable current and voltage that is necessary to supply all component. For example, during tune-up session, V_{bias} is tuned so it can supply desired current and voltage to operate the component. Based on the equation from the theory of a transistor in saturation region, the resulting value is the minimum value that can operates the transistor. However the value achieved from theory need to be increased until it get the suitable or stable current or voltage. So, what happens here is a trade-off pattern as mention in Chapter 2.

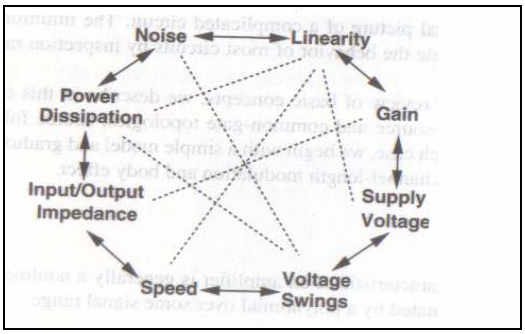

Figure 4.1: Trade Off Pattern in analog design

When the size of a transistor being increase (width size), more current can flow through it, but the consequences, resulting the increment of the resistance in the transistor. Each of the parameter above are related to each other and play an important role to decide the performance of amplifier design. It is important to design trade off [1]. Thus, the parameter are related to each other. Here, the gain is determined by a three factor. The factor are size of transistor $\left(\frac{W}{L}\right)$, drain resistance, R_D , DC voltage and drain current, I_D.

For the first factor, if current and R_D are kept constant, the increase of $\left(\frac{W}{L}\right)$ will not only increase the gain, but it is also increase the gate capacitance. Thus it makes lower bandwidth. Secondly, if I_D and $\left(\frac{W}{L}\right)$ are kept constant, R_D increases and the V_{DS} becomes smaller. Operating point gets closer to the borderline of triode region mode. When the operating point closer to the borderline, it mean less distortion had occured. Thirdly, if I_D decreases and $\left(\frac{W}{L}\right)$ and V_{RD} are kept constant, then R_D must be increased. The reason is R_D consume too much space, increases the noise level and slows the amplifier down.

4.2 Result

4.2.1 Schematic Result

The schematic result achieve after simulation and measurement of the circuit design. However some of the value did not achieve expected calculation from theory. Table 4.1 shows the result that has been determine from the amplifier core .

Table 4.1 Result for Amplifier Core

Port	Value (Measure)	Value (Theory)
V_{in}	0.75V	-
$\left(\frac{W}{L}\right)_1$	$\left(\frac{130um}{0.35um}\right)$	$\left(\frac{130um}{0.35um}\right)$
$\left(\frac{W}{L}\right)_2$	$\left(\frac{25.98um}{0.35um}\right)$	$\left(\frac{25.98um}{0.35um}\right)$
$\left(\frac{W}{L}\right)_3$	$\left(\frac{0.875um}{0.35um}\right)$	$\left(\frac{0.875um}{0.35um}\right)$
$\left(\frac{W}{L}\right)_4$	$\left(\frac{65.25um}{0.35um}\right)$	$\left(\frac{65.63um}{0.35um}\right)$

$\left(\frac{W}{L}\right)_5$	$\left(\frac{21.87um}{0.35um}\right)$	$\left(\frac{65.63um}{0.35um}\right)$
I_{D1}	2.38mA	3.3mA
I_{D2}	0.88mA	0.24mA
I_{D3}	0.25mA	0.12mA
I_{D4}	1.48mA	1.08mA
I_{D5}	0.25mA	0.12mA
V_{out}	3.143V	-

Although some of the result do isolates from theory, but the main concept that the current flow from $I_{D1} \succ I_{D2}$ are still maintained. Gain that is produced by the core amplifier are described as below:-

A_V = (gain of 1st stage) × (gain of the 2nd stage)

Gain of 1st stage = $\frac{i_{M1}}{V_{in}} = \frac{2.38A}{0.75V}$

$= 3.173\Omega^{-1}$

Gain of 2nd stage= $\frac{v_{d3}}{i_{M1}} = \frac{3.143V}{2.38A}$

$= 1.321\Omega$

$A_v = 3.173\Omega^{-1} \times 1.321\Omega$

$A_v = 4.2$ (measure)

The result did not achieve A_v=5, that is the target gain that has been set from specification. The increment of the transistor size which provide more current flow probably the reason of the gain reduction. When the size of transistor been increase, it will also increase the resistance value in it.

4.2.2 Layout Result

Once the schematic completes the setup, all the source for voltage will be replace with input or output port to start running a layout. Layout starts to draw by connecting one port to another until all the connections are finished.

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4.2.3 Design Schematic Layout (DRC)

Referring to **Figure 4.2**, this parts tell the result of design rule check thus are completed and successful. Each metal, poly and well have their own minimum size. If there is an error, the errors has to be clicked and it will highlight the error at the layout.

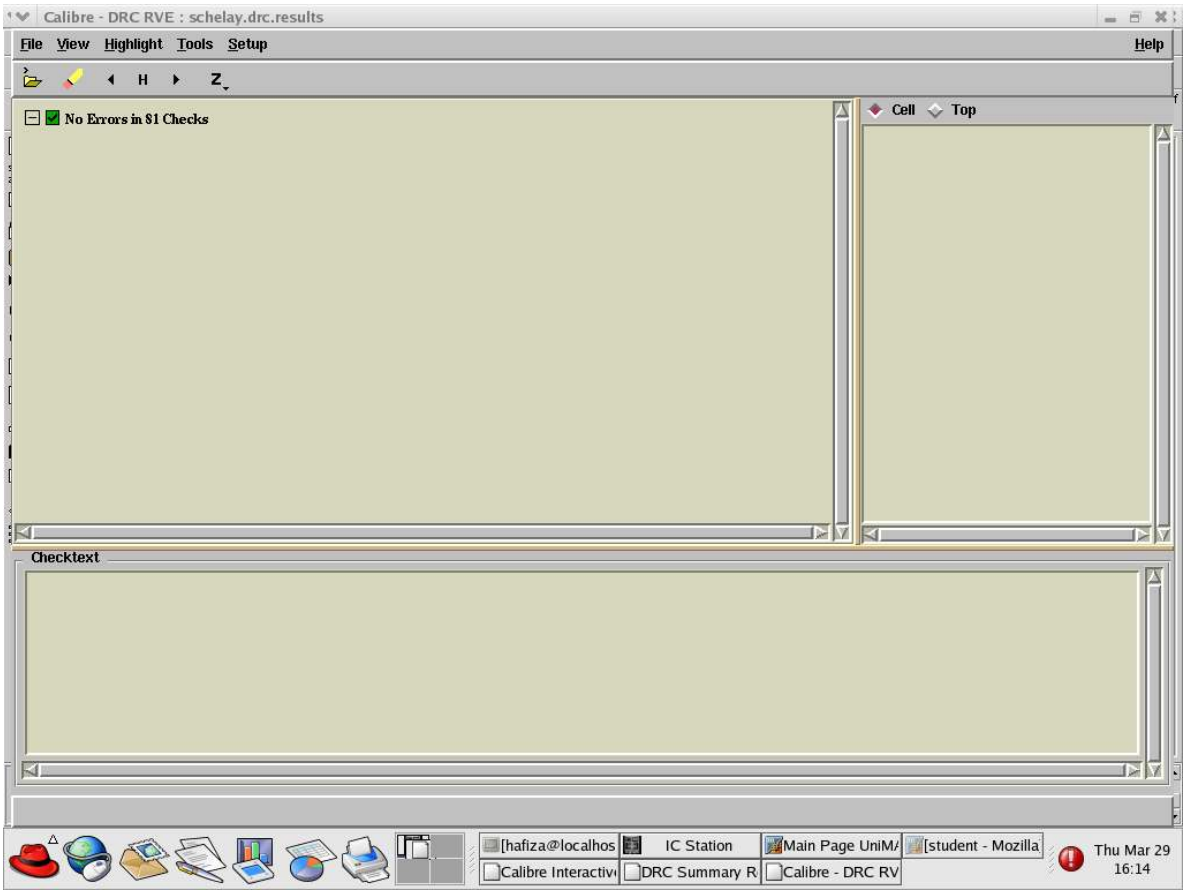

Figure 4.2: Calibre –DRC RVE window

4.2.4 Layout Versus Schematic (LVS)

The Calibre-LVS RVE window shows the simulation result of the LVS test. LVS will compare the electronic interconnection between the schematic and layout design.

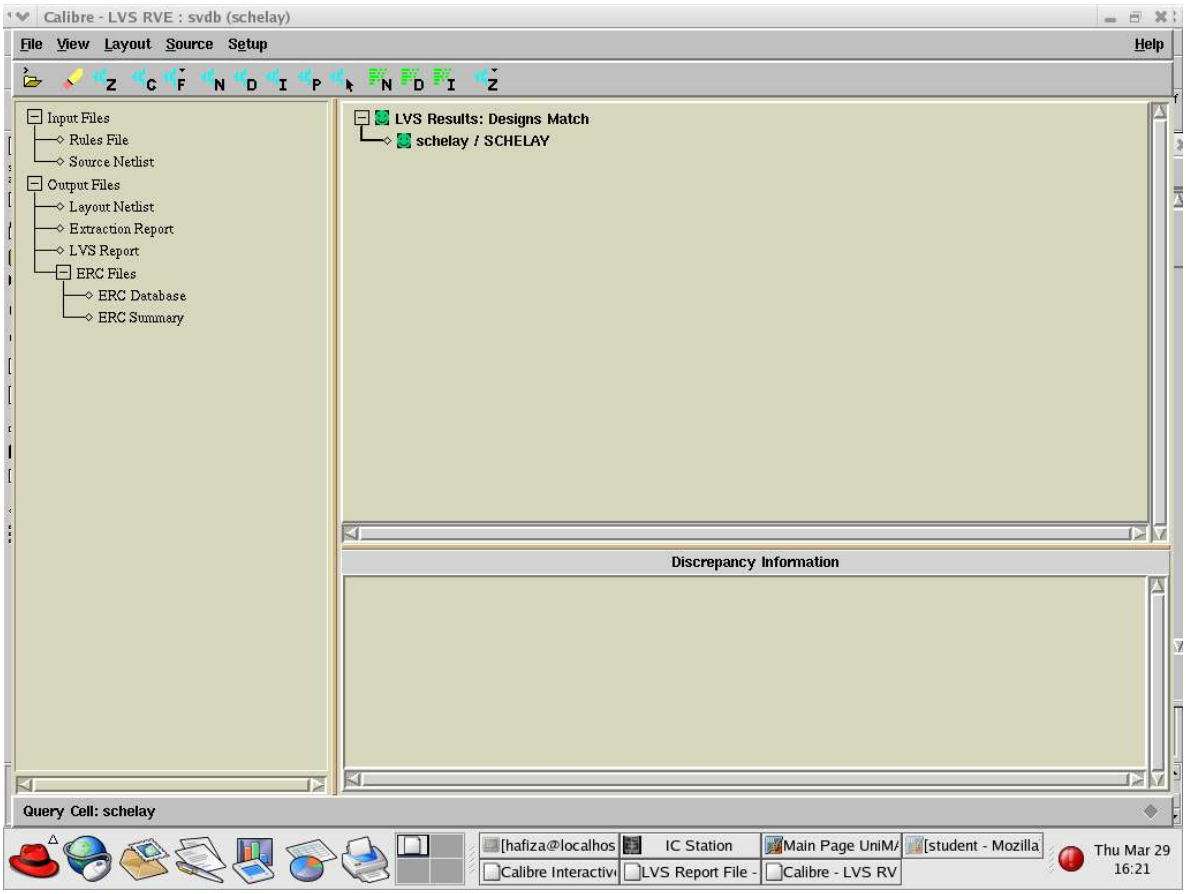

Figure 4.3: Layout meet the schematic and verification in LVS

4.2.5 Layout

After succeed via two simulation and calibration, the layout of this project has been produce. It consist of two metal layer that is metal1 and metal2.

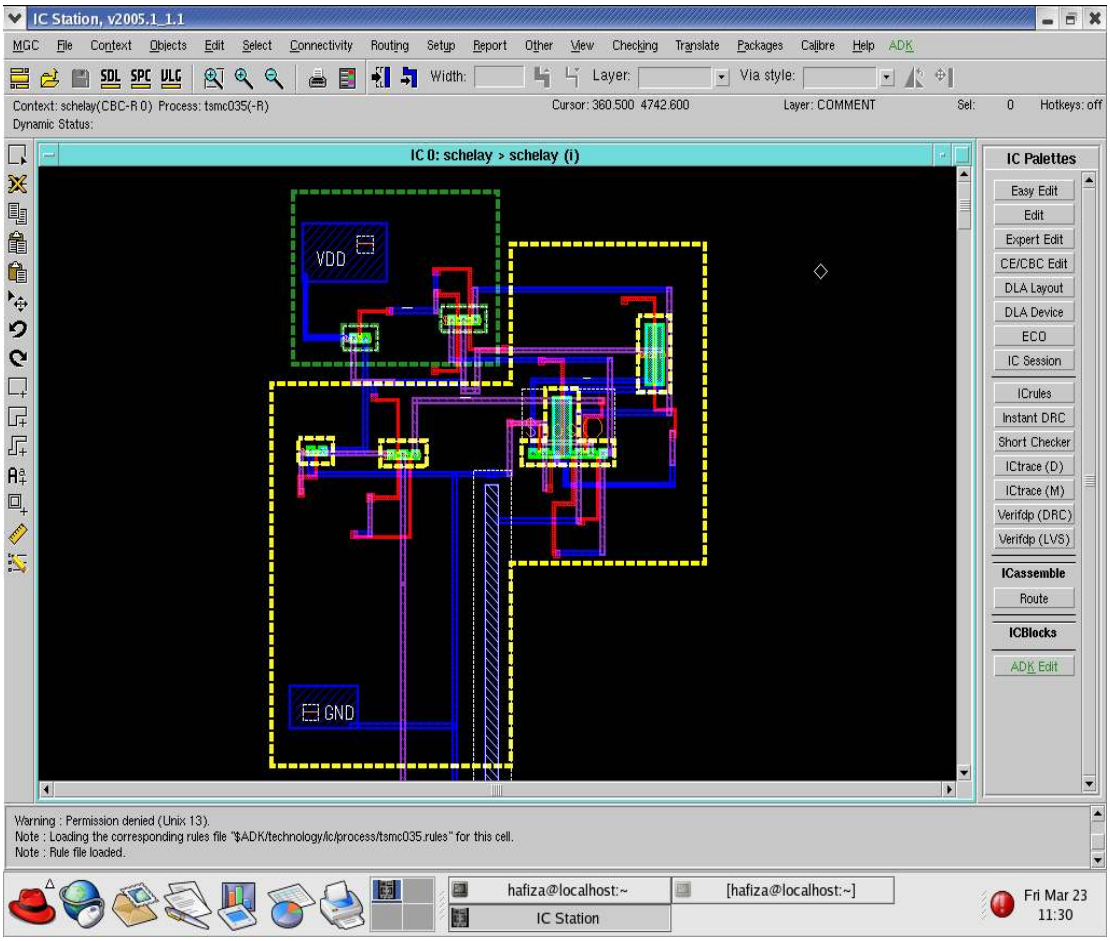

Figure 4.4: The layout design of Low Noise Amplifier