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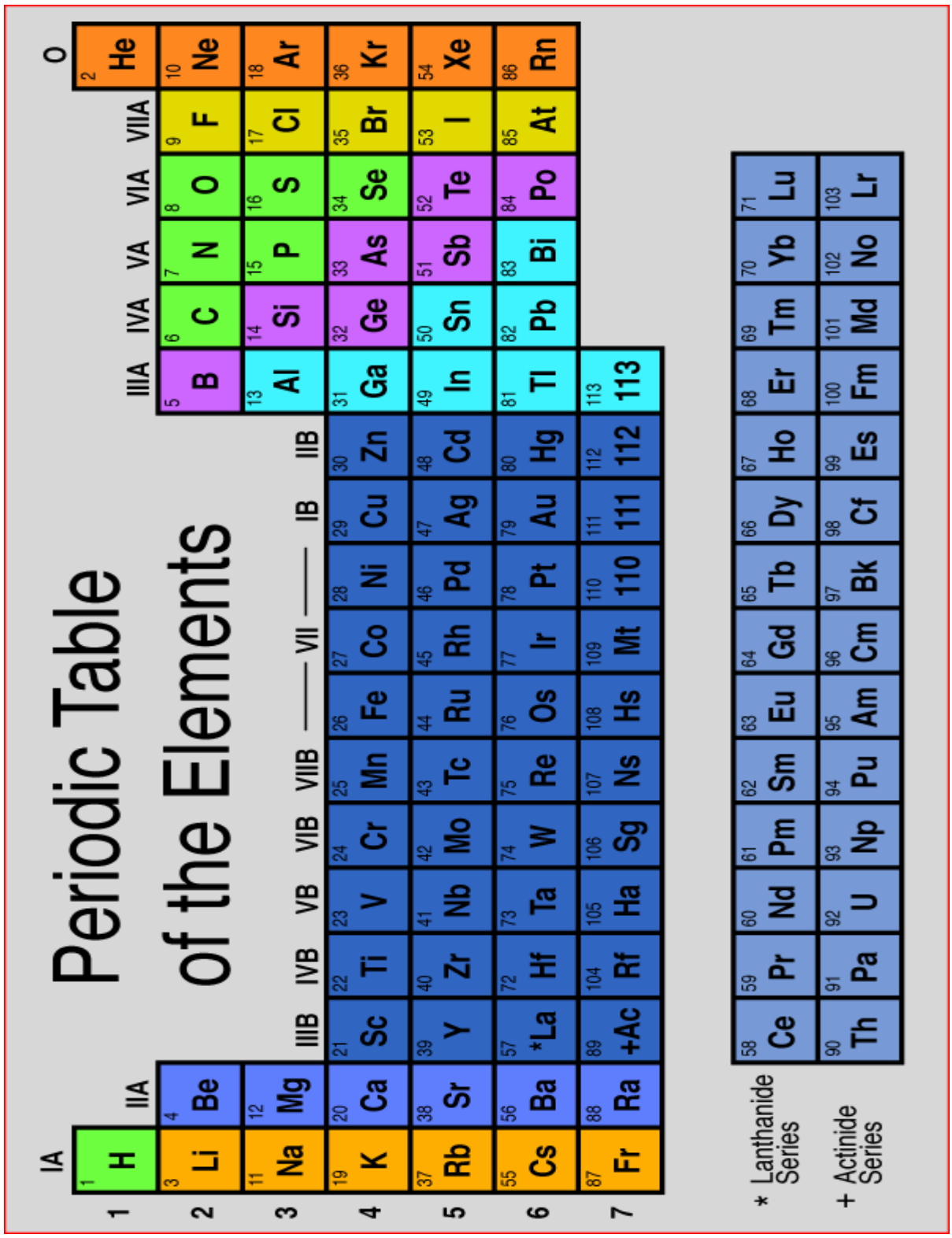
APPENDIX A

PERIODIC TABLE



APPENDIX B

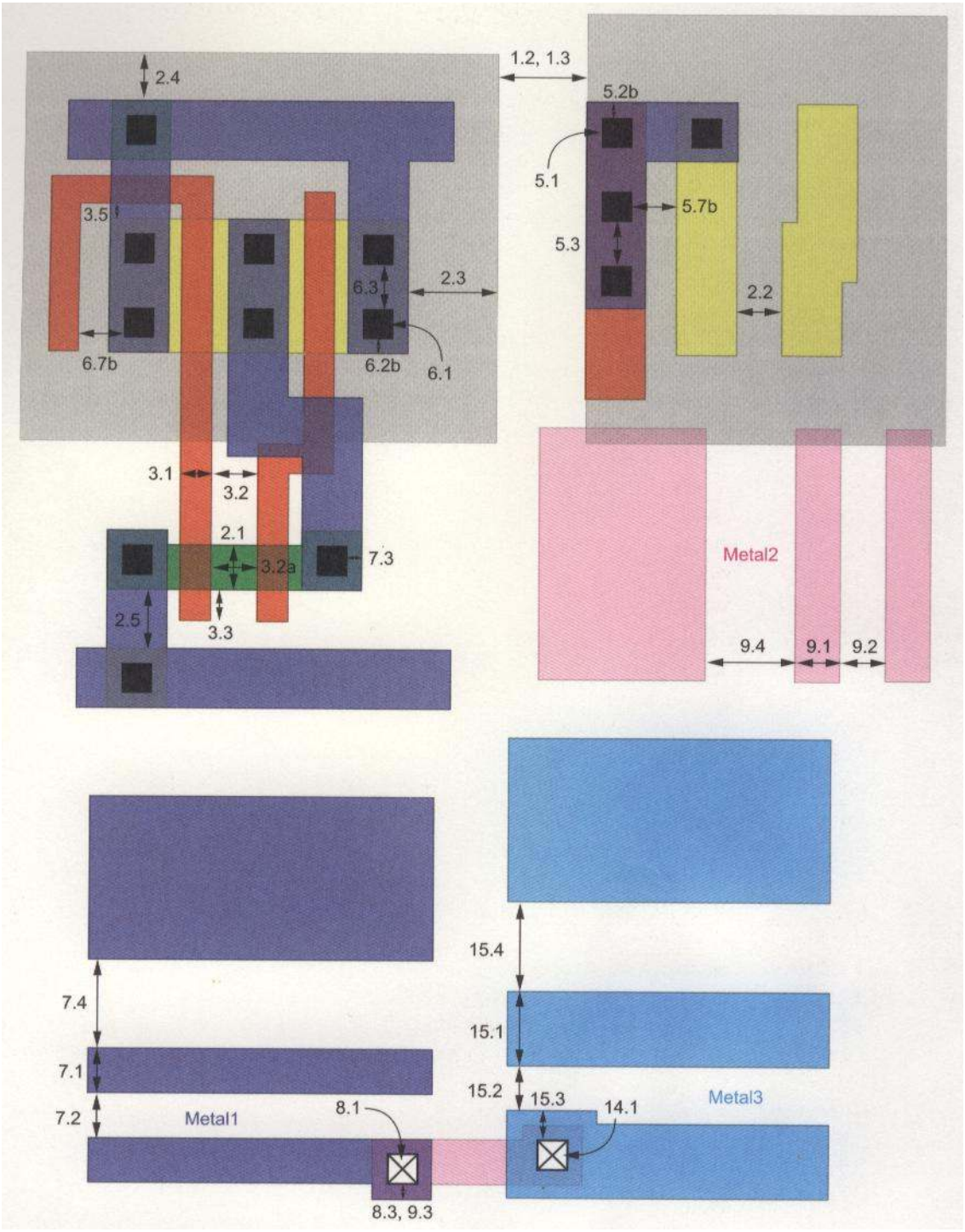


FIG 2.12 Illustrated MOSIS design rules

TABLE MOSIS DESIGN RULES (a)

Abbreviated MOSIS design rules					
Layer	**Rule**	**Description**	**SCMOS**	**SUBM**	**DEEP**
Well	1.1	Width	10	12	12
	1.2	Spacing to well at different potential	9	18	18
	1.3	Spacing to well at same potential	6	6	6
Active (diffusion)	2.1	Width	3	3	3
	2.2	Spacing to active	3	3	3
	2.3	Source/drain surround by well	5	6	6
	2.4	Substrate/well contact surround by well	3	3	3
	2.5	Spacing to active of opposite type	4	4	4
Poly	3.1	Width	2	2	2
	3.2	Spacing to poly over field oxide	2	3	3
	3.2a	Spacing to poly over active	2	3	4
	3.3	Gate extension beyond active	2	2	2.5
	3.4	Active extension beyond poly	3	3	4
	3.5	Spacing of poly to active	1	1	1
Select	4.1	Spacing from substrate/well contact to gate	3	3	3
	4.2	Overlap of active	2	2	2
	4.3	Overlap of substrate/well contact	1	1	1.5
	4.4	Spacing to select	2	2	4
Contact (to poly or active)	5.1, 6.1	Width (exact)	2x2	2x2	2x2
	5.2b, 6.2b	Overlap by poly or active	1	1	1
	5.3, 6.3	Spacing to contact	2	3	4
	5.4, 6.4	Spacing to gate	2	2	2
	5.5b	Spacing of poly contact to other poly	4	5	5
	5.7b, 6.7b	Spacing to active/poly for multiple poly/active contacts	3	3	3
	6.8b	Spacing of active contact to poly contact	4	4	4
Metal1	7.1	Width	3	3	3
	7.2	Spacing to metal1	2	3	3
	7.3, 8.3	Overlap of contact or via	1	1	1
	7.4	Spacing to metal for lines wider than 10 λ	4	6	6
Via1–Via(*N*-1)	8.1, 14.1, …	Width (exact)	2x2	2x2	3x3
	8.2, 14.2, …	Spacing to via on same layer	3	3	3
	8.4	Spacing to contacts (if no stacked vias)	2	2	n/a
	8.5	Spacing of via1 to poly or active edge	2	2	n/a
	14.4	Spacing of via2 to via1 (if no stacked vias)	2	2	n/a
Metal2–Metal(*N*-1)	9.1, …	Width	3	3	3
	9.2, …	Spacing to same layer metal	3	3	4
	9.3, …	Overlap of via	1	1	1
	9.4, …	Spacing to metal for lines wider than 10 λ	6	6	8
Metal3 (3-layer process)	15.1	Width	6	5	n/a
	15.2	Spacing to metal3	4	3	n/a
	15.3	Overlap of via2	2	2	n/a
	15.4	Spacing to metal for lines wider than 10 λ	8	6	n/a

TABLE MOSIS DESIGN RULES (b)

Layer	Rule	Description	90 nm rule (μm)
Well	1.1	Width	0.75
	1.2	Spacing to well at different potential	1.5
	1.3	Spacing to well at same potential	1.0
Active (diffusion)	2.1	Width	0.15
	2.2	Spacing to active	0.20
	2.3	Source/drain surround by well	0.25
	2.4	Substrate/well contact surround by well	0.25
	2.5	Spacing to active of opposite type	0.30
Poly	3.1	Width	0.09
	3.2	Spacing to poly over field oxide	0.15
	3.2a	Spacing to poly over active	0.15
	3.3	Gate extension beyond active	0.15
	3.4	Active extension beyond poly	0.15
	3.5	Spacing of poly to active	0.10
Select	4.1	Spacing from substrate/well contact to gate	0.25
	4.2	Overlap of active	0.20
	4.3	Overlap of substrate/well contact	0.10
	4.4	Spacing to select	0.30
Contact (to poly or active)	5.1, 6.1	Width (exact)	0.12
	5.2b, 6.2b	Overlap by poly or active	0.01
	5.3, 6.3	Spacing to contact	0.15
	5.4	Spacing to gate	0.10
Metal1	7.1	Width	0.13
	7.2	Spacing to well metal1	0.13
	7.3, 8.3	Overlap of contact or via	0.01
	7.4	Spacing to metal for lines wider than 0.5 μm	0.40
Via1–Via5	8.1, 14.1, …	Width (exact)	0.13
	8.2, 14.2, …	Spacing to via on same layer	0.13

Appendix C

LVS REPORT FILE

```
MGC_HOME = /EDA/ixl_cal_2004.3_9.21
$MGC_HOME/bin/calibre -spice schelay.lay.net -nowait
/home/hafiza/_tsmc035.rules_

//  Calibre v2004.3_9.21    Thu Sep 30 11:25:17 PDT 2004
//  Litho Libraries v2004.3_9.20  Wed Sep 29 14:30:13 PDT 2004
//
//                 Copyright Mentor Graphics Corporation 2004
//                               All Rights Reserved.
//         THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
//            WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
//              OR ITS LICENSORS AND IS SUBJECT TO LICENSE TERMS.
//
//  Mentor Graphics software executing under i386 Linux
//
//  Running on Linux localhost.localdomain 2.4.21-27.ELsmp #1 SMP Wed Dec
1 21:59:02 EST 2004 i686 glibc 2.3.2/linuxthreads-0.10 (2.4.19)
//
//  Starting time: Thu Mar 29 16:17:04 2007
//
//  Running on 1  CPU
//
//

--------------------------------------------------------------------------
-------
--------------------------------------------------------------------------
-------
-----          STANDARD VERIFICATION RULE FILE COMPILATION MODULE
-----
--------------------------------------------------------------------------
-------
--------------------------------------------------------------------------
-------

--- RULE FILE = /home/hafiza/_tsmc035.rules_

//
//  Rule file generated on Thu Mar 29 16:17:03 MYT 2007
//     by Calibre Interactive - LVS (v2004.3_9.21)
//
//      *** PLEASE DO NOT MODIFY THIS FILE ***
//
//

LAYOUT PATH "schelay.calibre.gds"
LAYOUT PRIMARY "schelay"
LAYOUT SYSTEM GDSII

MASK SVDB DIRECTORY "svdb" QUERY
```

```
LVS REPORT "schelay.lvs.report"

LVS REPORT MAXIMUM 50

LVS RECOGNIZE GATES ALL

LVS ABORT ON SOFTCHK NO
LVS ABORT ON SUPPLY ERROR YES
LVS IGNORE PORTS NO
LVS SHOW SEED PROMOTIONS NO
LVS SHOW SEED PROMOTIONS MAXIMUM 50

LVS ISOLATE SHORTS NO


VIRTUAL CONNECT COLON NO
VIRTUAL CONNECT REPORT NO
LVS EXECUTE ERC YES
ERC RESULTS DATABASE "schelay.erc.results"
ERC SUMMARY REPORT "schelay.erc.summary" REPLACE HIER
ERC MAXIMUM RESULTS 1000
ERC MAXIMUM VERTEX 4096

ERC SELECT CHECK
      "bad_active_area"
      "bad_contact_poly"
      "bad_contact_ELECTRODE"
      "bad_contact_active"
      "bad_contact_gate"
      "bad_via"
      "bad_via2"
      "bad_via3"
      "select_overlap"
      "bad_nwell"
      "bad_psubstrate"
      "bad_pgate"
      "bad_ngate"
      "bad_port"
      "DRC1_1"
      "DRC1_2"
      "DRC2_1"
      "DRC2_2"
      "DRC2_3"
      "DRC2_4"
      "DRC3_1"
      "DRC3_2"
      "DRC3_3"
      "DRC3_4"
      "DRC3_5"
      "DRC4.1p"
      "DRC4.1n"
      "DRC4.2"
      "DRC4.3p"
      "DRC4.3n"
      "DRC4.4pw"
      "DRC4.4ps"
```

```
      "DRC4.4nw"
      "DRC4.4ns"
      "DRC4.4np"
      "DRC5_1"
      "DRC5_2"
      "DRC5_3"
      "DRC5_4"
      "DRC6_1"
      "DRC6_2"
      "DRC6_3"
      "DRC6_4"
      "DRC7_1"
      "DRC7_2"
      "DRC7_3"
      "DRC7_4"
      "DRC8_1"
      "DRC8_2"
      "DRC8_3"
      "DRC9_1"
      "DRC9_2"
      "DRC9_3"
      "DRC9_4"
      "DRC11_1"
      "DRC11_2"
      "DRC11_3"
      "DRC11_4"
      "DRC11_5"
      "DRC11_sel"
      "DRC12_1"
      "DRC12_2"
      "DRC13_1"
      "DRC13_2"
      "DRC13_3"
      "DRC13_4"
      "DRC13_5"
      "DRC14_1"
      "DRC14_2"
      "DRC14_3"
      "DRC15_1"
      "DRC15_2"
      "DRC15_3"
      "DRC15_4"
      "DRC21_1"
      "DRC21_2"
      "DRC21_3"
      "DRC22_1"
      "DRC22_2"
      "DRC22_3"
      "DRC22_4"

#IFDEF $MGC_CALIBRE_INTERACTIVE
   DRC ICSTATION YES
#ENDIF


INCLUDE "/EDA/Mentor-training-ADK/technology/ic/process/tsmc035.rules"
```

```
--- STANDARD VERIFICATION RULE FILE COMPILATION MODULE COMPLETED.  CPU
TIME = 0  REAL TIME = 0

--- CALIBRE::HIERARCHICAL CIRCUIT EXTRACTOR - Thu Mar 29 16:17:04 2007

--------------------------------------------------------------------------
-------
--------------------------------------------------------------------------
-------
-----                    CALIBRE LAYOUT DATA INPUT MODULE
-----
--------------------------------------------------------------------------
-------
--------------------------------------------------------------------------
-------

--- LAYOUT SYSTEM = GDS

--------------------------------------------------------------------------
-------
-----                      GDS FILE SUMMARY INFORMATION
-----
--------------------------------------------------------------------------
-------

GDS FILENAME:        schelay.calibre.gds
GDS VERSION:         600
LIBRARY NAME:        mentor.db
LAST MODIFIED:       ON 2007/3/29 AT 16:17:4
LAST ACCESSED:       ON 2007/3/29 AT 16:17:4
DATABASE PRECISION:  0.001 user units per database unit
PHYSICAL PRECISION:  1e-09 meters per database unit

--------------------------------------------------------------------------
-------
-----                   GDS INPUT DATA FOR INDIVIDUAL CELLS
-----
--------------------------------------------------------------------------
-------
     CELL NAME                     PLACEMENTS   ARRAYS  POLYGONS   PATHS
TEXTS
--------------------------------------------------------------------------
-------
nwell_contact                               0        0          4        0
0
pwell_contact                               0        0          4        0
0
via2                                        0        0          3        0
0
via                                         0        0          3        0
0
schelay                                    42        0       1437       77
5
```

```
NOTE: UNUSED geometric data is present on the following layer/datatype
pairs:
    LAYER = 41 DATATYPE = 0

NOTE: The following required simple layers are EMPTY:
    2
    3
    4
    10
    25
    26
    30
    31
    34
    52
    111

--- LAYOUT DATABASE CONSTRUCTOR COMPLETED.  CPU TIME = 0  REAL TIME = 0
LVHEAP = 5/6/6

CONSTRUCTING HIERARCHICAL DATABASE
    COPYING LAYOUT DATABASE
    PROCESSING TEXT
    ELIMINATING EMPTY CELLS
    COMPUTING RECTANGULAR EXTENTS
    ELIMINATING DUPLICATE PLACEMENTS
    FLATTENING NON-ORTHOGONAL PLACEMENTS
    CLONING MAGNIFIED PLACEMENTS
    IDENTIFYING TOP LAYER CELLS
    IDENTIFYING VERY SMALL CELLS
        via
        pwell_contact
        via2
    CHECKING ACUTE/SKEW/OFFGRID
    TRANSFORMING VERY LARGE ARRAYS
    EXPANDING UNIQUE VERY SMALL CELL PLACEMENTS
        pwell_contact in schelay at (-30.95,4440.9)
    ELIMINATING DUPLICATE PLACEMENTS
    EXPANDING UNIQUE TOP LAYER CELL PLACEMENTS
    EXPANDING UNIQUE MONO-GEOMETRIC CELL PLACEMENTS
    COMPUTING RECTILINEAR EXTENTS
    EXPANDING UNIQUE TRANSPARENT CELL PLACEMENTS
        nwell_contact in schelay at (9.5,4754.95)
    ELIMINATING DUPLICATE PLACEMENTS
    EXPANDING UNIQUE LIGHT-WEIGHT CELL PLACEMENTS
    EXPANDING UNIQUE ROW CELL PLACEMENTS
    EXPANDING TRIVIAL CELL PLACEMENTS
    EXPANDING VERY SPARSE ARRAY PLACEMENTS
    EXPANDING VERY SPARSE CELL PLACEMENTS
    EXPANDING DENSE OVERLAPS
    EXPANDING UNIQUE META-CELL PLACEMENTS
    PUSHING VERY SMALL CELL PLACEMENTS
    PUSHING TOP LAYER CELL PLACEMENTS
    EXPANDING INJECTABLE ARRAY PLACEMENTS
    INJECTING HIERARCHY
    COMPUTING RECTANGULAR EXTENTS
    PUSHING VERY SMALL CELL PLACEMENTS
```

```
    PUSHING TOP LAYER CELL PLACEMENTS
    COMPUTING CELL-TO-WORLD TRANSFORMS
    SORTING PLACEMENT EXTENTS
    PACKING HIERARCHY
    PRE-MERGING LAYERS
        N_WELL
        POLY
        ACTIVE
        P_PLUS_SELECT
        N_PLUS_SELECT
        CONTACT_TO_ACTIVE
        ELECTRODE
        METAL1
        CONTACT_TO_POLY
        VIA
        METAL2
        CONTACT_TO_ELECTRODE
        VIA2
        METAL3
    COMPUTING PLACEMENT OVERLAP RECORDS
    COMPUTING CELL OVERLAP AREAS
    INTERSECTING PLACEMENTS AND OVERLAP AREAS
HIERARCHICAL DATABASE CONSTRUCTOR COMPLETE.
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8

-------------------------------------------------------------------------
-------
-----               TEXT OBJECTS FOR CONNECTIVITY EXTRACTION
-----
-------------------------------------------------------------------------
-------

GND (-14.4,4440.8) 2 schelay            VDD (-21.35,4746.5) 2 schelay

-------------------------------------------------------------------------
-------
-----                TEXT OBJECTS FOR WITH TEXT OPERATIONS
-----
-------------------------------------------------------------------------
-------


-------------------------------------------------------------------------
-------
-----               TEXT OBJECTS FOR EXPAND TEXT OPERATIONS
-----
-------------------------------------------------------------------------
-------


-------------------------------------------------------------------------
-------
-----                  TEXT OBJECTS FOR CAPI OPERATIONS
-----
-------------------------------------------------------------------------
-------
```

```
-------------------------------------------------------------------------------
-------
-----                                PORTS
-----
-------------------------------------------------------------------------------
-------

GND (-14.4,4440.8) 2 schelay           VDD (-21.35,4746.5) 2 schelay

-------------------------------------------------------------------------------
-------
-----             LAYER READ SUMMARY (SIMPLE LAYER GEOMETRIES)
-----
-------------------------------------------------------------------------------
-------
SIMPLE LAYER      GEOMETRIES
-------------------------------------------------------------------------------
-------

  2                     0
  3                     0
  4                     0
  10                    0
  25                    0
  26                    0
  30                    0
  31                    0
  34                    0
  42                    4
  43                   20
  44                    3
  45                    5
  46                   75
  47                   25
  48                   49
  49                   81
  50                    1
  51                   36
  52                    0
  55                 1216
  56                    4
  61                    1
  62                    2
  111                   0

-------------------------------------------------------------------------------
-------
-----            LAYER READ SUMMARY (ORIGINAL LAYER GEOMETRIES)
-----
-------------------------------------------------------------------------------
-------
ORIGINAL LAYER       INITIAL GEOMETRIES                FINAL GEOMETRIES
-------------------------------------------------------------------------------
-------

  N_WELL                  4 (4)                           1 (1)
```

POLY	75 (75)	15 (15)
ACTIVE	20 (20)	8 (8)
P_PLUS_SELEC	3 (3)	3 (3)
N_PLUS_SELEC	5 (5)	5 (5)
DIFFUSED_RES	0 (0)	0 (0)
CONTACT_TO_A	49 (49)	49 (49)
HI_RES_IMPLA	0 (0)	0 (0)
ELECTRODE	4 (4)	2 (2)
METAL1	81 (117)	42 (78)
CONTACT_TO_P	25 (25)	25 (25)
CONTACT	0 (0)	0 (0)
PADS	0 (0)	0 (0)
VIA	1 (37)	1 (37)
METAL2	36 (74)	18 (56)
CONTACT_TO_E	1216 (1216)	1216 (1216)
VIA2	1 (3)	1 (3)
METAL3	2 (4)	2 (4)
VIA3	0 (0)	0 (0)
METAL4	0 (0)	0 (0)
METAL1.PORT	0 (0)	0 (0)
METAL2.PORT	0 (0)	0 (0)
METAL3.PORT	0 (0)	0 (0)
OVERGLASS	0 (0)	0 (0)
METAL4.PORT	0 (0)	0 (0)

----- LAYER READ SUMMARY (TEXT FOR CONNECTIVITY EXTRACTION)

LAYER	TEXTS	LAYER	TEXTS
2	2 (2)		

----- LAYER READ SUMMARY (TEXT FOR WITH TEXT OPERATIONS)

LAYER	TEXTS	LAYER	TEXTS

----- LAYER READ SUMMARY (TEXT FOR EXPAND TEXT OPERATIONS)

```
LAYER               TEXTS                                LAYER
TEXTS
-------------------------------------------------------------------------
-------


-------------------------------------------------------------------------
-------
-----            LAYER READ SUMMARY (TEXT FOR CAPI OPERATIONS)
-----
-------------------------------------------------------------------------
-------
LAYER               TEXTS                                LAYER
TEXTS
-------------------------------------------------------------------------
-------


-------------------------------------------------------------------------
-------
-----                       LAYER READ SUMMARY (PORTS)
-----
-------------------------------------------------------------------------
-------
LAYER               PORTS                                LAYER
PORTS
-------------------------------------------------------------------------
-------

2                   2 (2)

-------------------------------------------------------------------------
-------
-----                       CELL AND PLACEMENT SUMMARY
-----
-------------------------------------------------------------------------
-------
CELL TYPE                 CELLS           PLACEMENTS       FLAT
PLACEMENTS
-------------------------------------------------------------------------
-------

USER                          3                40                    40
 VERY SMALL                   2                40                    40
 TOP LAYER                    0                 0                     0
  VERY SMALL                  0                 0                     0
PSEUDO                        0                 0                     0
TOTAL                         3                40                    40

-------------------------------------------------------------------------
-------
-----                    LAYOUT DATA INPUT MODULE SUMMARY
-----
-------------------------------------------------------------------------
-------

--- TOTAL GEOMETRIES READ FROM SIMPLE LAYERS = 1522
```

```
--- TOTAL GEOMETRIES READ FROM ORIGINAL LAYERS = 1522 (1636)
--- TOTAL GEOMETRIES WRITTEN TO ORIGINAL LAYERS = 1388 (1502)
--- LVHEAP = 5/7/8
--- DATABASE EXTENT = [ -41.8 , 9.8 ] -> [ 251.25 , 4796.05 ]
--- GEOMETRIC DEPTH = ALL
--- TEXT DEPTH FOR CONNECTIVITY EXTRACTION = PRIMARY
--- TOTAL TEXT OBJECTS FOR CONNECTIVITY EXTRACTION = 2 (2)
--- TOTAL TEXT OBJECTS FOR WITH TEXT OPERATIONS = 0 (0)
--- TOTAL TEXT OBJECTS FOR EXPAND TEXT OPERATIONS = 0 (0)
--- TOTAL TEXT OBJECTS FOR CAPI OPERATIONS = 0 (0)
--- TOTAL PORT OBJECTS = 2 (2)
--- GEOMETRY FLAGGING = ACUTE (NO)  SKEW (NO)  OFFGRID (NO)
                        NONSIMPLE POLYGON (NO)  NONSIMPLE PATH (NO)
--- PRIMARY CELL = schelay
--- EXCLUDED CELLS =

--- CALIBRE LAYOUT DATA INPUT MODULE COMPLETED.  CPU TIME = 0  REAL TIME
= 0

--------------------------------------------------------------------------
-------
--------------------------------------------------------------------------
-------
-----      CALIBRE::HIERARCHICAL CIRCUIT EXTRACTOR - EXECUTIVE MODULE
-----
--------------------------------------------------------------------------
-------
--------------------------------------------------------------------------
-------

VIA3 = OR VIA3
--------------
VIA3 (HIER TYP=1 CFG=3 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 1 OF 176

Original Layer VIA3 DELETED -- LVHEAP = 5/7/8

METAL3 = OR METAL3
-------------------
METAL3 (HIER TYP=1 CFG=3 HGC=2 FGC=4 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 2 OF 176

Original Layer METAL3 DELETED -- LVHEAP = 5/7/8

METAL4 = OR METAL4
-------------------
METAL4 (HIER TYP=1 CFG=3 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 3 OF 176

Original Layer METAL4 DELETED -- LVHEAP = 5/7/8

VIA2 = OR VIA2
--------------
VIA2 (HIER TYP=1 CFG=3 HGC=1 FGC=3 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 4 OF 176

Original Layer VIA2 DELETED -- LVHEAP = 5/7/8
```

```
METAL2 = OR METAL2
------------------
METAL2 (HIER TYP=1 CFG=3 HGC=18 FGC=56 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 5 OF 176

Original Layer METAL2 DELETED -- LVHEAP = 5/7/8

VIA = OR VIA
------------
VIA (HIER TYP=1 CFG=3 HGC=1 FGC=37 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 6 OF 176

Original Layer VIA DELETED -- LVHEAP = 5/7/8

METAL1 = OR METAL1
------------------
METAL1 (HIER TYP=1 CFG=3 HGC=42 FGC=78 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 7 OF 176

Original Layer METAL1 DELETED -- LVHEAP = 5/7/8

CONTACT_TO_POLY = OR CONTACT_TO_POLY
------------------------------------
CONTACT_TO_POLY (HIER TYP=1 CFG=3 HGC=25 FGC=25 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 8 OF 176

Original Layer CONTACT_TO_POLY DELETED -- LVHEAP = 5/7/8

POLY = OR POLY
--------------
POLY (HIER TYP=1 CFG=3 HGC=15 FGC=15 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 9 OF 176

Original Layer POLY DELETED -- LVHEAP = 5/7/8

CONTACT = OR CONTACT
--------------------
CONTACT (HIER TYP=1 CFG=3 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 10 OF 176

Original Layer CONTACT DELETED -- LVHEAP = 5/7/8

METAL4.PORT = OR METAL4.PORT
----------------------------
METAL4.PORT (HIER TYP=1 CFG=3 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 11 OF 176

Original Layer METAL4.PORT DELETED -- LVHEAP = 5/7/8

METAL3.PORT = OR METAL3.PORT
----------------------------
METAL3.PORT (HIER TYP=1 CFG=3 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 12 OF 176

Original Layer METAL3.PORT DELETED -- LVHEAP = 5/7/8
```

```
METAL2.PORT = OR METAL2.PORT
----------------------------
METAL2.PORT (HIER TYP=1 CFG=3 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 13 OF 176

Original Layer METAL2.PORT DELETED -- LVHEAP = 5/7/8

METAL1.PORT = OR METAL1.PORT
----------------------------
METAL1.PORT (HIER TYP=1 CFG=3 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 14 OF 176

Original Layer METAL1.PORT DELETED -- LVHEAP = 5/7/8

CONTACT_TO_ELECTRODE = OR CONTACT_TO_ELECTRODE
----------------------------------------------
CONTACT_TO_ELECTRODE (HIER TYP=1 CFG=3 HGC=1216 FGC=1216 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 15 OF 176

Original Layer CONTACT_TO_ELECTRODE DELETED -- LVHEAP = 5/7/8

ELECTRODE = OR ELECTRODE
------------------------
ELECTRODE (HIER TYP=1 CFG=1 HGC=2 FGC=2 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 16 OF 176

Original Layer ELECTRODE DELETED -- LVHEAP = 5/7/8

HI_RES_IMPLANT = OR HI_RES_IMPLANT
----------------------------------
HI_RES_IMPLANT (HIER TYP=1 CFG=0 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 17 OF 176

Original Layer HI_RES_IMPLANT DELETED -- LVHEAP = 5/7/8

HR_pin = ELECTRODE NOT HI_RES_IMPLANT
-------------------------------------
HR_pin (HIER TYP=1 CFG=3 HGC=2 FGC=2 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 18 OF 176

CAP_pin = METAL1 AND ELECTRODE
------------------------------
CAP_pin (HIER TYP=1 CFG=3 HGC=2 FGC=2 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 19 OF 176

P_PLUS_SELECT = OR P_PLUS_SELECT
--------------------------------
P_PLUS_SELECT (HIER TYP=1 CFG=3 HGC=3 FGC=3 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 20 OF 176

Original Layer P_PLUS_SELECT DELETED -- LVHEAP = 5/7/8

pres = POLY AND P_PLUS_SELECT
-----------------------------
pres (HIER TYP=1 CFG=3 HGC=3 FGC=3 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 21 OF 176
```

```
N_PLUS_SELECT = OR N_PLUS_SELECT
--------------------------------
N_PLUS_SELECT (HIER TYP=1 CFG=3 HGC=5 FGC=5 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 22 OF 176

Original Layer N_PLUS_SELECT DELETED -- LVHEAP = 5/7/8

respin = POLY AND N_PLUS_SELECT
-------------------------------
respin (HIER TYP=1 CFG=3 HGC=10 FGC=10 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 23 OF 176

CONTACT_TO_ACTIVE = OR CONTACT_TO_ACTIVE
----------------------------------------
CONTACT_TO_ACTIVE (HIER TYP=1 CFG=3 HGC=49 FGC=49 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 24 OF 176

Original Layer CONTACT_TO_ACTIVE DELETED -- LVHEAP = 5/7/8

ACTIVE = OR ACTIVE
------------------
ACTIVE (HIER TYP=1 CFG=1 HGC=8 FGC=8 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 25 OF 176

Original Layer ACTIVE DELETED -- LVHEAP = 5/7/8

DIFF = ACTIVE NOT POLY
----------------------
DIFF (HIER TYP=1 CFG=0 HGC=21 FGC=21 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 26 OF 176

NDIFF = DIFF AND N_PLUS_SELECT
------------------------------
NDIFF (HIER TYP=1 CFG=1 HGC=15 FGC=15 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 27 OF 176

nsdt = NDIFF NOT POLY
---------------------
nsdt (HIER TYP=1 CFG=0 HGC=15 FGC=15 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 28 OF 176

DIFFUSED_RESISTOR = OR DIFFUSED_RESISTOR
----------------------------------------
DIFFUSED_RESISTOR (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 29 OF 176

Original Layer DIFFUSED_RESISTOR DELETED -- LVHEAP = 5/7/8

dfcnt = CONTACT_TO_ACTIVE INSIDE DIFFUSED_RESISTOR
--------------------------------------------------
dfcnt (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 30 OF 176

dfcnto = SIZE dfcnt BY 2
------------------------
dfcnto (HIER TYP=1 CFG=0 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 31 OF 176
```

```
Layer dfcnt DELETED -- LVHEAP = 5/7/8

dfrs = DIFFUSED_RESISTOR NOT dfcnto
-----------------------------------
dfrs (HIER TYP=1 CFG=0 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 32 OF 176

Layer DIFFUSED_RESISTOR DELETED -- LVHEAP = 5/7/8

Layer dfcnto DELETED -- LVHEAP = 5/7/8

NSRCDRN = nsdt NOT dfrs
-----------------------
NSRCDRN (HIER TYP=1 CFG=3 HGC=15 FGC=15 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 33 OF 176

Layer nsdt DELETED -- LVHEAP = 5/7/8

PDIFF = DIFF AND P_PLUS_SELECT
------------------------------
PDIFF (HIER TYP=1 CFG=1 HGC=6 FGC=6 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 34 OF 176

Layer DIFF DELETED -- LVHEAP = 5/7/8

psdt = PDIFF NOT POLY
---------------------
psdt (HIER TYP=1 CFG=0 HGC=6 FGC=6 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 35 OF 176

PSRCDRN = psdt NOT dfrs
-----------------------
PSRCDRN (HIER TYP=1 CFG=3 HGC=6 FGC=6 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 36 OF 176

Layer psdt DELETED -- LVHEAP = 5/7/8

Layer dfrs DELETED -- LVHEAP = 5/7/8

DRC_0 = EXTENT
--------------
DRC_0 (HIER-LSL TYP=1 CFG=1 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 37 OF 176

BULK = SIZE DRC_0 BY 1
----------------------
BULK (HIER-LSL TYP=1 CFG=0 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 38 OF 176

Layer DRC_0 DELETED -- LVHEAP = 5/7/8

N_WELL = OR N_WELL
------------------
N_WELL (HIER TYP=1 CFG=3 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 39 OF 176
```

```
Original Layer N_WELL DELETED -- LVHEAP = 5/7/8

PSUB = BULK NOT N_WELL
----------------------
PSUB (HIER TYP=1 CFG=3 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 40 OF 176

Layer BULK DELETED -- LVHEAP = 5/7/8

CONNECTIVITY EXTRACTION TOTAL LAYER PREPARATION TIME:  CPU TIME = 0  REAL
TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6

CONNECTIVITY EXTRACTION
-----------------------
NC = Net Count  IPC = Internal Pin Count
CEC = Cell Edge Count  PEC = Promoted Edge Count
LVHEAP = Geometry heap memory allocation.
MALLOC = Total heap memory allocation.

CELL via
     via (NC=1 IPC=0 CEC=6 PEC=0 CFGC=3)
     via  CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
CELL via2
     via2 (NC=1 IPC=0 CEC=6 PEC=0 CFGC=3)
     via2  CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
CELL schelay
     schelay (NC=32 IPC=40 CEC=2994 PEC=160 CFGC=1531)
     schelay  CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
TOTAL CEC=3006 PEC=160

POST-PROCESSING CONNECTIVITY DATA STRUCTURE...
    MARKING TRUE NETS AND EXTERNAL PINS...
        CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
    DISCARDING FALSE VIRTUAL NETS, RESOLVING DEEP SHORTS AND PERFORMING
VIRTUAL CONNECTIONS...
        CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
    CREATING COMPACT PIN DATA STRUCTURE...
        CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
    RESOLVING SHORT CIRCUIT TEXT...
        CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
    PROCESSING HIGH SHORTS...
        CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
    COMPUTING FINAL NET NAMES AND REPORTING TEXT WARNINGS...
        CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  MALLOC = 6/6/6
POST-PROCESSING completed.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8
MALLOC = 6/6/6

CONNECTIVITY EXTRACTION completed.  CPU TIME = 0  REAL TIME = 0  LVHEAP =
5/7/8  MALLOC = 6/6/6

WRITING CELL INFORMATION to PHDB svdb
PHDB CELL DATA WRITE completed.  CPU TIME = 0  REAL TIME = 0  LVHEAP =
5/7/8  MALLOC = 6/6/6

WRITING CONNECT INFORMATION to PHDB svdb
PHDB CONNECT INFORMATION written. CPU TIME = 0  REAL TIME = 0  LVHEAP =
5/7/8  MALLOC = 6/6/6
```

```
Layer METAL4.PORT DELETED -- LVHEAP = 5/7/8

Layer pres DELETED -- LVHEAP = 5/7/8

Layer respin DELETED -- LVHEAP = 5/7/8

DEVICE RECOGNITION
----------------------
LVS PUSH DEVICES enabled.

GATES = POLY AND ACTIVE
----------------------
GATES (HIER TYP=1 CFG=1 HGC=13 FGC=13 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 41 OF 176

NGATE = GATES AND N_PLUS_SELECT
------------------------------
NGATE (HIER TYP=1 CFG=1 HGC=10 FGC=10 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 42 OF 176

PGATE = GATES AND P_PLUS_SELECT
------------------------------
PGATE (HIER TYP=1 CFG=1 HGC=3 FGC=3 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 43 OF 176

HR = ELECTRODE AND HI_RES_IMPLANT
---------------------------------
HR (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 44 OF 176

Layer HI_RES_IMPLANT DELETED -- LVHEAP = 5/7/8

CAP = POLY AND ELECTRODE
------------------------
CAP (HIER TYP=1 CFG=1 HGC=2 FGC=2 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 45 OF 176

DEVICE RECOGNITION TOTAL LAYER PREPARATION TIME:  CPU TIME = 0  REAL TIME
= 0  LVHEAP = 5/7/8

DEVICE RECOGNITION TOTAL PRECISE INTERACTION TIME:  CPU TIME = 0  REAL
TIME = 0  LVHEAP = 5/7/8
TENTATIVE SEED PROMOTIONS:   seed layer  seeds  cell : layers touched
TENTATIVE SEED PROMOTIONS: ------------  -----  -------------------------
----------------
SEED PROMOTIONS:
SEED PROMOTIONS:
============================================================
SEED PROMOTIONS:
SEED PROMOTIONS:   seed layer  seeds  cell : layers touched
SEED PROMOTIONS: ------------  -----  ---------------------------------
------
SEED PROMOTIONS:
SEED PROMOTIONS:       TOTAL:      0
```

```
DEVICE RECOGNITION completed.  CPU TIME = 0  REAL TIME = 0  LVHEAP =
5/7/8  MALLOC = 6/6/6

WRITING DEVICE INFORMATION to PHDB svdb
PHDB DEVICE INFORMATION written. CPU TIME = 0  REAL TIME = 0  LVHEAP =
5/7/8  MALLOC = 6/6/6

Layer CAP_pin DELETED -- LVHEAP = 5/7/8

Layer HR DELETED -- LVHEAP = 5/7/8

Layer HR_pin DELETED -- LVHEAP = 5/7/8


HIERARCHICAL SPICE NETLISTER
----------------------------
HIERARCHICAL SPICE NETLISTER completed.  CPU TIME = 0  REAL TIME = 0
LVHEAP = 5/7/8  MALLOC = 6/6/6

CALIBRE HIERARCHICAL ERC
----------------------------

bad_active_area::x = ACTIVE NOT P_PLUS_SELECT
-----------------------------------------------
bad_active_area::x (HIER TYP=1 CFG=0 HGC=5 FGC=5 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 46 OF 176

bad_active_area::<1> = bad_active_area::x NOT N_PLUS_SELECT
-------------------------------------------------------------
bad_active_area::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 47 OF 176

Layer bad_active_area::x DELETED -- LVHEAP = 5/7/8

Layer bad_active_area::<1> DELETED -- LVHEAP = 5/7/8

bad_contact_poly::<1> = CONTACT_TO_POLY NOT INSIDE POLY
-------------------------------------------------------
bad_contact_poly::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 48 OF 176

Layer bad_contact_poly::<1> DELETED -- LVHEAP = 5/7/8

bad_contact_poly::<2> = CONTACT_TO_POLY NOT INSIDE METAL1
---------------------------------------------------------
bad_contact_poly::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 49 OF 176

Layer bad_contact_poly::<2> DELETED -- LVHEAP = 5/7/8

bad_contact_ELECTRODE::<1> = CONTACT_TO_ELECTRODE NOT INSIDE ELECTRODE
----------------------------------------------------------------------
bad_contact_ELECTRODE::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 50 OF 176

Layer bad_contact_ELECTRODE::<1> DELETED -- LVHEAP = 5/7/8
```

```
bad_contact_ELECTRODE::<2> = CONTACT_TO_ELECTRODE NOT INSIDE METAL1
-------------------------------------------------------------------
bad_contact_ELECTRODE::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 51 OF 176

Layer bad_contact_ELECTRODE::<2> DELETED -- LVHEAP = 5/7/8

bad_contact_active::<1> = CONTACT_TO_ACTIVE NOT INSIDE ACTIVE
-------------------------------------------------------------
bad_contact_active::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 52 OF 176

Layer bad_contact_active::<1> DELETED -- LVHEAP = 5/7/8

bad_contact_active::<2> = CONTACT_TO_ACTIVE NOT INSIDE METAL1
-------------------------------------------------------------
bad_contact_active::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 53 OF 176

Layer bad_contact_active::<2> DELETED -- LVHEAP = 5/7/8

bad_contact_gate::<1> = CONTACT_TO_POLY AND ACTIVE
--------------------------------------------------
bad_contact_gate::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 54 OF 176

Layer bad_contact_gate::<1> DELETED -- LVHEAP = 5/7/8

bad_via::<1> = VIA NOT INSIDE METAL1
------------------------------------
bad_via::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 55 OF 176

Layer bad_via::<1> DELETED -- LVHEAP = 5/7/8

bad_via::<2> = VIA NOT INSIDE METAL2
------------------------------------
bad_via::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 56 OF 176

Layer bad_via::<2> DELETED -- LVHEAP = 5/7/8

bad_via2::<1> = VIA2 NOT INSIDE METAL2
--------------------------------------
bad_via2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 57 OF 176

Layer bad_via2::<1> DELETED -- LVHEAP = 5/7/8

bad_via2::<2> = VIA2 NOT INSIDE METAL3
--------------------------------------
bad_via2::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 58 OF 176

Layer bad_via2::<2> DELETED -- LVHEAP = 5/7/8

bad_via3::<1> = VIA3 NOT INSIDE METAL3
```

```
-------------------------------------
bad_via3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 59 OF 176

Layer bad_via3::<1> DELETED -- LVHEAP = 5/7/8

bad_via3::<2> = VIA3 NOT INSIDE METAL4
-------------------------------------
bad_via3::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 60 OF 176

Layer bad_via3::<2> DELETED -- LVHEAP = 5/7/8

select_overlap::<1> = P_PLUS_SELECT AND N_PLUS_SELECT
-----------------------------------------------------
select_overlap::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 61 OF 176

Layer select_overlap::<1> DELETED -- LVHEAP = 5/7/8

ACT_CONTACT = CONTACT_TO_ACTIVE OR CONTACT
------------------------------------------
ACT_CONTACT (HIER TYP=1 CFG=0 HGC=49 FGC=49 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 62 OF 176

Layer CONTACT DELETED -- LVHEAP = 5/7/8

NWTIE = NDIFF AND N_WELL
------------------------
NWTIE (HIER TYP=1 CFG=0 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 63 OF 176

bad_nwell::x = ACT_CONTACT AND NWTIE
------------------------------------
bad_nwell::x (HIER TYP=1 CFG=1 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 64 OF 176

Layer NWTIE DELETED -- LVHEAP = 5/7/8

bad_nwell::<1> = N_WELL NOT ENCLOSE bad_nwell::x
------------------------------------------------
bad_nwell::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 65 OF 176

Layer bad_nwell::x DELETED -- LVHEAP = 5/7/8

Layer bad_nwell::<1> DELETED -- LVHEAP = 5/7/8

PSUBTIE = PDIFF AND PSUB
------------------------
PSUBTIE (HIER TYP=1 CFG=0 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 66 OF 176

bad_psubstrate::x = ACT_CONTACT AND PSUBTIE
-------------------------------------------
bad_psubstrate::x (HIER TYP=1 CFG=1 HGC=1 FGC=1 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 67 OF 176
```

```
Layer ACT_CONTACT DELETED -- LVHEAP = 5/7/8

Layer PSUBTIE DELETED -- LVHEAP = 5/7/8

bad_psubstrate::<1> = PSUB NOT ENCLOSE bad_psubstrate::x
-------------------------------------------------------
bad_psubstrate::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 68 OF 176

Layer bad_psubstrate::x DELETED -- LVHEAP = 5/7/8

Layer bad_psubstrate::<1> DELETED -- LVHEAP = 5/7/8

bad_pgate::<1> = PGATE AND PSUB
-------------------------------
bad_pgate::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 69 OF 176

Layer PSUB DELETED -- LVHEAP = 5/7/8

Layer bad_pgate::<1> DELETED -- LVHEAP = 5/7/8

bad_ngate::<1> = NGATE AND N_WELL
---------------------------------
bad_ngate::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 70 OF 176

Layer bad_ngate::<1> DELETED -- LVHEAP = 5/7/8

bad_port::<1> = METAL1.PORT NOT INSIDE METAL1
---------------------------------------------
bad_port::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 71 OF 176

Layer METAL1.PORT DELETED -- LVHEAP = 5/7/8

Layer bad_port::<1> DELETED -- LVHEAP = 5/7/8

bad_port::<2> = METAL2.PORT NOT INSIDE METAL2
---------------------------------------------
bad_port::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 72 OF 176

Layer METAL2.PORT DELETED -- LVHEAP = 5/7/8

Layer bad_port::<2> DELETED -- LVHEAP = 5/7/8

bad_port::<3> = METAL3.PORT NOT INSIDE METAL3
---------------------------------------------
bad_port::<3> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 73 OF 176

Layer METAL3.PORT DELETED -- LVHEAP = 5/7/8

Layer bad_port::<3> DELETED -- LVHEAP = 5/7/8
```

```
DRC1_2::<1> = EXT N_WELL < 18 REGION SQUARE NOT CONNECTED SINGULAR
DRC1_1::<1> = INT N_WELL < 12 REGION SQUARE SINGULAR
-------------------------------------------------------------
DRC1_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC1_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 75 OF 176

Layer DRC1_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC1_2::<1> DELETED -- LVHEAP = 5/7/8

DRC2_2::<1> = EXT ACTIVE < 3 REGION SQUARE
DRC2_1::<1> = INT ACTIVE < 3 REGION SQUARE
-----------------------------------------
DRC2_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC2_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 77 OF 176

Layer DRC2_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC2_2::<1> DELETED -- LVHEAP = 5/7/8

DRC2_3::<1> = EXT N_WELL NDIFF < 6 REGION SQUARE SINGULAR
DRC2_4::<1> = ENC NDIFF N_WELL < 3 REGION ABUT == 0 OVERLAP SINGULAR
-----------------------------------------------------------------
DRC2_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC2_4::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 79 OF 176

Layer NDIFF DELETED -- LVHEAP = 5/7/8

Layer DRC2_3::<1> DELETED -- LVHEAP = 5/7/8

DRC2_4::<2> = EXT PDIFF N_WELL < 3 REGION SINGULAR
DRC2_3::<2> = ENC PDIFF N_WELL < 6 REGION SQUARE ABUT == 0 OVERLAP
SINGULAR
-------------------------------------------------------------------------
--
DRC2_4::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC2_3::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 81 OF 176

Layer PDIFF DELETED -- LVHEAP = 5/7/8

Layer DRC2_3::<2> DELETED -- LVHEAP = 5/7/8

Layer DRC2_4::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC2_4::<2> DELETED -- LVHEAP = 5/7/8

DRC3_2::<1> = EXT POLY < 3 SINGULAR
DRC3_1::<1> = INT POLY < 2 SINGULAR
-----------------------------------
DRC3_2::<1> (HIER TYP=3 HGC=0 FGC=0)
DRC3_1::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 83 OF 176
```

```
Layer DRC3_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC3_2::<1> DELETED -- LVHEAP = 5/7/8

DRC3_3::<1> = PGATE TOUCH PSRCDRN == 1
-------------------------------------
DRC3_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 84 OF 176

Layer PGATE DELETED -- LVHEAP = 5/7/8

Layer DRC3_3::<1> DELETED -- LVHEAP = 5/7/8

DRC3_3::<2> = NGATE TOUCH NSRCDRN == 1
-------------------------------------
DRC3_3::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 85 OF 176

Layer NGATE DELETED -- LVHEAP = 5/7/8

Layer DRC3_3::<2> DELETED -- LVHEAP = 5/7/8

DRC3_5::<1> = EXT ACTIVE POLY < 1 REGION SQUARE ABUT == 0
DRC3_3::<3> = ENC ACTIVE POLY < 2 REGION SQUARE ABUT == 0
DRC3_4::<1> = ENC POLY ACTIVE < 3 REGION SQUARE ABUT == 0
-------------------------------------------------------
DRC3_5::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC3_3::<3> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC3_4::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 88 OF 176

Layer DRC3_3::<3> DELETED -- LVHEAP = 5/7/8

Layer DRC3_4::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC3_5::<1> DELETED -- LVHEAP = 5/7/8

DRC4.1p::nxtor = NSRCDRN OR GATES
---------------------------------
DRC4.1p::nxtor (HIER TYP=1 CFG=1 HGC=8 FGC=8 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 89 OF 176

Layer NSRCDRN DELETED -- LVHEAP = 5/7/8

DRC4.1p::<1> = ENC GATES DRC4.1p::nxtor < 3
-------------------------------------------
DRC4.1p::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 90 OF 176

Layer DRC4.1p::nxtor DELETED -- LVHEAP = 5/7/8

Layer DRC4.1p::<1> DELETED -- LVHEAP = 5/7/8

DRC4.1n::pxtor = PSRCDRN OR GATES
---------------------------------
DRC4.1n::pxtor (HIER TYP=1 CFG=1 HGC=13 FGC=13 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 91 OF 176
```

```
Layer PSRCDRN DELETED -- LVHEAP = 5/7/8

DRC4.1n::<1> = ENC GATES DRC4.1n::pxtor < 3
-----------------------------------------
DRC4.1n::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 92 OF 176

Layer DRC4.1n::pxtor DELETED -- LVHEAP = 5/7/8

Layer DRC4.1n::<1> DELETED -- LVHEAP = 5/7/8

SELECT = N_PLUS_SELECT OR P_PLUS_SELECT
---------------------------------------
SELECT (HIER TYP=1 CFG=1 HGC=8 FGC=8 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 93 OF 176

DRC4.2::<1> = ENC ACTIVE SELECT < 2 ABUT == 0 OVERLAP SINGULAR
--------------------------------------------------------------
DRC4.2::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 94 OF 176

Layer SELECT DELETED -- LVHEAP = 5/7/8

Layer DRC4.2::<1> DELETED -- LVHEAP = 5/7/8

DRC4.3p::<1> = ENC CONTACT_TO_ACTIVE P_PLUS_SELECT < 1 ABUT == 0 OVERLAP
SINGULAR
------------------------------------------------------------------------
--------
DRC4.3p::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 95 OF 176

Layer DRC4.3p::<1> DELETED -- LVHEAP = 5/7/8

DRC4.3n::<1> = ENC CONTACT_TO_ACTIVE N_PLUS_SELECT < 1 ABUT == 0 OVERLAP
SINGULAR
------------------------------------------------------------------------
--------
DRC4.3n::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 96 OF 176

Layer DRC4.3n::<1> DELETED -- LVHEAP = 5/7/8

DRC4.4ps::<1> = EXT P_PLUS_SELECT < 2 NOT CONNECTED
DRC4.4pw::<1> = INT P_PLUS_SELECT < 2
-------------------------------------------------
DRC4.4ps::<1> (HIER TYP=3 HGC=0 FGC=0)
DRC4.4pw::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 98 OF 176

Layer DRC4.4pw::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC4.4ps::<1> DELETED -- LVHEAP = 5/7/8

DRC4.4ns::<1> = EXT N_PLUS_SELECT < 2 NOT CONNECTED
DRC4.4nw::<1> = INT N_PLUS_SELECT < 2
```

```
-------------------------------------------------
DRC4.4ns::<1> (HIER TYP=3 HGC=0 FGC=0)
DRC4.4nw::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 100 OF 176

Layer DRC4.4nw::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC4.4ns::<1> DELETED -- LVHEAP = 5/7/8

DRC4.4np::<1> = N_PLUS_SELECT AND P_PLUS_SELECT
-----------------------------------------------
DRC4.4np::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 101 OF 176

Layer DRC4.4np::<1> DELETED -- LVHEAP = 5/7/8

DRC5_1::<1> = NOT RECTANGLE CONTACT_TO_POLY == 2 BY == 2
--------------------------------------------------------
DRC5_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 102 OF 176

Layer DRC5_1::<1> DELETED -- LVHEAP = 5/7/8

PADS = OR PADS
--------------
PADS (HIER TYP=1 CFG=0 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 103 OF 176

Original Layer PADS DELETED -- LVHEAP = 5/7/8

DRC5_2::x = CONTACT_TO_POLY NOT PADS
------------------------------------
DRC5_2::x (HIER TYP=1 CFG=1 HGC=25 FGC=25 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 104 OF 176

DRC5_2::<1> = ENC DRC5_2::x POLY < 1.5 REGION SQUARE ABUT == 0 OVERLAP
----------------------------------------------------------------------
DRC5_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 105 OF 176

Layer DRC5_2::x DELETED -- LVHEAP = 5/7/8

Layer DRC5_2::<1> DELETED -- LVHEAP = 5/7/8

DRC5_3::<1> = EXT CONTACT_TO_POLY < 3 SQUARE SINGULAR
-----------------------------------------------------
DRC5_3::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 106 OF 176

Layer DRC5_3::<1> DELETED -- LVHEAP = 5/7/8

DRC5_4::<1> = EXT CONTACT_TO_POLY GATES < 2 REGION ABUT == 0 SINGULAR
---------------------------------------------------------------------
DRC5_4::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 107 OF 176

Layer DRC5_4::<1> DELETED -- LVHEAP = 5/7/8
```

```
DRC6_1::<1> = NOT RECTANGLE CONTACT_TO_ACTIVE == 2 BY == 2
-----------------------------------------------------
DRC6_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 108 OF 176

Layer DRC6_1::<1> DELETED -- LVHEAP = 5/7/8

DRC6_2::x = CONTACT_TO_ACTIVE NOT PADS
--------------------------------------
DRC6_2::x (HIER TYP=1 CFG=1 HGC=49 FGC=49 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 109 OF 176

Layer PADS DELETED -- LVHEAP = 5/7/8

DRC6_2::<1> = ENC DRC6_2::x ACTIVE < 1.5 REGION ABUT == 0 OVERLAP
-----------------------------------------------------------------
DRC6_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 110 OF 176

Layer DRC6_2::x DELETED -- LVHEAP = 5/7/8

Layer DRC6_2::<1> DELETED -- LVHEAP = 5/7/8

DRC6_3::<1> = EXT CONTACT_TO_ACTIVE < 3 REGION SQUARE SINGULAR
--------------------------------------------------------------
DRC6_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 111 OF 176

Layer DRC6_3::<1> DELETED -- LVHEAP = 5/7/8

DRC6_4::<1> = EXT CONTACT_TO_ACTIVE GATES < 2 REGION SQUARE ABUT == 0
SINGULAR
-------------------------------------------------------------------------
-----
DRC6_4::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 112 OF 176

Layer GATES DELETED -- LVHEAP = 5/7/8

Layer DRC6_4::<1> DELETED -- LVHEAP = 5/7/8

DRC7_2::<1> = EXT METAL1 < 3 SINGULAR
DRC7_1::<1> = INT METAL1 < 3 SINGULAR
-------------------------------------
DRC7_2::<1> (HIER TYP=3 HGC=0 FGC=0)
DRC7_1::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 114 OF 176

Layer DRC7_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC7_2::<1> DELETED -- LVHEAP = 5/7/8

BOTH_CONTACT = CONTACT_TO_POLY OR CONTACT_TO_ACTIVE
---------------------------------------------------
BOTH_CONTACT (HIER TYP=1 CFG=1 HGC=74 FGC=74 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 115 OF 176
```

```
Layer CONTACT_TO_ACTIVE DELETED -- LVHEAP = 5/7/8

DRC7_3::<1> = ENC BOTH_CONTACT METAL1 < 1 REGION SQUARE ABUT == 0
-----------------------------------------------------------------
DRC7_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 116 OF 176

Layer BOTH_CONTACT DELETED -- LVHEAP = 5/7/8

Layer DRC7_3::<1> DELETED -- LVHEAP = 5/7/8

DRC7_4::widem = METAL1 WITH WIDTH > 10
DRC7_4::thinm = METAL1 WITH WIDTH <= 10
---------------------------------------
DRC7_4::widem (HIER TYP=1 CFG=1 HGC=2 FGC=2 VHC=F VPC=F)
DRC7_4::thinm (HIER TYP=1 CFG=1 HGC=42 FGC=78 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 118 OF 176

DRC7_4::<1> = EXT DRC7_4::widem < 6 SINGULAR
--------------------------------------------
DRC7_4::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 119 OF 176

Layer DRC7_4::<1> DELETED -- LVHEAP = 5/7/8

DRC7_4::<2> = EXT DRC7_4::widem DRC7_4::thinm < 6 SINGULAR
----------------------------------------------------------
DRC7_4::<2> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 120 OF 176

Layer DRC7_4::widem DELETED -- LVHEAP = 5/7/8

Layer DRC7_4::thinm DELETED -- LVHEAP = 5/7/8

Layer DRC7_4::<2> DELETED -- LVHEAP = 5/7/8

DRC8_1::x = NOT RECTANGLE VIA == 2 BY == 2
------------------------------------------
DRC8_1::x (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 121 OF 176

OVERGLASS = OR OVERGLASS
------------------------
OVERGLASS (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 122 OF 176

Original Layer OVERGLASS DELETED -- LVHEAP = 5/7/8

DRC8_1::<1> = DRC8_1::x OUTSIDE OVERGLASS
-----------------------------------------
DRC8_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 123 OF 176

Layer DRC8_1::x DELETED -- LVHEAP = 5/7/8

Layer DRC8_1::<1> DELETED -- LVHEAP = 5/7/8
```

```
DRC8_2::<1> = EXT VIA < 3 REGION SQUARE SINGULAR
------------------------------------------------
DRC8_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 124 OF 176

Layer DRC8_2::<1> DELETED -- LVHEAP = 5/7/8

DRC8_3::<1> = ENC VIA METAL1 < 1 REGION SQUARE ABUT == 0
--------------------------------------------------------
DRC8_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 125 OF 176

Layer METAL1 DELETED -- LVHEAP = 5/7/8

Layer DRC8_3::<1> DELETED -- LVHEAP = 5/7/8

DRC9_2::<1> = EXT METAL2 < 3 SINGULAR
DRC9_1::<1> = INT METAL2 < 3 SINGULAR
-------------------------------------
DRC9_2::<1> (HIER TYP=3 HGC=0 FGC=0)
DRC9_1::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 127 OF 176

Layer DRC9_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC9_2::<1> DELETED -- LVHEAP = 5/7/8

DRC9_3::<1> = ENC VIA METAL2 < 1 REGION SQUARE ABUT == 0
--------------------------------------------------------
DRC9_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 128 OF 176

Layer VIA DELETED -- LVHEAP = 5/7/8

Layer DRC9_3::<1> DELETED -- LVHEAP = 5/7/8

DRC9_4::widem = METAL2 WITH WIDTH > 10
DRC9_4::thinm = METAL2 WITH WIDTH <= 10
---------------------------------------
DRC9_4::widem (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC9_4::thinm (HIER TYP=1 CFG=1 HGC=18 FGC=56 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 130 OF 176

DRC9_4::<1> = EXT DRC9_4::widem < 6 SINGULAR
--------------------------------------------
DRC9_4::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 131 OF 176

Layer DRC9_4::<1> DELETED -- LVHEAP = 5/7/8

DRC9_4::<2> = EXT DRC9_4::widem DRC9_4::thinm < 6 SINGULAR
----------------------------------------------------------
DRC9_4::<2> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 132 OF 176

Layer DRC9_4::widem DELETED -- LVHEAP = 5/7/8
```

```
Layer DRC9_4::thinm DELETED -- LVHEAP = 5/7/8

Layer DRC9_4::<2> DELETED -- LVHEAP = 5/7/8

DRC11_2::<1> = EXT CAP < 3 REGION SQUARE SINGULAR
DRC11_1::<1> = INT CAP < 7 REGION SQUARE SINGULAR
-------------------------------------------------
DRC11_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC11_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 134 OF 176

Layer DRC11_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC11_2::<1> DELETED -- LVHEAP = 5/7/8

DRC11_3::<1> = ENC CAP POLY < 5 REGION SQUARE ABUT == 0 OVERLAP
---------------------------------------------------------------
DRC11_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 135 OF 176

Layer DRC11_3::<1> DELETED -- LVHEAP = 5/7/8

DRC11_4::<1> = EXT ELECTRODE ACTIVE < 2 REGION SQUARE SINGULAR
--------------------------------------------------------------
DRC11_4::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 136 OF 176

Layer DRC11_4::<1> DELETED -- LVHEAP = 5/7/8

DRC11_4::<2> = EXT ELECTRODE N_WELL < 2 REGION SQUARE SINGULAR
--------------------------------------------------------------
DRC11_4::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 137 OF 176

Layer N_WELL DELETED -- LVHEAP = 5/7/8

Layer DRC11_4::<2> DELETED -- LVHEAP = 5/7/8

DRC11_5::<1> = EXT CAP CONTACT_TO_POLY < 6 REGION SQUARE SINGULAR
-----------------------------------------------------------------
DRC11_5::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 138 OF 176

Layer CONTACT_TO_POLY DELETED -- LVHEAP = 5/7/8

Layer DRC11_5::<1> DELETED -- LVHEAP = 5/7/8

DRC11_sel::x = POLY TOUCH CAP
-----------------------------
DRC11_sel::x (HIER TYP=1 CFG=0 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 139 OF 176

DRC11_sel::y = ELECTRODE TOUCH CAP
----------------------------------
DRC11_sel::y (HIER TYP=1 CFG=0 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 140 OF 176
```

```
DRC11_sel::z = DRC11_sel::x OR DRC11_sel::y
-------------------------------------------
DRC11_sel::z (HIER TYP=1 CFG=0 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 141 OF 176

Layer DRC11_sel::x DELETED -- LVHEAP = 5/7/8

Layer DRC11_sel::y DELETED -- LVHEAP = 5/7/8

DRC11_sel::<1> = DRC11_sel::z AND N_PLUS_SELECT
-----------------------------------------------
DRC11_sel::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 142 OF 176

Layer N_PLUS_SELECT DELETED -- LVHEAP = 5/7/8

Layer DRC11_sel::<1> DELETED -- LVHEAP = 5/7/8

DRC11_sel::<2> = DRC11_sel::z AND P_PLUS_SELECT
-----------------------------------------------
DRC11_sel::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 143 OF 176

Layer DRC11_sel::z DELETED -- LVHEAP = 5/7/8

Layer P_PLUS_SELECT DELETED -- LVHEAP = 5/7/8

Layer DRC11_sel::<2> DELETED -- LVHEAP = 5/7/8

DRC12_1::x = ELECTRODE NOT CAP
------------------------------
DRC12_1::x (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 144 OF 176

DRC12_1::<1> = EXT DRC12_1::x < 2 REGION SQUARE SINGULAR
--------------------------------------------------------
DRC12_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 145 OF 176

Layer DRC12_1::x DELETED -- LVHEAP = 5/7/8

Layer DRC12_1::<1> DELETED -- LVHEAP = 5/7/8

DRC12_2::<1> = EXT ELECTRODE < 3 REGION SQUARE SINGULAR
-------------------------------------------------------
DRC12_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 146 OF 176

Layer DRC12_2::<1> DELETED -- LVHEAP = 5/7/8

DRC13_1::<1> = NOT RECTANGLE CONTACT_TO_ELECTRODE == 2 BY == 2
--------------------------------------------------------------
DRC13_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 147 OF 176

Layer DRC13_1::<1> DELETED -- LVHEAP = 5/7/8
```

```
DRC13_2::<1> = EXT CONTACT_TO_ELECTRODE < 3 SQUARE SINGULAR
-----------------------------------------------------------
DRC13_2::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 148 OF 176

Layer DRC13_2::<1> DELETED -- LVHEAP = 5/7/8

DRC13_3::x = CAP AND CONTACT_TO_ELECTRODE
-----------------------------------------
DRC13_3::x (HIER TYP=1 CFG=1 HGC=1216 FGC=1216 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 149 OF 176

DRC13_3::<1> = ENC DRC13_3::x ELECTRODE < 3 REGION SQUARE ABUT == 0
OVERLAP
-------------------------------------------------------------------------
--
DRC13_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 150 OF 176

Layer DRC13_3::x DELETED -- LVHEAP = 5/7/8

Layer DRC13_3::<1> DELETED -- LVHEAP = 5/7/8

DRC13_4::x = CONTACT_TO_ELECTRODE NOT CAP
-----------------------------------------
DRC13_4::x (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 151 OF 176

Layer CAP DELETED -- LVHEAP = 5/7/8

DRC13_4::<1> = ENC DRC13_4::x ELECTRODE < 2 REGION SQUARE ABUT == 0
OVERLAP
-------------------------------------------------------------------------
--
DRC13_4::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 152 OF 176

Layer DRC13_4::x DELETED -- LVHEAP = 5/7/8

Layer ELECTRODE DELETED -- LVHEAP = 5/7/8

Layer DRC13_4::<1> DELETED -- LVHEAP = 5/7/8

DRC13_5::<1> = EXT CONTACT_TO_ELECTRODE POLY < 3 REGION SQUARE SINGULAR
-----------------------------------------------------------------------
DRC13_5::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 153 OF 176

Layer POLY DELETED -- LVHEAP = 5/7/8

Layer DRC13_5::<1> DELETED -- LVHEAP = 5/7/8

DRC13_5::<2> = EXT CONTACT_TO_ELECTRODE ACTIVE < 3 REGION SQUARE SINGULAR
-------------------------------------------------------------------------
DRC13_5::<2> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 154 OF 176
```

```
Layer CONTACT_TO_ELECTRODE DELETED -- LVHEAP = 5/7/8

Layer ACTIVE DELETED -- LVHEAP = 5/7/8

Layer DRC13_5::<2> DELETED -- LVHEAP = 5/7/8

DRC14_1::x = NOT RECTANGLE VIA2 == 2 BY == 2
-------------------------------------------
DRC14_1::x (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 155 OF 176

DRC14_1::<1> = DRC14_1::x OUTSIDE OVERGLASS
-------------------------------------------
DRC14_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 156 OF 176

Layer DRC14_1::x DELETED -- LVHEAP = 5/7/8

Layer DRC14_1::<1> DELETED -- LVHEAP = 5/7/8

DRC14_2::<1> = EXT VIA2 < 3 REGION SQUARE SINGULAR
--------------------------------------------------
DRC14_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 157 OF 176

Layer DRC14_2::<1> DELETED -- LVHEAP = 5/7/8

DRC14_3::<1> = ENC VIA2 METAL2 < 1 REGION SQUARE ABUT == 0
----------------------------------------------------------
DRC14_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 158 OF 176

Layer METAL2 DELETED -- LVHEAP = 5/7/8

Layer DRC14_3::<1> DELETED -- LVHEAP = 5/7/8

DRC15_2::<1> = EXT METAL3 < 3 SINGULAR
DRC15_1::<1> = INT METAL3 < 3 SINGULAR
--------------------------------------
DRC15_2::<1> (HIER TYP=3 HGC=0 FGC=0)
DRC15_1::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 160 OF 176

Layer DRC15_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC15_2::<1> DELETED -- LVHEAP = 5/7/8

DRC15_3::<1> = ENC VIA2 METAL3 < 1 REGION SQUARE ABUT == 0
----------------------------------------------------------
DRC15_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 161 OF 176

Layer VIA2 DELETED -- LVHEAP = 5/7/8

Layer DRC15_3::<1> DELETED -- LVHEAP = 5/7/8
```

```
DRC15_4::widem = METAL3 WITH WIDTH > 10
DRC15_4::thinm = METAL3 WITH WIDTH <= 10
---------------------------------------
DRC15_4::widem (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC15_4::thinm (HIER TYP=1 CFG=1 HGC=2 FGC=4 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 163 OF 176

DRC15_4::<1> = EXT DRC15_4::widem < 6 SINGULAR
-----------------------------------------------
DRC15_4::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 164 OF 176

Layer DRC15_4::<1> DELETED -- LVHEAP = 5/7/8

DRC15_4::<2> = EXT DRC15_4::widem DRC15_4::thinm < 6 SINGULAR
-------------------------------------------------------------
DRC15_4::<2> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 165 OF 176

Layer DRC15_4::widem DELETED -- LVHEAP = 5/7/8

Layer DRC15_4::thinm DELETED -- LVHEAP = 5/7/8

Layer DRC15_4::<2> DELETED -- LVHEAP = 5/7/8

DRC21_1::x = NOT RECTANGLE VIA3 == 2 BY == 2
--------------------------------------------
DRC21_1::x (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 166 OF 176

DRC21_1::<1> = DRC21_1::x OUTSIDE OVERGLASS
-------------------------------------------
DRC21_1::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 167 OF 176

Layer DRC21_1::x DELETED -- LVHEAP = 5/7/8

Layer OVERGLASS DELETED -- LVHEAP = 5/7/8

Layer DRC21_1::<1> DELETED -- LVHEAP = 5/7/8

DRC21_2::<1> = EXT VIA3 < 3 REGION SQUARE SINGULAR
--------------------------------------------------
DRC21_2::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 168 OF 176

Layer DRC21_2::<1> DELETED -- LVHEAP = 5/7/8

DRC21_3::<1> = ENC VIA3 METAL3 < 1 REGION SQUARE ABUT == 0
----------------------------------------------------------
DRC21_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 169 OF 176

Layer METAL3 DELETED -- LVHEAP = 5/7/8

Layer DRC21_3::<1> DELETED -- LVHEAP = 5/7/8
```

```
DRC22_2::<1> = EXT METAL4 < 6 SINGULAR
DRC22_1::<1> = INT METAL4 < 6 SINGULAR
-------------------------------------
DRC22_2::<1> (HIER TYP=3 HGC=0 FGC=0)
DRC22_1::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 171 OF 176

Layer DRC22_1::<1> DELETED -- LVHEAP = 5/7/8

Layer DRC22_2::<1> DELETED -- LVHEAP = 5/7/8

DRC22_3::<1> = ENC VIA3 METAL4 < 2 REGION SQUARE ABUT == 0
-----------------------------------------------------
DRC22_3::<1> (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 172 OF 176

Layer VIA3 DELETED -- LVHEAP = 5/7/8

Layer DRC22_3::<1> DELETED -- LVHEAP = 5/7/8

DRC22_4::widem = METAL4 WITH WIDTH > 10
DRC22_4::thinm = METAL4 WITH WIDTH <= 10
----------------------------------------
DRC22_4::widem (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
DRC22_4::thinm (HIER TYP=1 CFG=1 HGC=0 FGC=0 VHC=F VPC=F)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 174 OF 176

Layer METAL4 DELETED -- LVHEAP = 5/7/8

DRC22_4::<1> = EXT DRC22_4::widem < 12 SINGULAR
-----------------------------------------------
DRC22_4::<1> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 175 OF 176

Layer DRC22_4::<1> DELETED -- LVHEAP = 5/7/8

DRC22_4::<2> = EXT DRC22_4::widem DRC22_4::thinm < 12 SINGULAR
-------------------------------------------------------------
DRC22_4::<2> (HIER TYP=3 HGC=0 FGC=0)
CPU TIME = 0  REAL TIME = 0  LVHEAP = 5/7/8  OPS COMPLETE = 176 OF 176

Layer DRC22_4::widem DELETED -- LVHEAP = 5/7/8

Layer DRC22_4::thinm DELETED -- LVHEAP = 5/7/8

Layer DRC22_4::<2> DELETED -- LVHEAP = 5/7/8

CALIBRE HIERARCHICAL ERC completed. CPU TIME = 0  REAL TIME = 0  LVHEAP =
5/7/8  MALLOC = 6/6/6

WRITING PHDB to directory svdb
PHDB WRITE completed.  CPU TIME = 0  REAL TIME = 0  LVHEAP = 1/7/8
MALLOC = 6/6/6

--- CALIBRE::HIERARCHICAL CIRCUIT EXTRACTOR COMPLETED - Thu Mar 29
16:17:04 2007
--- TOTAL CPU TIME = 0  REAL TIME = 0  LVHEAP = 1/7/8  MALLOC = 6/6/6
```

```
--- PROCESSOR COUNT = 1

--- SPICE NETLIST FILE = schelay.lay.net
--- CIRCUIT EXTRACTION REPORT FILE = schelay.lvs.report.ext
--- PERSISTENT HIERARCHICAL DATABASE(PHDB) = svdb/schelay.phdb
--- QUERY DATABASE = svdb  TOP CELL = schelay
--- TOTAL RULECHECKS EXECUTED = 81
--- TOTAL RESULTS GENERATED = 0 (0)
--- ERC RESULTS DATABASE FILE = schelay.erc.results (ASCII)
--- ERC SUMMARY REPORT FILE = schelay.erc.summary
```

APPENDIX D

CALIBRE SYSTEM LVS REPORT

```
                ################################################
                ##                                            ##
                ##         C A L I B R E    S Y S T E M       ##
                ##                                            ##
                ##             L V S   R E P O R T            ##
                ##                                            ##
                ################################################


REPORT FILE NAME:         schelay.lvs.report
LAYOUT NAME:              schelay.lay.net ('schelay')
SOURCE NAME:
/home/hafiza/schelay/tsmc035a/schelay_tsmc035a.spi ('schelay')
RULE FILE:                /home/hafiza/_tsmc035.rules_
CREATION TIME:            Thu Mar 29 16:21:14 2007
CURRENT DIRECTORY:        /home/hafiza
USER NAME:                hafiza
CALIBRE VERSION:          v2004.3_9.21    Thu Sep 30 11:25:17 PDT 2004


                              OVERALL COMPARISON RESULTS


                          #       ###################        _   _
                        #         #                 #       *   *
                      #   #       #     CORRECT     #         |
                       # #        #                 #       \___/
                         #        ###################


********************************************************************************
************************************
                                    CELL  SUMMARY
********************************************************************************
************************************

  Result         Layout                        Source
  -----------    -----------                   --------------
  CORRECT        schelay                       SCHELAY


********************************************************************************
************************************
                                    LVS PARAMETERS
```

```
********************************************************************************
************************************
```

o LVS Setup:

```
   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   // LVS POWER NAME
   // LVS GROUND NAME
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       NO
   LVS CHECK PORT NAMES                   NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       NO
   LVS EXPAND UNBALANCED CELLS            YES
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
   LVS SPICE PREFER PINS                  NO
   LVS SPICE SLASH IS SPACE               YES
   LVS SPICE ALLOW FLOATING PINS          YES
   LVS SPICE ALLOW UNQUOTED STRINGS       NO
   LVS SPICE CONDITIONAL LDD              NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   LVS SPICE IMPLIED MOS AREA             NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS             NO
   LVS SPICE REDEFINE PARAM               NO
   LVS SPICE REPLICATE DEVICES            NO
   LVS SPICE STRICT WL                    NO
   // LVS SPICE OPTION
   LVS STRICT SUBTYPES                    NO
   LAYOUT CASE                            NO
   SOURCE CASE                            NO
   LVS COMPARE CASE                       NO
   LVS DOWNCASE DEVICE                    NO
   LVS REPORT MAXIMUM                     50
   LVS PROPERTY RESOLUTION MAXIMUM        32
   // LVS SIGNATURE MAXIMUM
   // LVS FILTER UNUSED OPTION
   // LVS REPORT OPTION
   LVS REPORT UNITS                       YES
   // LVS NON USER NAME PORT
   // LVS NON USER NAME NET
   // LVS NON USER NAME INSTANCE

   // Reduction

   LVS REDUCE SERIES MOS                  NO
   LVS REDUCE PARALLEL MOS                YES
   LVS REDUCE SEMI SERIES MOS             NO
```

```
   LVS REDUCE SPLIT GATES                 YES
   LVS REDUCE PARALLEL BIPOLAR            YES
   LVS REDUCE SERIES CAPACITORS           YES
   LVS REDUCE PARALLEL CAPACITORS         YES
   LVS REDUCE SERIES RESISTORS            YES
   LVS REDUCE PARALLEL RESISTORS          YES
   LVS REDUCE PARALLEL DIODES             YES

   // Filter

   LVS FILTER  sch_filter_direct_open  OPEN SOURCE DIRECT
   LVS FILTER  sch_filter_direct_short  SHORT SOURCE DIRECT
   LVS FILTER  sch_filter_mask_open  OPEN SOURCE MASK
   LVS FILTER  sch_filter_mask_short  SHORT SOURCE MASK
   LVS FILTER  lay_filter_direct_open  OPEN LAYOUT DIRECT
   LVS FILTER  lay_filter_direct_short  SHORT LAYOUT DIRECT
   LVS FILTER  v  OPEN
   LVS FILTER  i  OPEN
   LVS FILTER  e  OPEN
   LVS FILTER  f  OPEN
   LVS FILTER  g  OPEN
```

CELL COMPARISON RESULTS (TOP LEVEL)


```
LAYOUT CELL NAME:         schelay
SOURCE CELL NAME:         SCHELAY

------------------------------------------------------------------------------
-----------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              2         2

 Nets:              11        11

 Instances:         10        10         MN (4 pins)
                     3         3         MP (4 pins)
                     2         2         C (2 pins)
                ------    ------
 Total Inst:        15        15
```

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	2	2	
Nets:	10	10	
Instances:	8	8	MN (4 pins)
	3	3	MP (4 pins)
	2	2	C (2 pins)
	1	1	SMN2 (4 pins)
Total Inst:	14	14	

****
****
INFORMATION AND WARNINGS
****
****

Component	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Type
Ports:	2	2	0	0	
Nets:	10	10	0	0	
Instances:	8	8	0	0	MN(N)
	3	3	0	0	MP(P)
	2	2	0	0	C(NOTCHEDROW)
	1	1	0	0	SMN2
Total Inst:	14	14	0	0	

o Initial Correspondence Points:

Ports: GND VDD

****
****
SUMMARY
****
****

Total CPU Time: 0 sec
Total Elapsed Time: 0 sec