CHAPTER 3

METHODOLOGY

3.1   General Utilizing of Mentor Graphic

Simulation mode consist of utilizing Mentor Graphic software. The technology is set to 0.35 tsmc (Taiwan Manufacturing Semiconductor Company) to describe small feature of the design and at the end of the process it shows how close it can be fabricated during manufacturing process. Mentor Graphic software is a software where designer can design and simulated their circuit at the schematic phase before proceed to the next step which is to produce layout when the circuit is done through the simulation. The process flow of the software shown in the below flow chart in **Figure 3.1**.

Generally, Mentor Graphic software consist of two parts. The first part is the Design Architect (DA). The purpose of this part is as a starting point for designers to start designing their circuit schematic for their circuit. The results of the performance of the design are analyze here.

Circuit schematic that has been analyze will be go through the Schematic Driven Layout Phase (SDL). The schematic is converted into layout at this phase. Layout start to design and the layout must follow the design rules as mention in chapter 2.

The next step of the design is go through two simulation to make sure that the design achieve the specification desire in layout design. The first simulation is, Calibre Design Rules Check (DRC). DRC; main purpose is to check whether the layout produced

followed the layout design rules. An example is the spacing between polysilicon and contact must be 3λ. If the spacing of polysilicon and the contact less that the mention, an error message will pop-up after simulation session is done.   Designers need to repair this error until the design is error- free. Another simulation which is need to be done is the simulation by Calibre Layout Versus Schematic(LVS) , where it compares layout and schematic whether it correspond to each other. It will inspect whether every port declared at schematic phase is the same port that has been declared in layout session. The error will pop-up if it encounters error and designer need to repair it until it passed and shows no error message The final design can delivered to clean room to be fabricated.

3.1.1   Schematic.

To design a schematic layout, the Design Architect (DA) is the software to used. It contains a standard cell library where tools been place and provide simulation after circuit been design. Meanwhile auto placing/ routing layout which is embedded with physical layout is available in the 'ic library'. The technology to be used can be chosen here. Block of symbol should be created after the schematic design has been set up. This symbol is used to generate netlist to make sure all the configuration in the schematic are correct. Schematic should be checked and saved first before the block of symbol is generated. Each input and output should be named in order for easy port reorganization.

3.1.2   Layout

The layout must pass a series of checks in a process known as verification. The two most common checks in the verification process are Design Rule Checking (DRC), and Layout Versus Schematic (LVS).

3.1.3   DRC (Design Rules Check)

Design Rule Checking or Check(s) (DRC) is the area of <u>Electronic Design Automation</u> that determines whether a particular chip design satisfies a series of recommended parameters called Design Rules. Design rule checking is a major step during <u>Physical verification</u> of the design, which also involves LVS (<u>Layout versus schematic</u>) Check, XOR Checks, ERC (Electrical Rule Check) and Antenna Checks

3.1.4 LVS(Layout Versus Schematic)

LVS-check recognizes the electrical components of the layout, as well as the connections between them, and compares them with the schematic or circuit diagram.

LVS Checking involves following three steps:

I. Extraction:

The software program takes a database file containing all the layers drawn to represent the circuit during layout. It then runs the database through many logic operations to determine the semiconductor components represented in the drawing by their layers of construction. It then examines the various drawn metal layers and finds how each of these components connects to others.

II. Reduction:

During reduction the software generates a <u>netlist</u> representation of the layout database.

III. Comparison:

The extracted layout netlist is then compared this to a netlist taken from the circuit schematic. If the two netlists match, then the circuit passes the LVS check. At this point it is said to be "LVS clean."
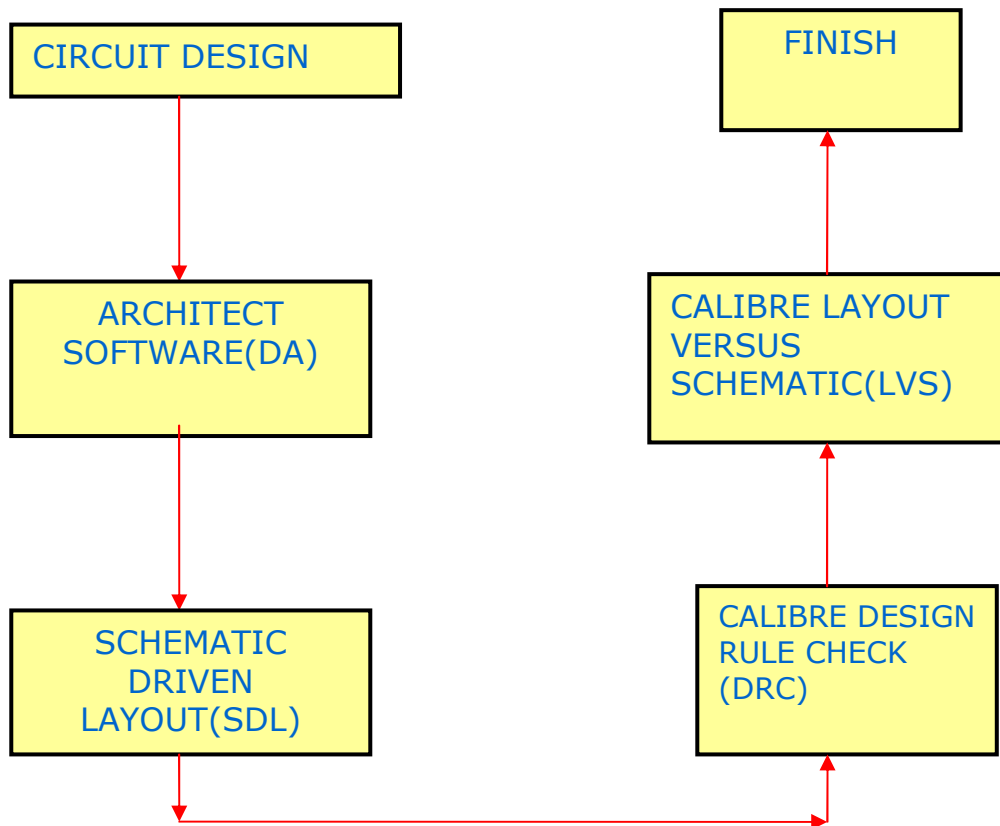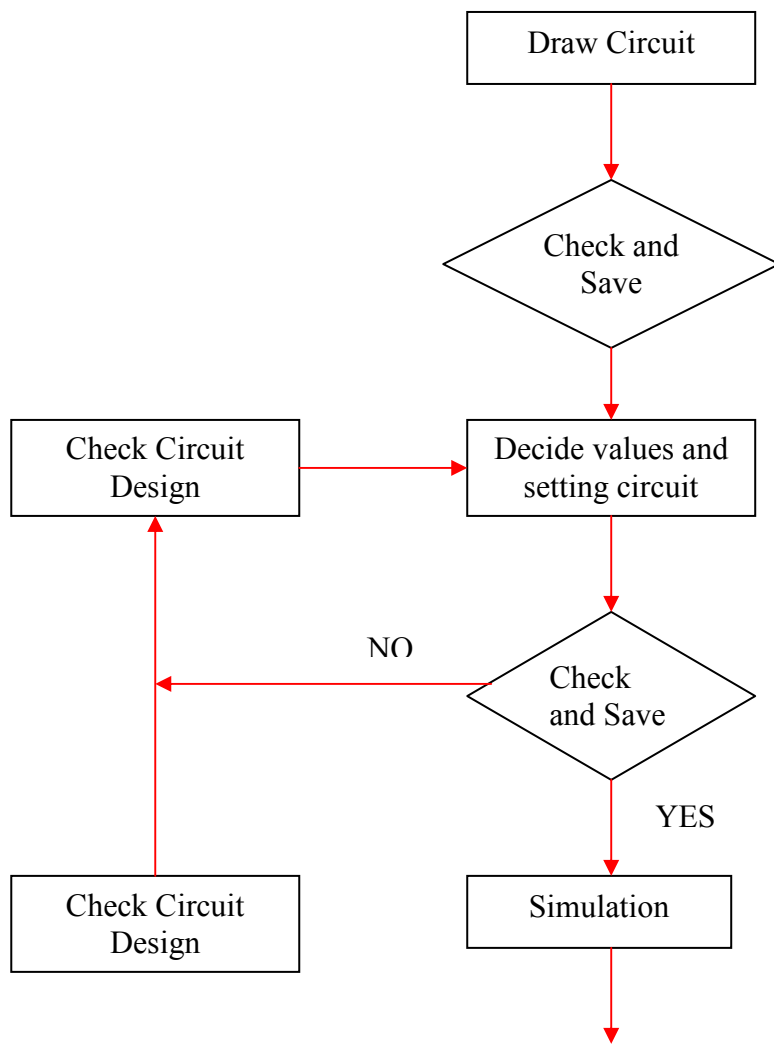
3.2 Process Flow

```
┌─────────────────────┐                    ┌─────────────────────┐
│   CIRCUIT DESIGN    │                    │       FINISH        │
└─────────────────────┘                    └─────────────────────┘
           │                                          ▲
           ▼                                          │
┌─────────────────────┐                    ┌─────────────────────┐
│     ARCHITECT       │                    │  CALIBRE LAYOUT     │
│   SOFTWARE(DA)      │                    │  VERSUS             │
│                     │                    │  SCHEMATIC(LVS)     │
└─────────────────────┘                    └─────────────────────┘
           │                                          ▲
           ▼                                          │
┌─────────────────────┐                    ┌─────────────────────┐
│     SCHEMATIC       │                    │  CALIBRE DESIGN     │
│      DRIVEN         │                    │  RULE CHECK         │
│   LAYOUT(SDL)       │                    │  (DRC)              │
└─────────────────────┘                    └─────────────────────┘
           │                                          ▲
           └──────────────────────────────────────────┘
```
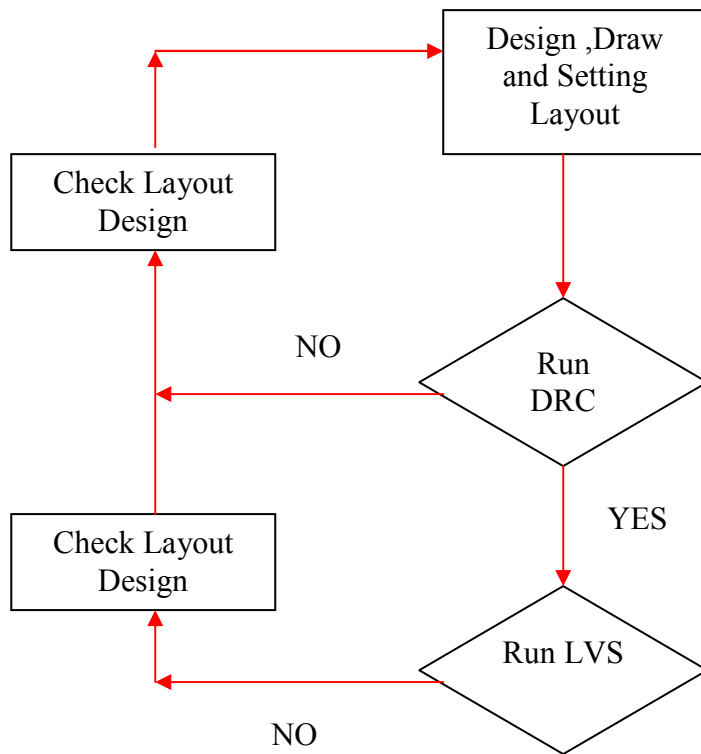
Figure 3.1: Process Flow of Mentor Graphic Software

```
                          ┌─────────────────┐
                          │   Draw Circuit  │
                          └─────────────────┘
                                   │
                                   ▼
                              ◇ Check and ◇
                              ◇   Save    ◇
                                   │
                                   ▼
┌─────────────────┐      ┌─────────────────┐
│ Check Circuit   │─────▶│ Decide values and│
│ Design          │      │ setting circuit  │
└─────────────────┘      └─────────────────┘
       ▲                          │
       │                          ▼
       │          NO        ◇  Check   ◇
       │◀──────────────────◇ and Save ◇
       │                          │
       │                        YES│
┌─────────────────┐      ┌─────────────────┐
│ Check Circuit   │      │   Simulation    │
│ Design          │      └─────────────────┘
└─────────────────┘              │
                                 ▼
```

NO

View
waveform

YES

Procede to layout
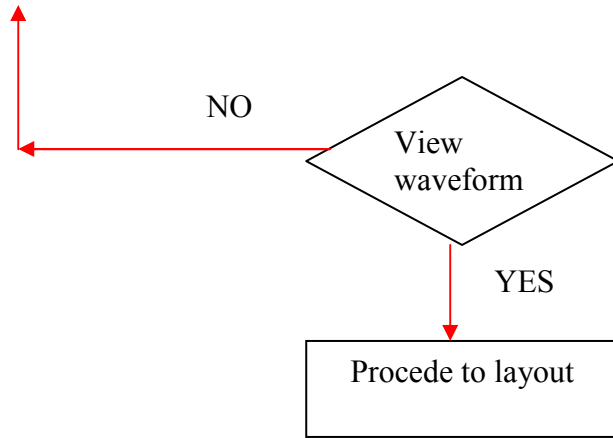
Figure 3.2: Flow chart at the schematic phase

Design ,Draw
and Setting
Layout

Check Layout
Design

NO

Run
DRC

YES

Check Layout
Design

Run LVS

NO

YES

END
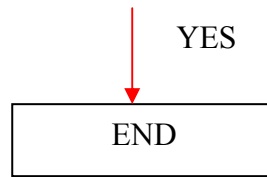
Figure 3.3: Flow chart for layout process

3.3   Circuit Overview

Before starting to draw schematic and layout, some theorytical calculation need to be done. It is important as a guidance during the simulation thus makes the work become regulated in place. In addition, the values will be the bench mark of the design. As mention in chapter 1, the project design specification is using the specification of Digital Enhanced Cordless Telecommunication (DECT). Calculation process includes the determination for voltage gain, voltage supply and transistor size that are used during simulation process.

The circuit used 12 Complementary Metal-Oxide Semiconductor(CMOS) transistor and two capacitor. It includes one R-C-R filter that react as detention voltage, Vs from being injected into current bias chain.

3.4   Circuit Specification.

Table 3.1 Specification of LNA Circuit

Specification	Value
V_{DD}	3.3V
u_n	415.86×10^{-4}
u_p	150.63×10^{-4}
C_{ox}	4.56×10^{-3}
f_o	1.9GHZ
$V_{TH,p}$	0.69V
$V_{TH,N}$	0.5V

λ	$0.2V^{-1}$
f_o	1.9GHz
Noise factor	$NF \prec 3dB$
Voltage gain	15 dB
Power at 3.3V	40mW

Table 3.1 is specification and assumption been made while designing amplifier core of the low noise amplifier. These values is only an assumption values. It is not compulsory applied in design characteristic.
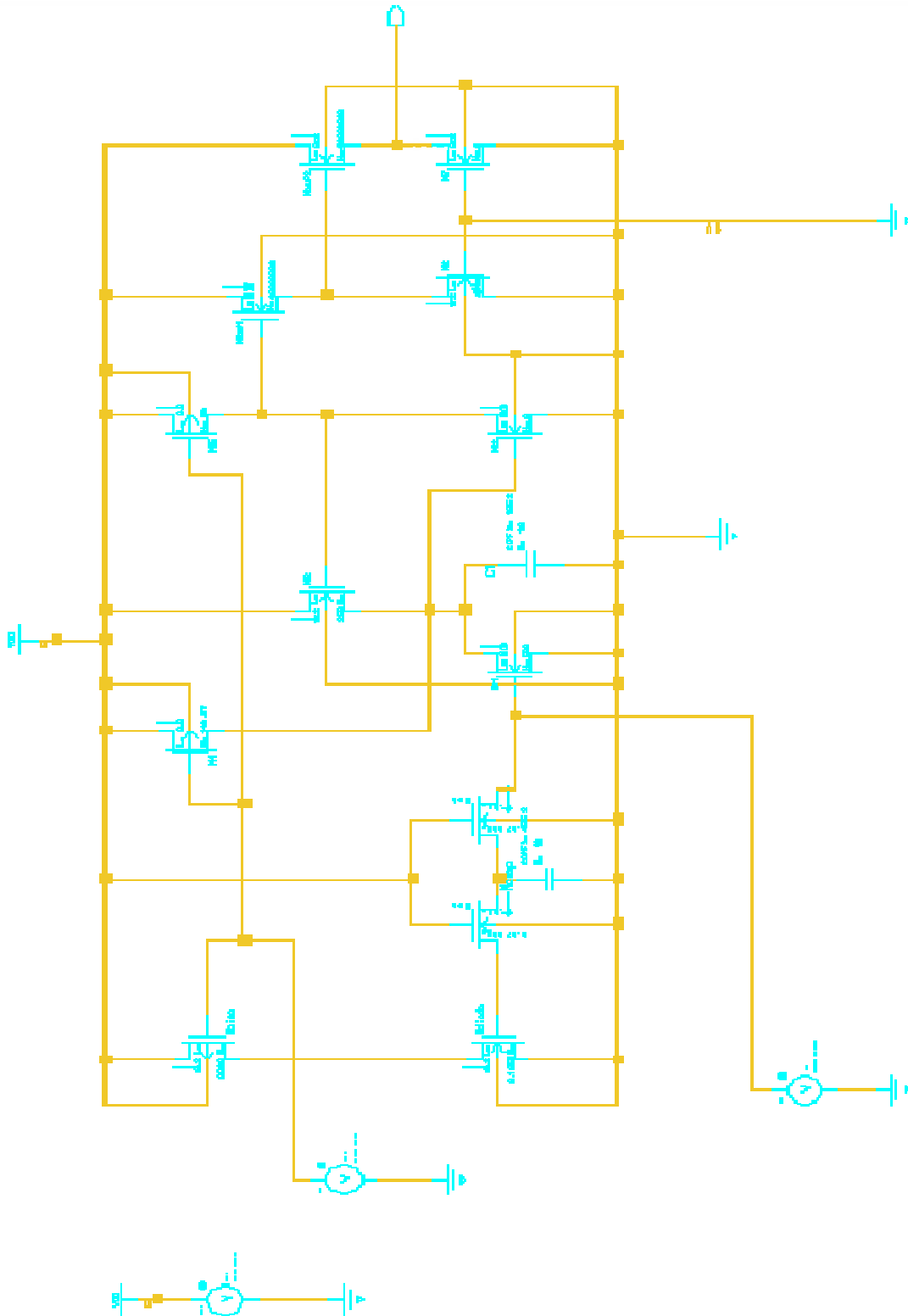
Figure 3.4: Circuit of Wideband Low Noise Amplifier

3.4.1 Determine size of M1

$$NF = 1 + \frac{4kT\frac{2}{3}\frac{1}{g_{m1}}}{4kTR_s} = 1 + \frac{2}{3g_{m1}R_s} \tag{3.1}$$

$$2 = 1 + \frac{2}{3g_{m1}50\Omega}$$

$$\frac{1}{g_{m1}} = 75\Omega \ \text{ or } \ g_{M1} = 0.013\Omega$$

g_{m1} are in connection with bias current I_{D1} and $\left(\frac{W}{L}\right)_1$ as follow:

$$g_{M1} = \sqrt{2I_{D1}u_n C_{ox}\left(\frac{W}{L}\right)_1} \tag{3.2}$$

$$0.013\Omega = \sqrt{2I_{D1}u_n C_{ox}\left(\frac{W}{L}\right)_1}$$

$$\left(\frac{W}{L}\right)_1 = ? \ ; \ I_{D1} = ?$$

Power specifications and noise is dominated by the first stage of amplifier. If noise occur, and it need to be minimize, transconductance at transistor M_1 is larger than transconductance at transistor M_2 and transistor M_3, $g_{M1} > g_{M2}, g_{M3}$. It also mean, current flow at transistor M_1 is larger than current flow through transistor M_2 and transistor

M3, $I_{M1} >$ $I_{M2,}I_{M3}$. So the power of the amplifier core is dominated by current I_{D1}. From **Figure 3.4**, there are four branches that are $M_{diode}, M_1, M_{buf1}, M_{buf2}$. Assume that each branch carries same current. Thus, the total current is $4 \times I_{D1}$. So, the total power is given as $4 \times I_{D1} \times V_{dd}$.

$$I_{D1} \leq \frac{P_{total}}{4 \times V_{dd}} = \frac{40mW}{4 \times 3.3V} = 3mA \tag{3.3}$$

Use some safety margin and set

$$I_{D1} = 1.2mA$$

Recall back to (3.7-2);

$$0.013\Omega = \sqrt{2 I_{D1} u_n C_{ox} \left(\frac{W}{L}\right)_1}$$

$$0.013\Omega = \sqrt{2(1.2mA)1.896 \times 10^{-4} \left(\frac{W}{L}\right)_1}$$

$$\left(\frac{W}{L}\right)_1 = 371.395$$

$$\left(\frac{W}{L}\right)_1 = \frac{130um}{0.35um}$$

3.4.2 Determine size of M2

Using the gain specification from Figure 3.4 that is Av= 15db or 5.6 and above calculation, $g_{M1} = 0.013\Omega^{-1}$

As mention in literature review chapter 2, from (2.14):

$$A_v = g_{M1} \frac{1}{g_{M2}}$$

$$5 = \frac{g_{M1}}{g_{M2}} = \frac{0.013\Omega^{-1}}{g_{M2}}$$

$$g_{M2} = 2.6m\Omega^{-1}$$

To achieve the g_{M2} value, which is 5 time lesser than g_{M1}, two variable appear, I_{D2} and $\left(\dfrac{W}{L}\right)_2$.

Simple choice to get $I_{D2} < I_{D1}$ and $\left(\dfrac{W}{L}\right)_2 < \left(\dfrac{W}{L}\right)_1$

$$I_{D2} = \frac{1}{5} I_{D1} \qquad\qquad\qquad \left(\frac{W}{L}\right)_2 = \frac{25.98um}{0.35u}$$

$$I_{D2} = \frac{1}{5}(1.2mA)$$

$$I_{D2} = 0.24mA$$

I_{D2} is set smaller than I_{D1} so it meet the assumption during M1 set up, that is $I_{M1} \succ I_{M2}$. It is also related to $\left(\dfrac{W}{L}\right)_2$ because if $\left(\dfrac{W}{L}\right)_2$ small, it will produce smaller C_{gs2}.

Power assume 45% from specification, 40mW = 18mW

$$P = 4 \times I_{bias} \times V_{dd} \qquad (3.4)$$

$$18mW = 4 \times I_{bias} \times 3.3V$$

$$18mW = 13.2 \times I_{bias}$$

$$I_{bias} = 1.363mA$$

Assume in saturation Mode

$$I_D = 0.5u_p C_{ox} \left[\frac{W}{L} \right] (V_{gs} - V_{th,p})^2 \qquad (3.5)$$

$$1.363mA = 0.5u_p C_{ox} \left[\frac{W}{L} \right] (0.9245 - 0.69)^2$$

$$1.363mA = \left[\frac{W}{L} \right] 1.889 \times 10^{-6}$$

$$721.578 = \left[\frac{W}{L} \right]$$

$$\left[\frac{W}{L} \right]_{Mbias} = \left(\frac{252.55}{0.35} \right)$$

3.4.3 Determine size of M3

Refer back from specification, fo= 1.9 GHz. To pass the signal, f_{-3db} should larger than 1.9 Ghz. To simplify, f_{-3db} is set so its equal fo= 1.9Ghz.

$$f_{-3db} = \frac{g_{M3}g_{M2}R_{op}}{2\eta C_{PD1}}$$ (3.6)

Obtain the parasitic capacitor, C_{PD1}, at the drain of M1. Once more, need to assume that the parasitic capacitance of large transistor M1 dominate C_{PD1}.

$$C_{PD1} = C_{gd1} + C_{db1}$$ (3.7)

C_{gd1} is drain overlap capacitance of M1 and is given by

$$C_{gd1} = w \cdot L_D \cdot C_{ox}$$ (3.8)

Lateral diffusion, $L_D = 0.12$um

$$C_{ox} = 1\frac{fF}{um^2}$$

Process 0.8um

So, $C_{gd1} = w \cdot L_D \cdot C_{ox}$ (3.9)

$$= 590\text{um} \times 0.12\text{um} \times 1\frac{fF}{um^2}$$

$$= 70.8\text{fF}$$

C_{db1} is capacitance from drain to substrate and given as

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{V_{db}}{\psi_0}}}$$ (3.10)

Where

$$C_{db0} = C_{jsw0} \times drain - parameter + C_{j0} \times drain - area \tag{3.11}$$

Assume design rules specifies the height of drain area to 9um, $C_{jswo} = 1\dfrac{fF}{um^2}$ and

$$C_{jo} = 0.18\frac{fF}{um}. \tag{3.12}$$

Substituting information above,

$$C_{db0} = \frac{1fF}{um}(590um + 9um + 9um) + \frac{1fF}{um^2}(590um \times 9um) \tag{3.13}$$

$$= 608fF + 956fF$$

$$= 1564fF$$

Note that $V_{db} = \sqrt{\dfrac{2I_{D3}}{k'\left(\dfrac{W}{L}\right)_3}} + V_T$ \hfill (3.14)

I_{D3} need to be set as small as possible to achieve save power. However, the assumption that I_{D3} is small enough at M3 has been neglected.

$$V_{db} \approx V_T = 1V \tag{3.15}$$

$V_T = 1V$(given in process)

$$\Psi_0 = 0.65V \text{ (given in process)}$$

Substituting (3.13),(3.15) and $\Psi_0 = 0.65V$ into (3.10).

$$C_{db1} = 981fF \tag{3.16}$$

Substituting (3.9) and (3.16) into (3.7),

$$C_{PD1} = 981fF + 70.8fF = 1052fF \tag{3.17}$$

Previous calculations show that for large devices, the source and drain to substrate capacitance is important. Substituting (3.17) and g_{m2} into (3.6) and predict for $g_{m3}R_{op}$

That will result $f_{-3db} = 1.9GHz = \dfrac{g_{M2} \times g_{M3}R_{op}}{2\Pi C_{PD1}}$

$$= \dfrac{\dfrac{1}{750\Omega}}{2\Pi(1052fF)} \Rightarrow G_{M3}R_{op} = 9.5 \tag{3.18}$$

Assume that $r_{o3} \prec r_{o5,}$, so $R_{op} \approx r_{03}$. Substituting this into (3.18),

$$g_{M3}r_{o3} = 9.5 \tag{3.19}$$

After calculating r_{o3}, current I_{D3} need to be determined. I_{D3} is set so the value is approximately the same value of I_{D2} in order get limited power consumption. Use the theory of R_{on} for transistor to operate.

$$r_{o3} = \dfrac{1}{\lambda I_{D3}} = \dfrac{1}{(0.2V^{-1})(0.12mA)} = 41.5k\Omega \tag{3.20}$$

(channel length modulation factor in 0.35-um= $0.2V^{-1}$)

Substituting (3.16) into (3.15),

$$g_{M3} = \frac{9.5}{r_{o3}} = \frac{9.5}{41.5k\Omega} = \frac{1}{4.3k\Omega} = 0.23m\Omega^{-1}$$

Now size of transistor M3 can be determined ,

$$g_{M3} = \frac{1}{4.3k\Omega} = \sqrt{2 \times 0.12mA \times u_n C_{ox} \times \left(\frac{W}{L}\right)_3}$$

$$= 2.2 = \frac{0.77um}{0.35um} \approx \frac{1um}{0.35um}$$

3.4.4 Determine Size of M_4.

The size of M4 need to be determining as it controls the current flow through the circuit. Using back equation transistor in saturation mode;

$$I_D = 0.5u_p C_{ox} \left[\frac{W}{L}\right] \left(V_{gs} - V_{th,p}\right)^2$$

Here, there are two values which are not identified that is, min value of V_{gs} and size of transistor M4

Thus, assumption has been made for size of $\left(\frac{W}{L}\right)_4 = \frac{65.63um}{0.35um}$, so

$$I_D = 0.5 u_p C_{ox} \left[\frac{W}{L} \right]_4 \left(V_{gs} - V_{th,p} \right)^2$$

$$1.08 mA = 0.5 \times 6.87 \times 10^{-5} \times \left(\frac{100 um}{0.35 um} \right) \left(V_{GS} - 0.69 V \right)^2$$

$$1.08 mA = 9.814 mA \left(V_{Gs} - 0.69 V \right)^2$$

$$0.331 = V_{GS} - 0.69 V$$

$$V_{GS} = 1.021 V \rightarrow \text{Min value for } V_{bias1}$$

Note that I_D is total current of I_{D1} and I_{D2}

$$I_{D1} - I_{D2} = I_{D4}$$

$$1.2 mA - 0.12 mA = 1.08 mA$$