# CHAPTER 2

# LITERATURE REVIEW

## 2.1    History of Wireless and Application

The wireless era was started by two European scientists, James Clerk Maxwell and Heinrich Rudolf Hertz. In 1984, Maxwell presented the Maxwell's equations by combining the works of Lorentz, Faraday, Ampere and Gauss [6]. He predicted the propagation of electromagnet waves in free space at the speed of light. His theory was accepted 20 years later, after Hertz validated electromagnetic wave (wireless) propagation. Hertz demonstrated RF generation, propagation and reception in the laboratory.  His work then continue by Guglielmo Marconi after 2 decades. He then acquire a method for transmitting and  receiving information. Marconi started to commercialized the use of electromagnet wave propagation for wireless telegraphs and allowed the transfer of information from one continent to another without physical connection [6]. Since the cellular mobile phone system was introduced in the early 1980's, the wireless industry has gone several generations of revolutionary changes. Other  examples for this  application are in remote sensing, broadcast, smart automobile and highways and so on.

## 2.2    Noise

Noise limits the minimum signal level that a circuit can process with acceptable quality [3]. In addition, it is a random process. Nowadays, it is important to analogue

designers to deal with the problem of noise because it trades with power dissipation, speed and linearity. Circuit noise is associated with the electrical components that build the subcomponents, such as resistor and transistor. The noise phenomena considered are caused by small current and voltage fluctuation that are generated within the device themselves.

### 2.2.1 Noise Sources.

Circuit noise is subdivided into three part which are thermal noise, shot noise and flicker noise.

### 2.2.1.1 Thermal Noise.

Thermal Noise basically occur due to the random thermally generated motion of electrons [5]. It occurs in resistive devices and is proportional to the temperature. Fundamentally, the thermal energy of electrons causes them to move randomly, causing local concentrations of electrons. This net concentration of negative charge in a local spot will result in a local nonzero voltage. As the concentration changes randomly, the resulting voltage also changes randomly, resulting in a noiselike behavior. The important thing is noise exist even though the resistor is not connected and no current is flowing through it.

$$\frac{\overline{v^2}}{\Delta f} = 4kTR \quad \text{or} \quad \frac{\overline{i^2}}{\Delta f} = 4kT\frac{1}{R} \tag{2.1}$$

Where,

$\overline{v^2}$ = Square noise voltage

$\overline{i^2}$ = Square noise current

k = Boltzman Constant

T　= Temperature in Kelvin

R　= Resistance value

## 2.2.1.2　Shot Noise

Shot noise occur in all energy barrier junctions, usually, in diodes and bipolar transistors. Actually, it happen whenever a flux of carrier passes over an energy boundary. Since the potential energy of the carrier is random, the number of carriers that possess enough energy to cross the barrier is random in nature, resulting in a flux whose density is also random in nature. This random nature gives rise to shot noise. It is thus obvious that shot noise exists only when there is a current, as opposed to thermal noise. For example, a bipolar junction resistor (BJT) is a device whose current $I$ is composed of holes and electrons that have sufficient energy to overcome the potential barrier at the junction. Thus, the current consists of discrete charges and not of continuum of charges. The fluctuation in the current $I$ is termed shot noise. This current, $I$ is composed of random pulses with average value $I_{DC}$.

$$\frac{\overline{i^2}}{\Delta f} = 2qI_{dc} \qquad\qquad (2.2)$$

Where,

q = charge of an electron in coulomb

$I_{dc}$ = Value of dc current in amperes

## 2.2.1.3  Flicker Noise

Flicker noise or *1/f* noise arises from random trapping of charge at the oxide –silicon interface of MOS transistor and in some resistive devices. The idea is, more current that is flowing in a non ideal silicon interface, the higher is the rate of electrons that are trapped. The time constants associated with these trapping and releasing process give rise to a noise signal with energy at low frequencies. Consequently, the noise density is given by:-

$$\frac{\overline{i^2}}{\Delta f} = K \frac{I^\alpha}{f} \tag{2.3}$$

Where,

K  = constant that depend on nature of the device

α  = constant that depend on nature of the device

*I*  = dc current in amperes

f  = frequency in hertz

## 2.2.2  Noise Figure

A parameter called noise figure (NF) is a commonly used method of specifying the additive noise inherent in a circuit or system. Use of this parameter is limited to situation where the sources impedance is resistive. However, it is often the case in a front end, and so this method of specifying noise is adopted here.

The noise figure describe how much the internal noise of an electronic element degrades its SNR (signal noise ratio). It is often specified for a 1Hz bandwidth at a given frequency. In this case, the noise figure is also called spot noise figure to emphasize the very small bandwidth as opposed to the average noise figure, where the band of interest is taken into account. The noise figure is defined as:

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{S_{in} N_{out}}{S_{out} N_{in}} \tag{2.4}$$

Where,

$N_{in}$ : input power and always taken as the noise in the source resistance.

$N_{out}$ : output noise power including the circuit contribution and noise transmit from the source resistance.

Combine S$_{out}$ = GS in into equation above, where G is power gain of corresponding stage,

$$NF == \frac{N_{out}}{GN_{in}} \tag{2.5}$$

2.3  Filter

A passive microwave filter is a circuit component consisting of lumped elements (inductors, capacitors and resistor) only or distributed elements or both arranged in particular configuration so that desired signal frequencies are allowed to pass with minimum possible attenuation while undesired frequencies are attenuated. In the design of a filter, the important specification one looks into are frequency range, bandwidth, insertion

loss, stopband attenuation and frequencies, input and output impedance levels, voltage standing- wave ratio (VSWR), group delay, temperature range and transient response [6].

## 2.3.1   Types of Filter

Basically, there are four types of filters, that are the low pass, band-pass, band stop and high-pass. Their frequency response is shown in below figure.
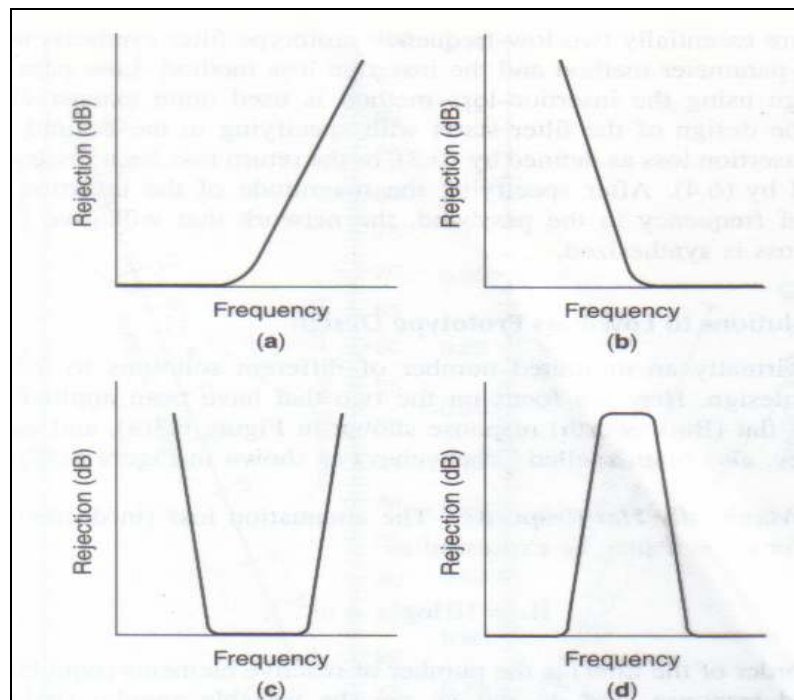


**Figure 2.1**: Basic filter responses (a) Low pass; (b)  High-pass; (c) Bandpass and (d) Bandstop

An ideal filter would have zero insertion loss and constant group delay across the desired. All filters shows fake response where they have low loss where the rejection should be high. The best way to accomplished are to have filter perform well over estimated frequency.

2.4   Analog  Circuit Design Topology.

Amplification is an important function in most analog circuit. The amplification process cause either signal from digital or analog is too small to drive load, overcome noise came from previous stage or bring logical level to digital circuit. Some  aspects that must be take into account while designing amplifier and measure performance amplification process are power dissipation, supply voltage, linearity and noise [1]. In addition, input and output impedance also play some role to  determine how the circuit interact  leading and lagging stages. Below figure shows parameter that need to highlight while designing an amplifier.
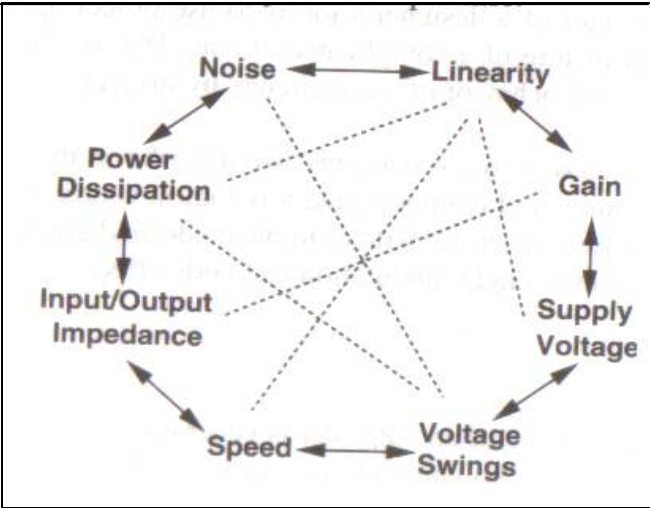


**Figure 2.2**: Trade off while designing analog circuit

2.4.1    Introduction to Circuit Design

Derivation of the low- frequency small-signal at amplifier core

$$A_v = (\text{gain if } 1^{st} \text{ stage}) \times (\text{ gain of } 2^{nd} \text{ stage}) \qquad (2.6)$$

 From circuit

$$\text{Gain of } 1^{st} \text{ stage} = -g_{m1} = \frac{I_{M1}}{v_{in}} \qquad (2.7)$$

and

$$\text{Gain of } 2^{nd} \text{ stage} = \frac{v_{d3}}{i_{M1}} \qquad (2.8)$$

$$\text{Gain of the } 2^{nd} \text{ stage} = \frac{a}{1 + af} \qquad (2.9)$$

Where,

$a$ = forward gain with loading and f = feedback factor

To calculate $a$, refer to **Figure 2.3**, which show the forward amplifier with loading from the feedback network. It is shown as two M2 transistor with the drain grounded at the

input and output nodes). From the circuit, $im1$ flows into a resistance of $\dfrac{1}{g_{m2}} \| Rin_{M3}$

$= \dfrac{1}{g_{m2}}$ This will develops a voltage of $\dfrac{I_{M1}}{g_{M2}}$. The voltage multiplied to voltage gain of M3

to develop $v_{d3}$. For the single stage CS amplifier, the voltage gain is simply $g_{M3}r_{out}$ , where

$r_{out} = r_{o3} \| r_{o5} \| r_{in2} = r_{o3} \| r_{o5}$ as $r_{in} = \infty$. Here $r_{o3}$ and $r_{o5}$ are the output resistance of $M_3$

and $M_5$ and $r_{in}$ is the input resistance of $M_2$. Now $r_{o3} \| r_{o5} = R_{op}$ , so
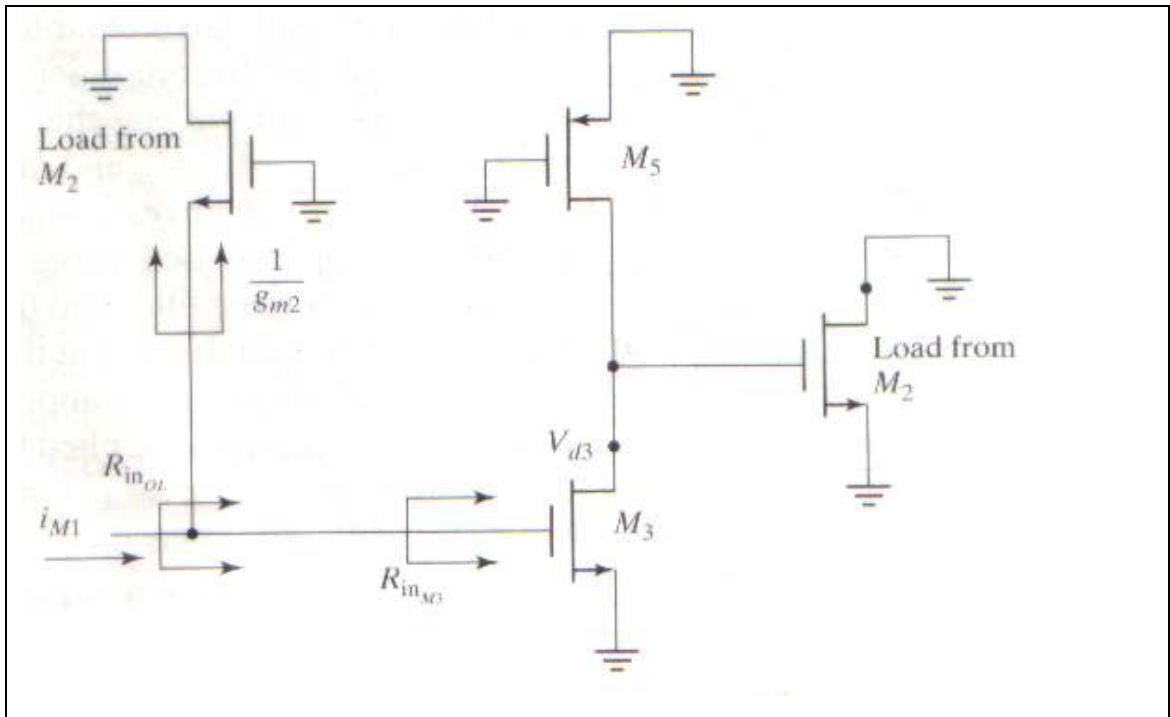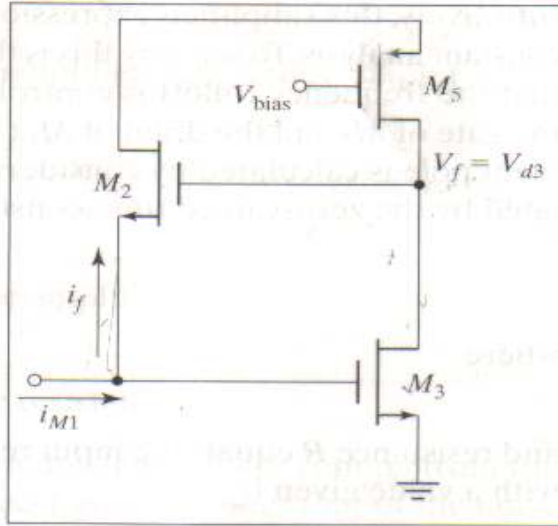


Figure 2.3: The a circuit of core amplifier with loading

$$v_{d3} = -\left( \frac{I_{M1}}{g_{M2}} g_{M3} R_{op} \right) \tag{2.10}$$

From (2.10)

$$a = \frac{v_{d3}}{I_{M1}} = -\left( \frac{I_{M1}}{g_{M2}} g_{M3} R_{op} \right) \tag{2.11}$$

which is very large, as $R_{op}$ is large. Based on **Figure 2.4** $f$ is defined as

$$\frac{i_f}{v_f} = -g_{M2} \qquad (2.12)$$



**Figure 2.4**: The $f$ circuit of core amplifier with loading

Substituting (2.11) and (2.12) into (2.9), note that since $af$ is very large, it follow that

$$\text{Second stage gain} \approx \frac{1}{f} \qquad (2.13)$$

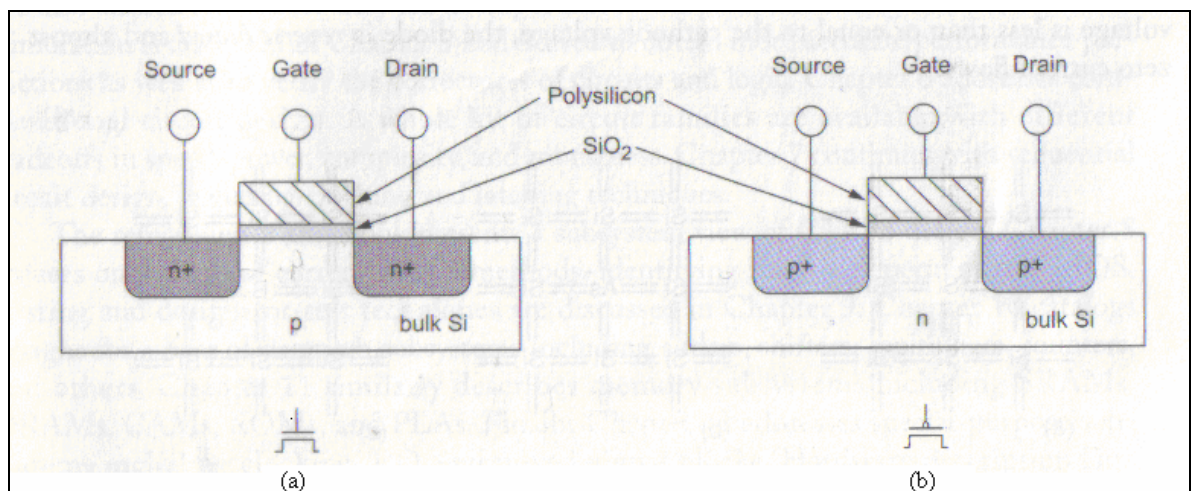Substituting (2.12) into (2.13) ,

$$\text{Second stage gain} \approx -\frac{1}{g_{M2}} \qquad (2.14.)$$

Substituting (2.7) and (2.14) into (2.6), produce:

$$A_v = g_{M1} \frac{1}{g_{M2}} \qquad (2.15)$$

Notice that the body effect lost has been neglected

## 2.5 Metal-Oxide-Semiconductor(MOS) Transistor Theory.



**Figure 2.5**: Transistor (a) nMOS (b) pMOS

Transistor is called, T-R-A-N-S-I-S-T-O-R, because it is a resistor or semiconductor devices which can amplify electrical as they are transferred[4]. Semiconductor is a group of materials having electrical conductivities intermediate between metals and insulators. The materials are found in columns IV and neighboring columns of the periodic table ( Refer to appendix A).

Silicon (Si), is one example of semiconductor that have basic form material for build transistor. Pure silicon contain of a dimensional three lattice of atoms. Because silicon is group IV element, it construct covalent bonds with four adjacent atom. All its valance electrons involved in chemical bond, make it poor conductor. The conductivity can be increase by introducing small amount of impurities into the silicon. This impurities is called as dopants.

A junction between p-type and n-type  is called a diode, as shown in **Figure 2.5**. When the voltage on the p-type semiconductor, called as anode, raised above the n-type cathode, the diode is forward bias and current will flow. Otherwise, if the anode voltage is less that or equal to the cathode voltage, the diode is in reverse bias condition and the current flow is almost zero.

An MOS (Metal-oxide semiconductor) structure created by impress several layers of conducting and insulating materials to form a sandwich like structure. Structure are build using a series of chemical process steps involving oxidation of the silicon, the diffusion of impurities into silicon to give it certain conduction characteristic and lastly deposition and etching of metals to provide interconnection in the same way that a printed wiring board is constructed.

CMOS technology equip two type of transistor: an n-type transistor(nMOS)  and p-type transistor (pMOS). The operation of a transistor are based on electric fields. The cross section of  nMOS and pMOS are shown in **Figure 2.5a** and **Figure 2.5b**. Each transistor consists of conducting gate, silicon wafer that called as bulk, substrate or body and insulating layer of silicon dioxide ($SiO_2$ ). For nMOS  transistor it is built with a p-type body and has region of n-type semiconductor beside to the gate called the source and drain. The bulk is typically grounded. While a pMOS transistor opposite from nMOS construction, consisting of p-type source and drain regions with an n-type body.

 For an nMOS transistor operation, the body are grounded so the p-n junction of the source and drain to body operate in reversed bias. The gate acts as control input. It controls

the flow of electrical current between the source and drain. The gate is not grounded so the current can operate as mention above. So, the transistor are in OFF condition. For tune-up transistor so it is in ON condition, gate voltage is raised, so it create an electric filed that start to attract free electron to the side of Si-SiO$_2$ interface.. If the voltage raised enough, the electrons outside the holes and a thin region under the gate inverted to act as n-type semiconductor. A conducting path of electron carrier is formed from source to drain so the current can flow and the transistor is in ON condition.

pMOS transistor situation are against to nMOS operation. The bulk or body held at a high potential. When the gate is also at high potential, the source and drain junctions are reversed biased and no current flows so the transistor is OFF. When the voltage at gate is lowered, positive charge are attracted to the underside of Si-SiO2 interface. A sufficiently low gate voltage inverts the channel and a conducting path of positives carrier is formed from source to drain, so the transistor is in the ON condition.

2.5.1   Layout Design Rules

Layout design rules define how small features can be and how close it can be packed in particular manufacturing process. Usually, industrial design rules specified in microns. Mead and Conway[5] invented lambda-based design rules based on a single parameter, $\lambda$, which characterizes the resolution of the process. $\lambda$ is half from minimum drawn transistor channel length. This length is the distance between source and drain of a transistor and is set by the minimum width of polysilicon wire.