CHAPTER 1

INTRODUCTION

1.0 Semiconductor Technology

Many important semiconductor technologies have been derived from process invented centuries ago. For example, the lithography process was invented in 1798; in this first process, the pattern, or image, was transferred from a stone plate (litho). In this section, consider the milestones of technologies that were applied for the first time to semiconductor processing or developed specifically for semiconductor-device fabrication [1].

The diffusion of impurity atom in semiconductors is important for device processing. The basic diffusion theory was considered by Fick in 1855. The idea of using diffusion technique to alter the type of conductivity in silicon was disclosed in a patent in 1952 by Pfann [1]. In 1958, Shockley proposed the method of using ion implantation to dope the semiconductors. Ion implantation has the capability of precisely controlling the number of implanted dopant atoms. Diffusion and ion implantation can complement each other for impurity doping. For example, diffusion can be used for high-temperature, depth-junction process, whereas ion implantation can be used for lower-temperature, shallow-junction process [1].

As the complexity of the IC increased, we have moved from NMOS (n-channel MOSFET) to CMOS (complementary MOSFET) technology, which employs both NMOS and PMOS (p-channel MOSFET) to form the logic elements. The CMOS concept was

proposed by Wanlass and Sah in1963[1]. The advantages of CMOS technology is that logic elements draw significant current only during the transition from one state to another and draw very little current between transitions allowing power consumption to be minimized. CMOS technology is the dominant technology for advanced ICs [1].

A silicon bipolar junction transistor (BJT) is a type of transistor. It is a three-terminal device constructed of doped semiconductor material and may be used in amplifying or switching applications. Bipolar transistors n-p-n / p-n-p are so named because their operation involves both electrons and holes. Although a small part of the base–emitter current is carried by the majority carriers, the main current is carried by minority carriers in the base and so bipolar junction transistor are classified as 'minority-carrier' devices [1].

An NPN transistor can be considered as two diodes with a shared anode region. In typical operation, the emitter–base junction is forward biased and the base–collector junction is reverse biased. In an NPN transistor, for example, when a positive voltage is applied to the base–emitter junction, the equilibrium between thermally generated carriers and the repelling electric field of the depletion region becomes unbalanced, allowing thermally excited electrons to inject into the base region. These electrons wander (or "diffuse") through the base from the region of high concentration near the emitter towards the region of low concentration near the collector. The electrons in the base are called minority carriers because the base is doped p-type which would make holes as the majority carrier in the base [2, 1].

The base region of the transistor must be made thin, so that carriers can diffuse across it in much less time than the semiconductor's minority carrier lifetime, to minimize the percentage of carriers that recombine before reaching the collector–base junction. The collector–base junction is reverse-biased, so little electron injection occurs from the collector to the base, but electrons that diffuse through the base towards the collector are swept into the collector by the electric field in the depletion region of the collector–base junction [2, 1].

1.1 Process Ion Implantation And Diffusion

The process that involved in the project is ion implantation and diffusion that cause significantly phenomenon such as boron thermal diffusion and boron transient enhanced diffusion. Ion implantation is an adding process by which dopant atoms are forcefully added into the form of energetic ion beam injection. It is dominant doping method in the semiconductor industry and is commonly used for various doping process in integrated circuit fabrication. The ion implantation provides much better control of doping than the diffusion process. Ion implantation process can independently control both dopant concentration and junction depth. Dopant concentration can be controlled by the combination of ion beam current and implantation time, and junction depth can be control by the ion energy. The main application for ion implantation is doping the semiconductor substrate. A silicon wafer needs to be doped to change its conductivity in designated areas to form junctions, such as wells and source/drain for CMOS IC [3].

Further more, when the process ion implantation, the behavior and interaction of interstitial and vacancies also need to be investigate. The definition of interstitial is atom in the crystal lattice located in between lattice atoms. The definition of the vacancy is point defect in crystalline solids; a missing atom in single crystal lattice; also know as Schottky defect [2].

The diffusion is the physical phenomenon that material moves from high concentration region to low concentration region, driven by thermal motion of the molecules. Diffusion process happens anywhere and anytime. Perfume is a good example of diffusion in air, sugar, salt and ink of diffusion in liquid; wood soaking in water or oil of diffusion in a solid. Diffusion doping process was widely used in the early years of the IC industry. By introducing high concentration of dopant on the silicon surface with high temperature, dopants can be diffuse into the silicon substrate, which change the conductivity of the semiconductor. Compared with the ion implantation doping process, the diffusion process cannot control the dopant concentration and junction depth. Diffusion is an isotropic process, thus, when used in small feature size, it can cause the neighboring

junction short. Therefore, the ion implantation now is mostly replacing the diffusion process for small device [3]

Transient enhanced diffusion (TED) effect observed during post-implantation annealing; due to the crystal damage resulting from implantation the diffusion coefficient of implanted atoms increases temporarily up to 10 times. Boron transient enhanced diffusion (TED) is characterized by enhanced tail diffusion coupled with an electrically inactive immobile peak associated with the clustering of boron in the presence of excess interstitials. The transient enhanced diffusion (TED) of dopants in silicon is a central issue in silicon device processing because (TED) is a limiting factor for shallow junction formation. It is generally accepted that the large super saturation of silicon self-interstitials produced by ion implantation damage causes (TED). The transient enhanced diffusion (TED) of ion implanted boron in silicon is a major problem in the fabrication of ultra shallow junctions for advanced integrated circuits. It is now well established that boron diffuses by a kick-out mechanism in silicon. During the post-implantation annealing, the transient enhanced diffusion will occur and it may increase the junction depth. In addition, high concentration boron will lead to boron clustering and boron precipitation, which reduce electrical activation [1]. A more detailed and explicit discussion on the theories involved will be given in chapter 2.

1.2 Research Background

Over the past few years there has been considerable interest in the effect of fluorine on boron diffusion in silicon [4]. This research has been motivated by the requirement in advanced CMOS technologies to minimize boron diffusion for the formation of shallow source/drain junctions and sharply defined halo profiles [4]. The minimization of boron diffusion is also important in bipolar transistors, where boron diffusion limits the achievable base width and hence the value of cutoff frequency that can be obtained [5]. The suppression of boron diffusion is difficult to achieve in practice because of both boron

thermal diffusion and boron transient enhanced diffusion due to damage created during ion implantation. Work on the effects of fluorine from a BF_2^+ implant showed that shallower junctions could be obtained when BF_2^+ was implanted instead of B^+ [5].

The work showed that the fluorine implant reduced boron transient enhanced diffusion and increased boron activity [5]. However, there have also been contradictory reports in the literature, which showed that fluorine implants had little or no effect on boron transient enhanced diffusion and that fluorine enhanced boron diffusion in preamorphized silicon using a silicon implant [4]. Recently El Mubarek and Ashburn showed that a deep F^+ implants significantly reduced boron thermal diffusion, as well as eliminating transient enhanced diffusion [4].

Fluorine has long been used as a co-implant in BF_2^+ implant to produce shallower junctions in silicon transistors. More recently, it has been used as a countermeasure to reduce boron transient enhanced diffusion (TED) and boron thermal diffusion, which is necessary for a continued aggressive scaling of transistors. It has also been reported in the literature that fluorine can improve the threshold voltage roll-off characteristics in PMOS transistors when introduced in the source/drain extension region and also produce a super sharp halo profile in NMOS transistors [6]. Such promising results have increased the need to understand the mechanism by which fluorine reduces boron diffusion. Vacancy–fluorine clusters, fluorine–silicon interstitial interactions and boron–fluorine reactions have been proposed as the mechanisms by which fluorine reduces boron diffusion [6].

Several alternative mechanisms have been proposed to explain the effect of the fluorine on both boron transient enhanced diffusion and boron thermal diffusion in silicon. A chemical interaction between boron and fluorine has been proposed to explain the suppression of boron transient enhanced diffusion by fluorine in which the fluorine combines with interstitial boron reducing its mobility or reduces the probability of formation of a boron interstitial pair [5]. Alternatively, the formation of vacancy-fluorine complexes has been proposed which act as a barrier for boron diffusion or suppress the interstitial concentration and hence reduce boron transient enhanced diffusion and thermal

diffusion [5]. Finally the interaction of fluorine with silicon interstitials has been widely proposed as a mechanism of suppressing boron transient enhanced diffusion .In this paper, experiments are performed to investigate and modeling of Boron diffusion reduction in silicon and by Fluorine Implantation Using Numerical Simulation.

The minimization of boron diffusion is important in bipolar junction transistor, where boron diffusion limits the achievable base width and hence the value of cutoff frequency that can be obtained. The suppression of boron diffusion is difficult to achieve in practice because of boron thermal diffusion and boron transient enhanced diffusion due to damage created during implantation. Reduction of boron diffusion in silicon that permits the realization of shallow junction in bipolar and CMOS transistor would benefit the fabrication of high performance device [4].

The objective of this project is to investigate the reduction of both the boron thermal diffusion and transient enhanced diffusion in silicon by fluorine implantation at the silicon surface. The Monte Carlo Method used extensively by generating special structure in the process simulation. Both boron thermal diffusion and transient enhanced diffusion are also will be modeled. Further more, the reduction of boron thermal diffusion in silicon that permit the realization of the shallow junction in bipolar transistor and CMOS transistors would benefit the fabrication of high performance devices. It is expected that reduction of boron diffusion can be achieved when fluorine is implanted at the surface, then also hoped that this work would proof the utilization of fluorine as interstitial sink that reduce boron thermal diffusion.

This report is organized in five chapters. Chapter 1 will simply brief about the objective, scope of study, theory involved, background of problem and project background. Chapter 2 will discuss about the literature review about the fluorine implantation on boron reduction in silicon, the transient enhanced diffusion (TED) and boron thermal diffusion reduction when the fluorine implantation is used. Chapter 3 will discuss about the methodology of the project and the step to precede the project by using the Taurus TSUPREM 4 TCAD tool. Next, chapter 4 will discuss about the results obtained related to

the project and finally chapter 5 will discuss about the conclusion and summarize of the research project followed by business plan and the recommendation of the future project.