# CHAPTER 3

METHODOLOGY

The previous chapter reviewed on the operational amplifier and its modes and parameters. The fundamentals of two stages CMOS operational amplifier is also surveyed and analyzed. In this chapter, the method to design the two stages CMOS operational amplifier according to design objective is discussed.

3.1   Design Approach

Figure 3.1 is the block diagram about the project flow of the CMOS operational amplifier design. The design system consists of 4 stages.
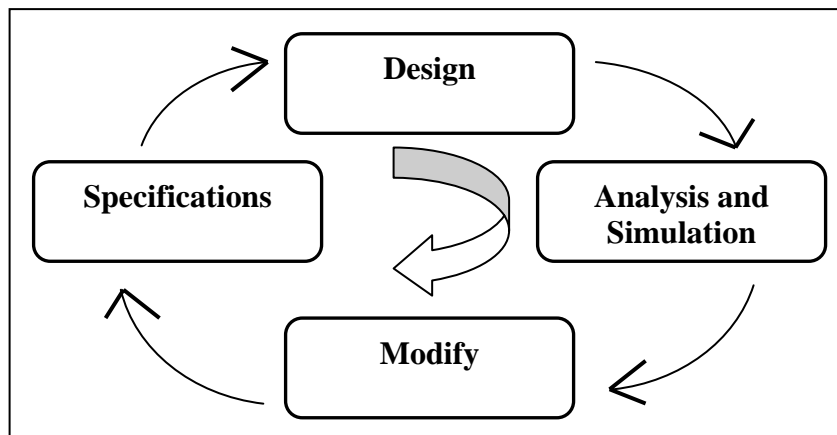
Figure 3.1: The Block Diagram for the Design System.

The first stage is the design process of CMOS operational amplifier. The design process involves two distinct activities, architecture design and component design. In architecture design, available architecture based on theories of advanced analog circuit design is founded and adapted to present requirements. After that, new architecture has been created in order to meet the requirements of design objectives. Once a satisfactory architecture has been obtained, component is designed. For component design, first of all, the transistor sizes were designed followed by compensation network.

In the second stage, the analysis and simulation of CMOS operational amplifier is done. The complete schematic is implemented in Mentor Graphics design architecture station employing $0.35\mu m$ technology. The DC analysis is done to determine the transistor drain currents. Using the drain current VGS, gm and gds is determined, where VGS is gate to source voltage, gm is transconductance and gds is drain to source transconductance. Next offset voltage, dc gain, output swing, common mode input range and power dissipation parameters were measured.

In the third stage, modification was done to CMOS operational amplifier schematic. The redesign is necessary to meet the requirements of design objectives. For example, initially the load capacitance was assumed to be 0.44pF, which had to be later adjusted in order to meet the slew rate specifications.

In the final stage, analysis was done to simulation results to compare the simulated results with the two stages CMOS operational amplifier design specifications. The comparison is tabulated and the discussion of its design performance is done and concluded.

3.2   Design Schematic

The CMOS operational amplifier circuit shown in Figure 3.2, in general, is a low power, moderate gain and fast settling time operational amplifier architecture consisting of three stages. The first stage provides of the biasing circuitry for the amplifier. The bias current sets the gate voltage of transistor M8, and this gate voltage is used as a gate bias voltage for the transistor current sources, M5 and M7, which bias the second and third stages of the amplifier.
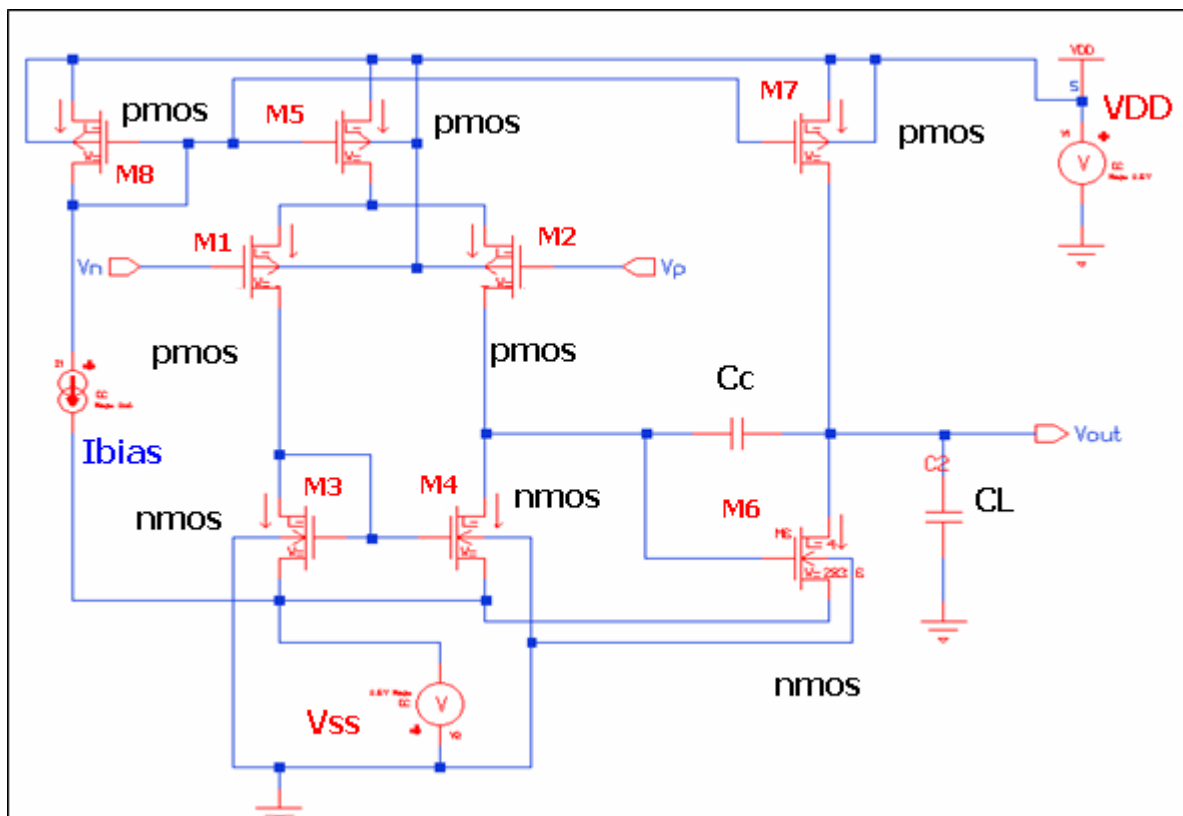
Figure 3.2: The schematic design for the CMOS operational amplifier.

The last stage is the second gain stage and consists of transistors M6 and M7. The NMOS transistor M6 is the driver with M7 acting as the load. Again, the high output

resistances of these two transistors equate to a relatively large gain for this stage and an overall moderate gain for the complete amplifier.

The large gain of the last stage is further utilized in the compensation of the amplifier via the capacitance Cc. Without compensation, the op-amp will oscillate in feedback circuits with a high loop gain. By taking advantage of the Miller Effect and the high resistance at the drain of M2, a smaller value for the capacitance Cc is used than would be needed otherwise.

The three stages of the amplifier and its compensation circuitry provide a stable, moderate gain, low power and fast settling time monolithic CMOS operational amplifier. The following sections discuss the design of this amplifier, the constraints for the design, the simulation and performance results, and a discussion of the overall amplifier.

3.3   Design Objective

The design objective is to design a two stage CMOS operational amplifier to meet the following specifications. The specifications referred from Joseph A. Potkay "CMOS Operational Amplifier Design Project" EECS 413, December 15th , 2000.

1) Open Loop gain > 10 000

2) GBW > 50 MHz

3) Power Supply = +/- 2.5V

4) Load Capacitance = 2 pF

5) Slew Rate >= 20V/uS

6) Output Range > +/- 2.2V

7) Input CMR > +/- 1.75V

8) Power dissipation 250uW or less

3.4   Design

The CMOS operational amplifier consists of two stages, the differential amplifier stage and common source amplifier. All the transistors assumed to be symmetrical. The basic relationship used in the designing process is discussed in this section.

DC Gain:

Total DC gain is equal to the product of 2 gain stages and is given by:

$$\frac{vo}{vi} = \frac{g_{m2} \times g_{m6}}{(g_{ds2} + g_{ds4}) \times (g_{ds6} + g_{ds7})} = \frac{\sqrt{k_p \times 2k_n}}{(\lambda 2 + \lambda 4) \times (\lambda 6 + \lambda 7)} \times \frac{\sqrt{(\frac{W}{L})_2 \times (\frac{W}{L})6}}{\sqrt{I_{D5} \times I_{D7}}} \qquad (3.0)$$

Given the design specification of 85dB and using the minimum L=0.8um to minimize capacitance, this reduces to the following:

$$\frac{(\frac{W}{L})_2 \times (\frac{W}{L})_6}{I_{D5} \times I_{D7}} \geq 15.44 X 10^{12} A^{-2} \qquad (3.1)$$

Where g_m =   transconductance.

g_{ds} =   transconductance drain to source.

λ =   channel length modulation parameter.

k_p =   pmos transconductance parameter (in saturation).

I_D =   drain current.

Common-Mode Input Range:

The negative common mode input range is given by:

$$CMR^- = V_{GS3} + |V_{DSAT1}| - |V_{GS1}| = \sqrt{\frac{I_{D5}}{k_n(\frac{W}{L})_3}} \leq 0.75V \quad \text{or,} \quad \frac{I_{D5}}{(\frac{W}{L})_3} \leq 32.4 \times 10^{-6} \quad (3.2)$$

The positive common mode input range is given by:

$$CMR^+ = |V_{DSAT5}| + |V_{GS2}| = \sqrt{\frac{2I_{D5}}{k_p(\frac{W}{L})_5}} + \sqrt{\frac{I_{D5}}{k_p(\frac{W}{L})_2}} + Vto \leq 0.75, \text{ or} \quad (3.3)$$

$$\sqrt{\frac{2I_{D5}}{(\frac{W}{L})_5}} + \sqrt{\frac{I_{D5}}{(\frac{W}{L})_2}} \leq 380 \times 10^{-6} A^{1/2} \quad (3.4)$$

Where 　　　V_{DSAT5} 　=　 drain saturation voltage.

　　　　　　　V_{GS} 　=　 gate to source voltage.

Output Swing:

The calculation to determine the positive and negative output voltage swing is as follows:

$$Vout^+ = |V_{DSAT7}| = \sqrt{\frac{2I_{D7}}{k_p(\frac{W}{L})_7}} \leq 0.3 \quad \text{or,} \quad \frac{I_{D7}}{(\frac{W}{L})_7} \leq 2.6 \times 10^{-6} A \quad (3.5)$$

$$Vout^- = |V_{DSAT6}| = \sqrt{\frac{2I_{D7}}{k_n(\frac{W}{L})6}} \leq 0.3 \quad \text{or,} \quad \frac{I_{D7}}{(\frac{W}{L})6} \leq 5.7 \times 10^{-6} A \quad (3.6)$$

Power Dissipation:

The total power dissipation of circuit follows the following relationship:

$$(I_{D8} + I_{D5} + I_{D7})*(V_{DD}-V_{SS}) \le 250uW, \tag{3.7}$$

The total power dissipation should be 250uW or less.

Unity Gain Frequency:

The unity gain frequency is given by:

$$fu = \frac{g_{m2}}{2\pi C_C} = \frac{\sqrt{I_{D5}k_p(\frac{W}{L})_2}}{2\pi C_C} \ge 50MHz \text{, or, } \frac{\sqrt{I_{D5}(\frac{W}{L})_2}}{C_C} \ge 41.4\times10^9 A^{1/2}F^{-1} \tag{3.8}$$

        Where fu =   unity gain frequency.

                                 C_C =   compensation capacitor.

The unity gain frequency should be $50MHz$ or more.

3.5   Design steps

The design technique is started using the specification given for load capacitance C_L. The value of the compensating capacitance assumed to be greater than C_L (2.2/10) to get phase margin greater than 60°.

$$Cc \geq C_L \times (\frac{2.2}{10}) = 10\,pF \times 0.22 = 0.44\,pF$$

We take the value of Cc to be $0.44\,pF$.

Using the relationship for slew rate current I_5 calculated.

$$SR = \frac{I_5}{Cc} \tag{3.9}$$

$$I_5 = SR \times Cc = 20 \times 10^6 \times 0.4 \times 10^{-12} = 8\,\mu A$$

I_5 assumed to be $= 8\,\mu A$.

Hence we get $I_1 = I_2 = I_3 = I_4 = \frac{I_5}{2} = 4\,\mu A$.

Using the formula for GBW, $gm2$ calculated.

$$GBW = \frac{gm2}{Cc} \tag{3.10}$$

$$gm2 = GBW \times Cc$$
$$= 85 \times 10^6 \times 2\pi \times 0.4 \times 10^{-12}$$
$$= 213.628 \times 10^{-6} V\,/\,A$$

Using the values for $gm2$ and I_2 we calculate the widths of transistors M1 and M2 using the general formula for gm,

$$gm = \sqrt{2 \times kp \times W/L \times I_D}$$ (3.11)

W/L=82.5

Using the value of $gm2$ and I_2 we obtain W = 66um

W1 = W2 = 66um

Now the widths of transistors M3, M4, M5 are obtained using the input CMR value in such a way that the none of the transistor goes into saturation for the given conditions. The condition that the transistor does not go into saturation is that $V_{DS} > V_{GS} - V_T$.

For negative CMR the width of M5 is adjusted such that

-ve CMR = $(V_{GS} - V_T)_5 + V_{GS2} - 2.5$

The V_{GS} of the transistor is obtained using the relation:

$$I_{D2} = \frac{1}{2} \times kp \times \frac{W}{L}(V_{GS} - V_{TH})^2$$ (3.12)

Using this relation $V_{GS2} = 0.728$ V.

The given –ve CMR is –1.75V , but to give some margin for simulation we assume it to be -2V for design purpose.

-2 = $(V_{GS} - V_T)_5 + 0.728 - 2.5$
$(V_{GS} - V_T)_5 = 0.228$ V .

Using this value of $(V_{GS} - V_T)_5$ and the value of I_5 in the current equation we calculate the width of transistor M5.

$$I_{D5} = \frac{1}{2} \times kp \times \frac{W}{L}(V_{GS} - V_{TH})^2 \tag{3.13}$$

The width is, W5 = 15um

Similarly for +ve CMR = 1.75 V width of M3 and M4 is obtained in such a way that none of the two go into saturation.

+ve CMR = 2.5 – $(V_{GS} - V_T)_4$

$(V_{GS} - V_T)_4 = 0.75$ V.

Using this value of $(V_{GS} - V_T)_4$ and the current I4 in the current equation we obtain the width of M4. This width is obtained as 12um. So we take the width of M4 as 12µm. As M3 and M4 are matched W3 =W4.

W3 = W4 = 12um

Thus we have obtained the widths of all the transistors of the first stage.

For second stage we assume the current I_7 is assumed to be $4 \times I_5$ since we assumed C_c to be $(\frac{1}{4.5})$ of C_L to maintain the slew rate.

$I_7 = 32\mu A$

The output swing of the amplifier is used to determine the widths of the transistors M6 and M7. Also the width of the transistor M6 is to be adjusted so as to adjust the W/L ratios with transistor M8 so as to give the required current.

For negative output swing the width of M7 is adjusted so that it does not go out of saturation.

$$-ve\ V_O = (V_{GS} - V_T)_7 - 2.5$$

The given output swing is –2.2 V but assuming it to be –2.25 V, about 0.5 V more than the specification we calculate $(V_{GS} - V_T)_7$.

$$(V_{GS} - V_T)_7 = 0.25\ V.$$

Using this value and the current I7 in the current equation we calculate the width of transistor M7. This width has to be adjusted according to the W/L and the current ratios of the transistor M8, which is the current source. Let the current at M8 = 8 μA. (For minimum power consumption). Now from the expression:

$$I_{D5} = I_{D8} \frac{(\frac{W}{L})5}{(\frac{W}{L})8} \tag{3.14}$$

Using this we get the width of M8 as:

W8 = 15um

Using this W8 we calculate the width of M7 is calculated again and found out to be

W7 = 52um

For this width again the $(V_{GS} - V_T)_7$ is calculated to obtain the output swing and verify it is as per the specifications.

$$(V_{GS} - V_T)_7 = 0.25\ V$$
$$V_O = 0.25 - 2.5$$
$$= -2.25\ V.$$

For +ve output swing the width of M6 is adjusted so that it does not go out of saturation. Assuming the output swing to be 2.25V we get $(V_{GS} - V_T)_6 = 0.25$ V. Using this value and the value of current I_6 in the current equation we calculate the width of M6.

W6 =64um

Thus we have obtained the widths of all the transistors. All these values are summarized in the table 1.0 below:

Table 1.0: Transistor values and drain current summary

Transistor	W/L (um/um)	I_D (uA)
M1	66/0.8	4.060
M2	66/0.8	4.060
M3	12/0.8	4.060
M4	12/0.8	4.060
M5	15/0.8	8.111
M6	64/0.8	28.000
M7	54/0.8	28.000
M8	15/0.8	8.000

Complete circuit:

Figure 3.3 shows the complete schematic design of the CMOS operational amplifier with the transistors width and length values.
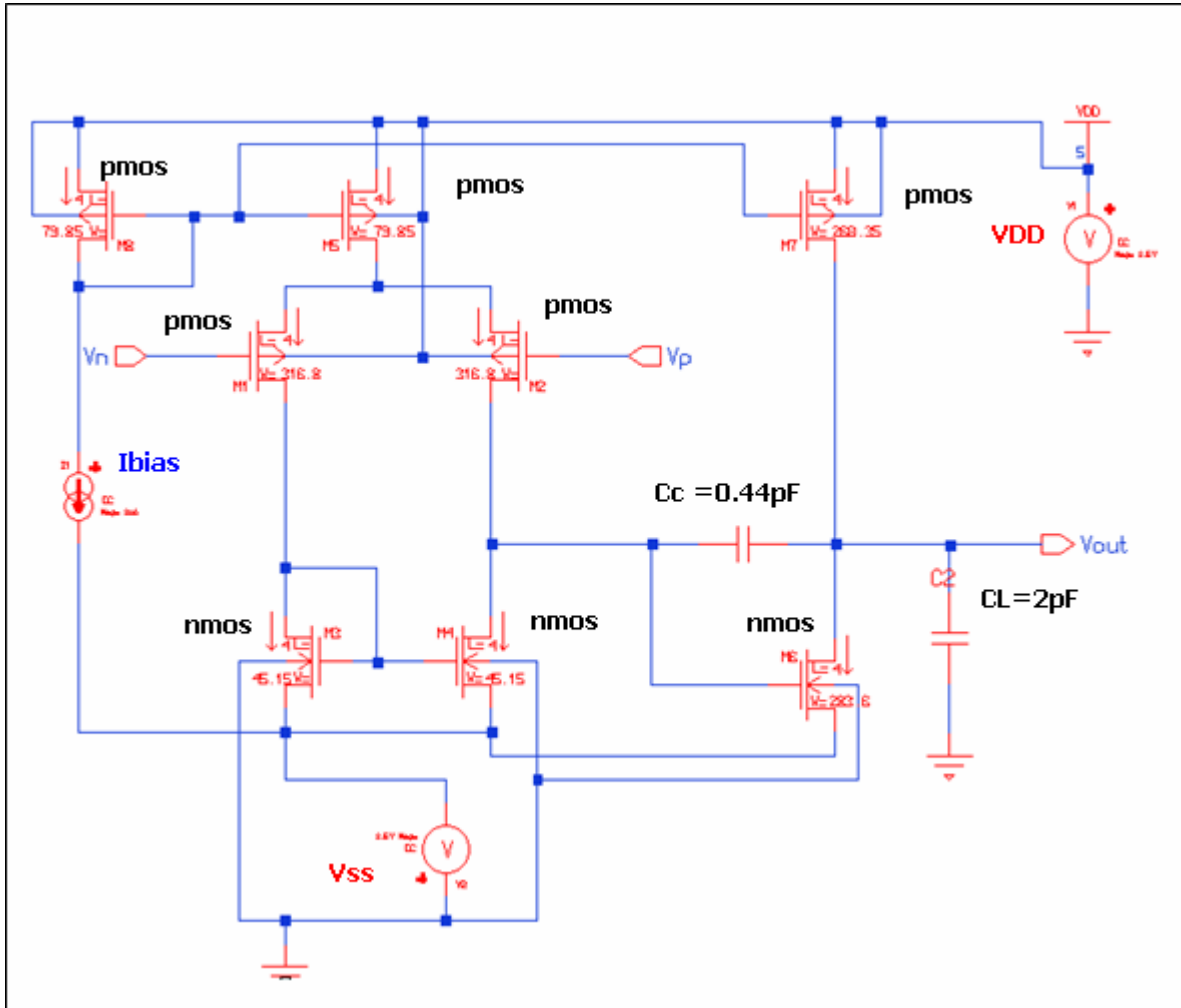
Figure 3.3: The complete schematic design for the CMOS operational amplifier.