

## **CHAPTER 1**

### **INTRODUCTION**

In this chapter; historical background, project overview and objectives will be reviewed. The historical background is reviewed about technology of semiconductor; project overview is reviewed about project flow and the objective of this project is about mainly the outcome for this project.

#### **1.1 Historical Background**

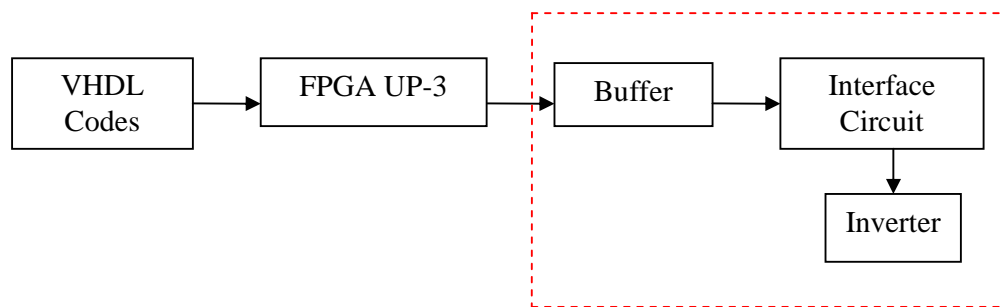
The applications of Very Large Scale Integration (VLSI) are getting more important and popular. Recently, microcontroller is widely used in industry and the application of this VLSI chip extended in many applications especially as the main controller for various types of controller circuit. Additionally, with the advance of power electronics technology, solid state devices such as relays and many more are replaced by the high speed power semiconductor switches. This introduced to the digital controller to replace the existing analog controller mostly in switches controlled devices.

The inverter circuit is one application of it. The inverter is desired to produce purely sine wave of the output voltage with less harmonics contents. The growth of power switches with high speed capability and the availability of the VHSIC Hardware Description Language (VHDL) coding to produce proper design of the control signal with high flexibility introduced to the used of Quartus II in this project as the controller for the

single phase full bridge inverter. Proper designs of control signal with powerful switches are very important in order to reduce the harmonics contents of the inverter output voltage. This approach hopefully will replace the existing analog controller due to its ability to produce precise control, low overall system cost, lower power dissipation and resulting longer life of operation.

## 1.2 Project overview

The flow chart as shown in Figure 1.1 illustrated the overview of this project. It consists of four stages including the development of the software and hardware of the control circuit



**Figure 1.1:** Project Overview

At the first stage for VHDL codes, the switching pulse is designed based on theories and the Quartus II software environment. In the next stage, the FPGA (Field Programmable Gate Array) technology by using the UP3 board as main controller had used to download the design that had done before. Next stage is to develop of the controller circuit. The controller circuit consists of the buffer, interface circuit and inverter. The buffer had used to provide improved noise rejections, interface circuit used

to increase the voltage from the buffer and inverter used as switching to get output both of positive and negative parts like as the design. Development of the control circuit is done after the generated signal from the main controller is simulated and downloaded. Each stages of the circuit design are tested through experiments. The testing for overall circuit is done and the output signal from the control circuit is compared with the calculation and theories.

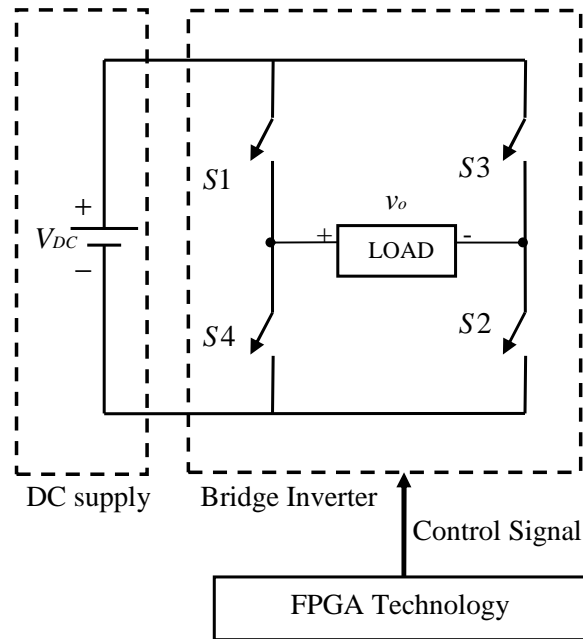
### **1.3 Objectives**

The objective of this project is mainly to develop the control circuit using FPGA technology as the main controller for a single phase full bridge inverter. The main objectives of the task undertaken were:

- 1.3.1 To design the control circuit for the bridge inverter switching.
- 1.3.2 To program the suitable pulse switching using the FPGA UP-3 Board.
- 1.3.3 To test and investigate the result of the control circuit.

## 1.4 Introduction

The basic block diagram of the full bridge single phase inverter with its control circuit is shown in Figure 1.2.



**Figure 1.2:** Basic block diagram of the bridge inverter with control circuit.

The input supply is a fixed DC supply used as the inverter input. The next stage is the analogy of the bridge inverter circuit. It is represented by four switches connected in a bridge connection. It is an electronic power converter that is necessary to convert the dc input voltage into an ac form of output voltage with magnitude and frequency controllable. The control circuit is used to generate the control signal which is used to control the inverter switches. It consists of a FPGA (Field Programmable Gate Array) technology by using Quartus II software, buffer and the interface circuit to generate the control signal to be used as a controller for a single phase full bridge inverter switches.

In this project, the input dc voltage is fixed at a certain value. The sinusoidal pulse width modulation control is used to control the inverter switches using FPGA (Field Programmable Gate Array) technology. Practical inverters normally produce the non-sinusoidal waveform and contain certain harmonics. This problem may be acceptable for low and medium power applications such as for an AC motor drive, where the filtering stage is not required. In some applications such as for designing the uninterruptible power supplies (UPS), high purity sine wave output is required. An L-C section filter is normally fitted at the inverter output to reduce the high frequency harmonics.

## **1.5 Thesis Organization**

This thesis is organized into five chapters as follows.

Chapter 2 discusses the literature survey about the FPGA (Field Programmable Gate Array) and on the theories of an inverter switching scheme.

Chapter 3 presents the design of the control circuit include software design and the control circuit design needed to generate the control signal for inverter switches. The inverter switching frequency is design and then downloaded into UP-3 Board using VHDL programming. The control circuit is designed and tested stage by stage before being used as the inverter control circuit.

Chapter 4 discussed the simulation and experimental results include the results of inverter test using the generated control signal. The discussion for each stage is done and concluded.

Chapter 5 outlines the conclusion and future works. Conclusion for the overall research findings especially on the control circuit is done and the suggestion for the future works is also stated.