CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Overview

This chapter provides results obtained from the experimental and an analytical and subjective approach had applied on discussion session to obtain a better understanding behind the experimental and also compare the theoretical and practical results.

4.2 Analysis

Referring to previous objective, these schematics are focus to two part of analysis included current analysis and voltage analysis.

4.2.1 Current Analysis

Thus, the results provide that using cascade technique and differential pair technique it can drive the VCO circuit that needed at least 3.3V to operate. Which I_{BIAS} is 2 times than the I_{REF} with waveform is stable mode.

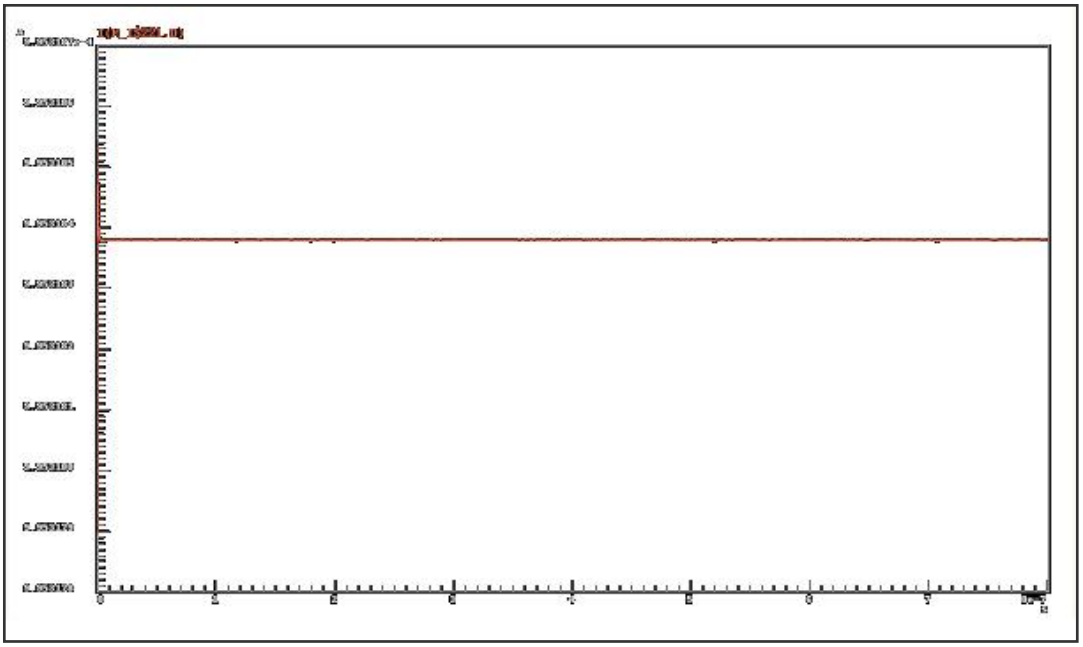

Figure 4.1 : Biasing Current

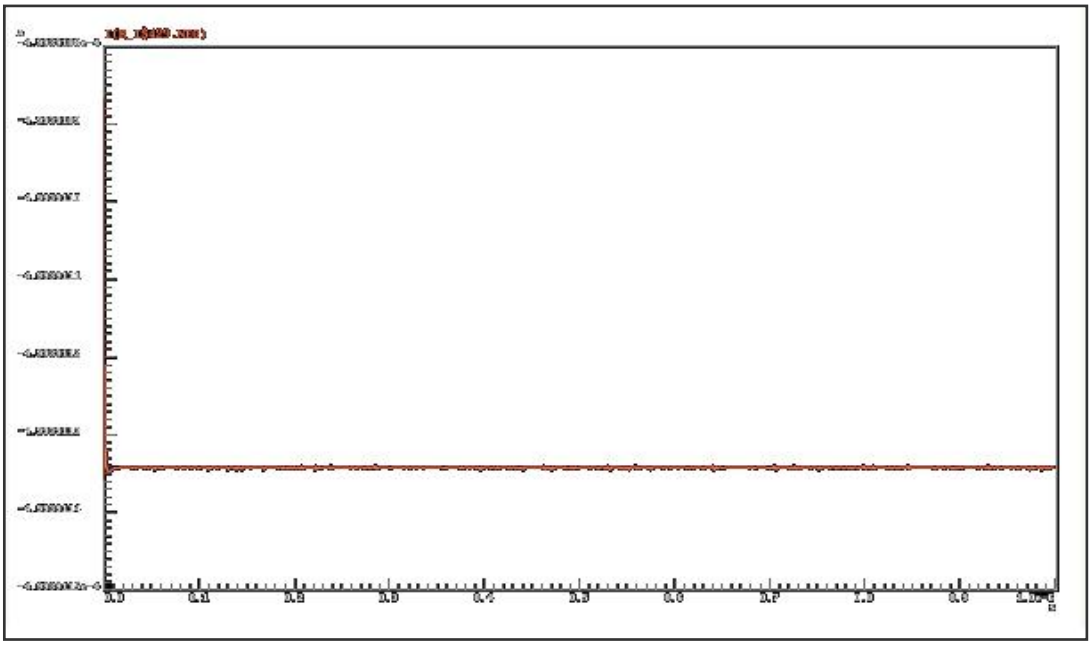

Figure 4.2: Biasing Current divide by two

From the figure (4.1 and, 4.2), the waveform present the biasing current for voltage supply 3.3V. According to the objective, value between calculation and measuring are not same. It is because he value at calculation is just guideline value in saturation mode that been use in tuning during designing schematic. Therefoe the value different are very small. The tuning at V_{DD} 3.3V and I_{REF} 0.6mA can produced the 0.258mA $I_{BIAS,}$, the tuning have control the $V_{GS} = V_{IN.}$ Practically I_{BIAS} = 0.6mA and I_D = 0.50mA thus I_{BIAS} nearly value I_D. Overall tuning this circuit mostly focus to get the smooth wavesharp of VCO, $I_{REF} = ½I_{BIAS}$ and also the same time the current are in stable condition not in unconditionally mode.

4.2.2 Voltage and Frequency Analysis

Analyze the voltage by changing the size of NMOS until the value of voltage 3.3V has been reach to get the 2.0GMHz frequency.

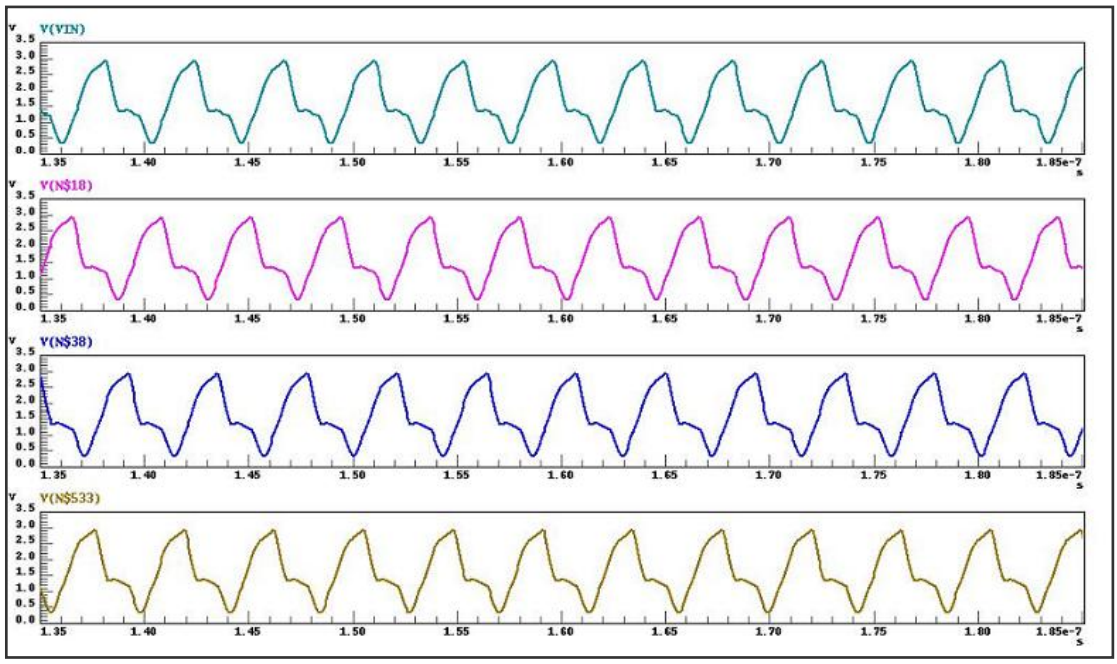

Figure 4.3 : Output Voltage

From figure 4.3,to get the smooth and fulfill the objective 3.3V voltage supply and tuning the frequency. Tuning the frequency by calculation to get the value of one cycle periodic to get the time. Thus, for VOUT – 3.3V frequency are 2.0MHZ, times is 5.02ns. using equation F=1/T for calculate the frequency.

4.3 Layout Result

Referring to figure 4.4, the layouts have been complete design thus using metal1 and metal2 for connection in the layout base on schematic figure 3.2. This schematic is performing to input supply.

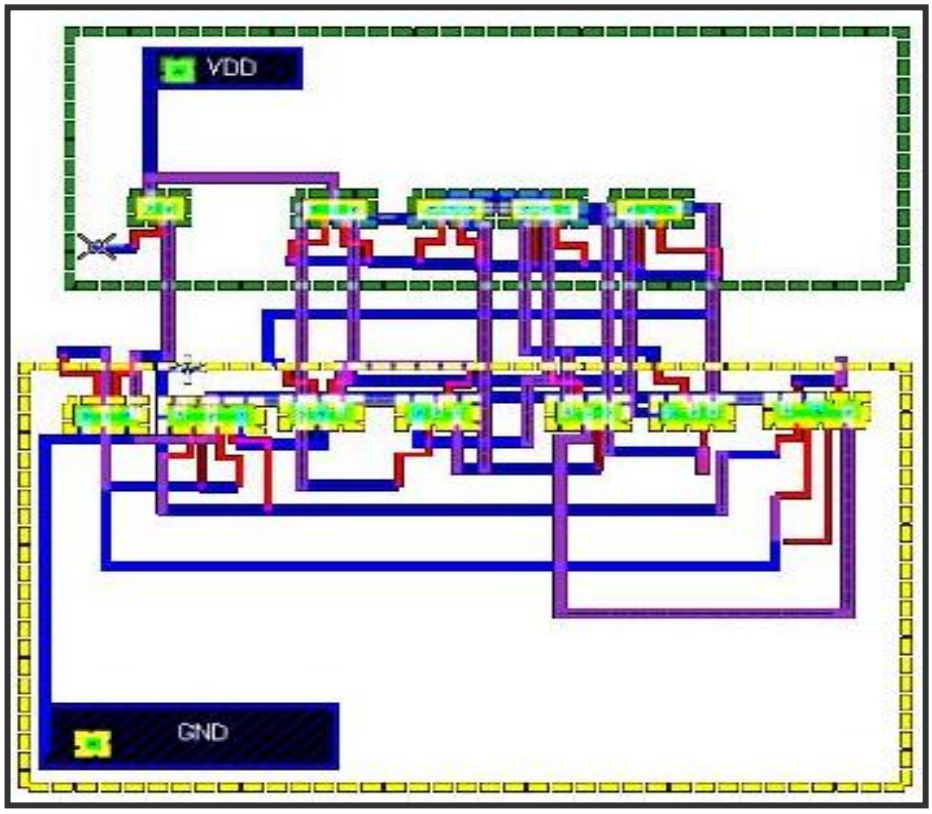

Figure 4.4: Shows the layout result

According to the layout, there have an Nwell and a Pwell area. Circuit has supplied by 3.3V voltage. Practically, this layout are using metal3 and metal4 but using manually technique only metal1 and metal2 are used. Comparing using autoroute technique the manually technique is better because it can reduce applications of metal.

4.4 Layout versus Schematic (LVS) Result

Referring to figure 4.5 is the result of the LVS design is matching. This figure show that the design is matching between the schematic and netlist layout as shown table (4.1). Both netlist, schematic and layout must same each other before result is successful. The results of the layout are base on the connection and also name port based on schematic. The results come out as figure 4.5.

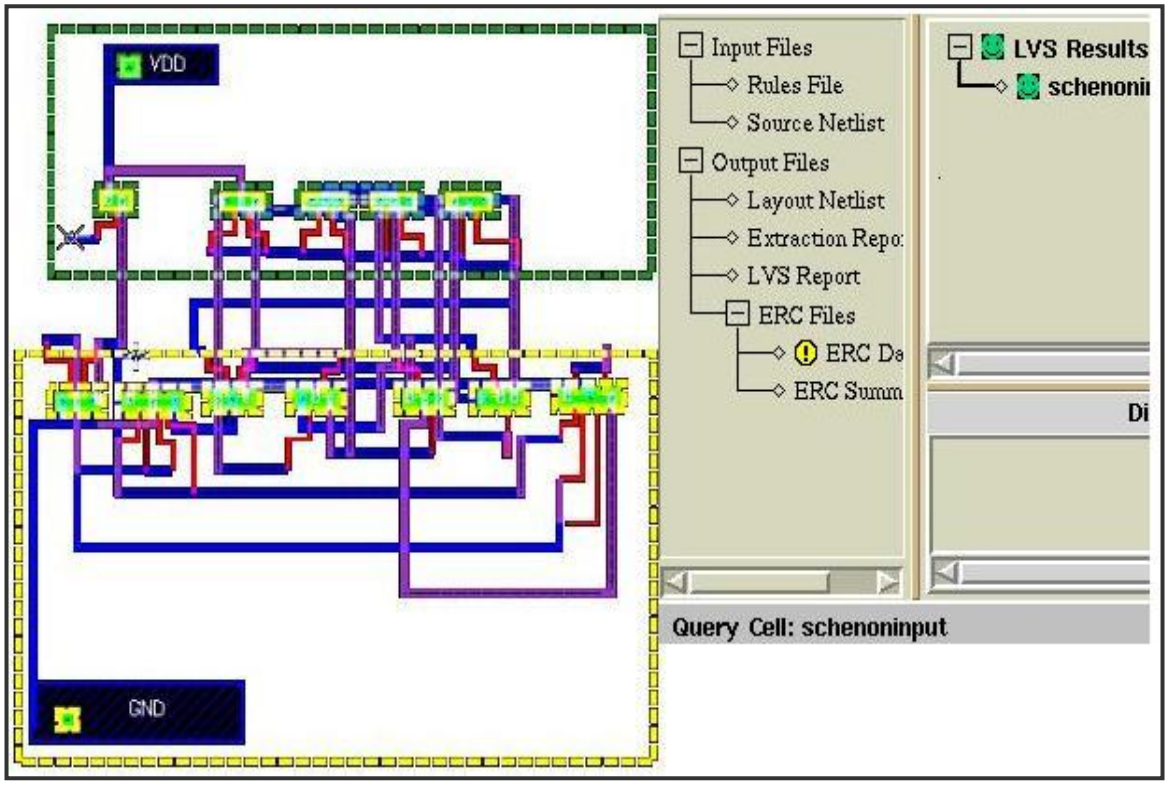

Figure 4.5 : LVS layout result

Table 4.1: Netlist for layout.

1. **NETLIST (Layout)**

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* SPICE NETLIST
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.SUBCKT ver21 Vout GND VinA VinB VDD
** N=49 EP=5 IP=0 FDC=27
M0 15 VinB VDD VDD p L=5e-07 W=5e-06 AD=5.5e-12 AS=5.5e-12 $X=-2718200 $Y=-51400
M1 VDD VinA 6 VDD p L=5e-07 W=5e-06 AD=6e-12 AS=5.5e-12 $X=-2735200 $Y=4700
M2 4 VinA VDD VDD p L=5e-07 W=5e-06 AD=5.5e-12 AS=6e-12 $X=-2735200 $Y=13200
M3 VDD VinA 9 VDD p L=5e-07 W=5e-06 AD=6e-12 AS=5.5e-12 $X=-2734800 $Y=51450
M4 8 VinA VDD VDD p L=5e-07 W=5e-06 AD=5.5e-12 AS=6e-12 $X=-2734800 $Y=59950
M5 VDD VinA 1 VDD p L=5e-07 W=5e-06 AD=6e-12 AS=5.5e-12 $X=-2734800 $Y=98350
M6 2 VinA VDD VDD p L=5e-07 W=5e-06 AD=5.5e-12 AS=6e-12 $X=-2734800 $Y=106850
M7 VDD VinA Vout VDD p L=5e-07 W=5e-06 AD=6e-12 AS=5.5e-12 $X=-2734450 $Y=146650
M8 3 VinA VDD VDD p L=5e-07 W=5e-06 AD=5.5e-12 AS=6e-12 $X=-2734450 $Y=155150
M9 46 15 5 GND n L=5e-07 W=4e-05 AD=2.4e-11 AS=4.4e-11 $X=-2662650 $Y=-55750
M10 GND 11 46 GND n L=5e-07 W=4e-05 AD=4.8e-11 AS=2.4e-11 $X=-2662650 $Y=-50250
M11 47 11 GND GND n L=5e-07 W=4e-05 AD=2.4e-11 AS=4.8e-11 $X=-2662650 $Y=-41750
M12 7 15 47 GND n L=5e-07 W=4e-05 AD=4.4e-11 AS=2.4e-11 $X=-2662650 $Y=-36250
M13 48 15 14 GND n L=5e-07 W=4e-05 AD=2.4e-11 AS=4.4e-11 $X=-2433950 $Y=-56850
M14 GND 11 48 GND n L=5e-07 W=4e-05 AD=4.8e-11 AS=2.4e-11 $X=-2433950 $Y=-51350
M15 49 11 GND GND n L=5e-07 W=4e-05 AD=2.4e-11 AS=4.8e-11 $X=-2433950 $Y=-42850
M16 13 15 49 GND n L=5e-07 W=4e-05 AD=4.4e-11 AS=2.4e-11 $X=-2433950 $Y=-37350
M17 11 11 GND GND n L=5e-07 W=2e-05 AD=2.4e-11 AS=2.2e-11 $X=-2214700 $Y=-51350
M18 15 15 11 GND n L=5e-07 W=2e-05 AD=2.2e-11 AS=2.4e-11 $X=-2214700 $Y=-42850
M19 13 3 6 GND n L=5e-07 W=0.0001136 AD=1.3632e-10 AS=1.2466e-10 $X=-2664450 $Y=144850
M20 4 Vout 13 GND n L=5e-07 W=0.0001136 AD=1.2466e-10 AS=1.3632e-10 $X=-2664450
$Y=153350
M21 5 1 Vout GND n L=5e-07 W=0.0001136 AD=1.3632e-10 AS=1.2466e-10 $X=-2663000 $Y=3250
M22 3 2 5 GND n L=5e-07 W=0.0001136 AD=1.2466e-10 AS=1.3632e-10 $X=-2663000 $Y=11750
M23 7 9 1 GND n L=5e-07 W=0.0001136 AD=1.3632e-10 AS=1.2466e-10 $X=-2662850 $Y=50200
M24 2 8 7 GND n L=5e-07 W=0.0001136 AD=1.2466e-10 AS=1.3632e-10 $X=-2662850 $Y=58700
M25 14 6 9 GND n L=5e-07 W=0.0001136 AD=1.3632e-10 AS=1.2466e-10 $X=-2662550 $Y=99400
M26 8 4 14 GND n L=5e-07 W=0.0001136 AD=1.2466e-10 AS=1.3632e-10 $X=-2662550 $Y=107900
.ENDS
**************************************
```

4.5 Design Rules Check (DRC) Result

Referring to figure 4.6, this figure tells the result of ‘design rule check (DRC)’ at this case, the DRC result was successfully. The region of “Nwell must be well contact.”. This is the rules that must follow before the design want to fabricate and for this case the bulk and the V_{DD} is well connected to each other.So, the DRC can accept the specification and it can simulate easily without major problems. For the DRC, it just a rule that can be modified using another technique that can create the designing at fabrication field.

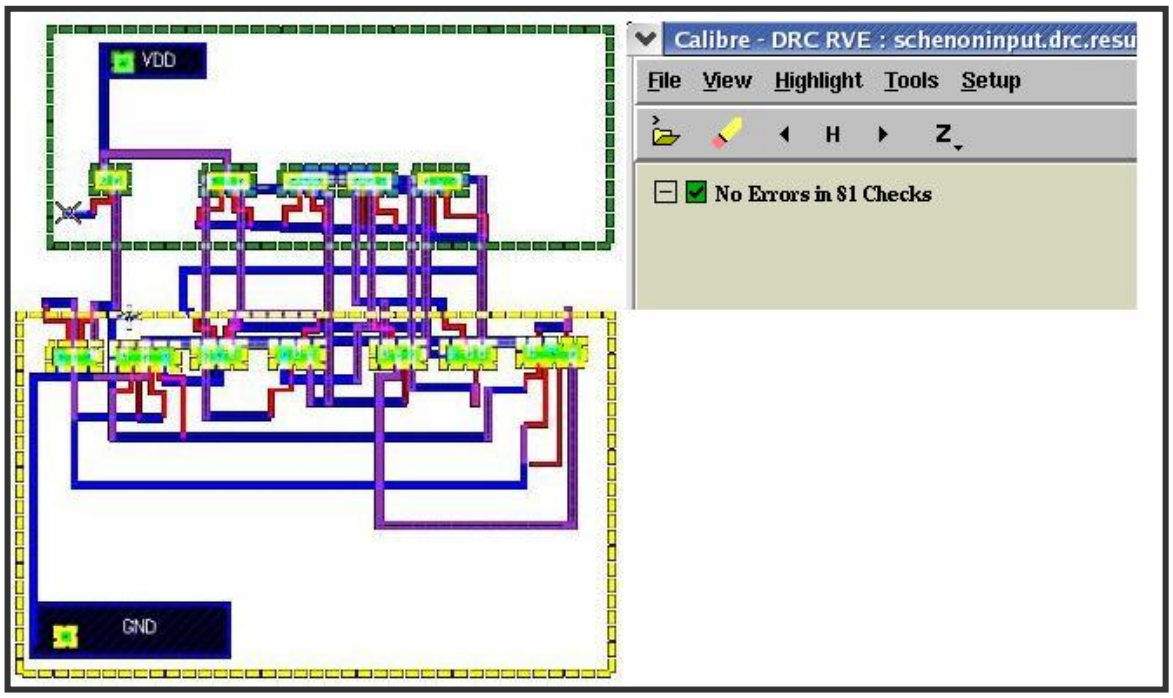

Figure 4.6: Shows the DRC layout result.

All the DRC report and LVS report as shown in appendix C.