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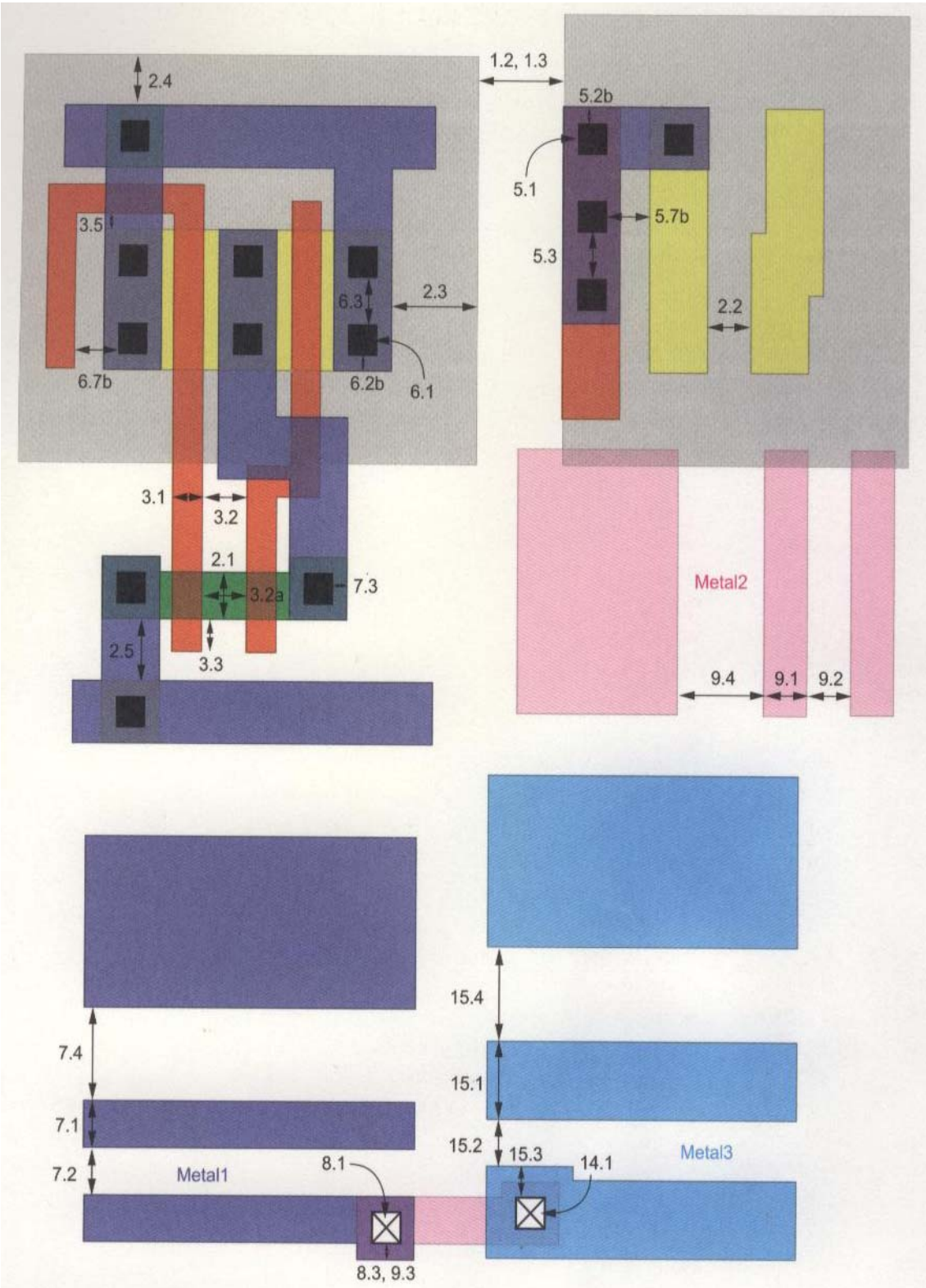
APPENDIXS

Appendix A (i).



Illustrated MOSIS design rules

Appendix A (ii).

Layer	Rule	Description	90 nm rule (μm)
Well	1.1	Width	0.75
	1.2	Spacing to well at different potential	1.5
	1.3	Spacing to well at same potential	1.0
Active (diffusion)	2.1	Width	0.15
	2.2	Spacing to active	0.20
	2.3	Source/drain surround by well	0.25
	2.4	Substrate/well contact surround by well	0.25
	2.5	Spacing to active of opposite type	0.30
Poly	3.1	Width	0.09
	3.2	Spacing to poly over field oxide	0.15
	3.2a	Spacing to poly over active	0.15
	3.3	Gate extension beyond active	0.15
	3.4	Active extension beyond poly	0.15
	3.5	Spacing of poly to active	0.10
Select	4.1	Spacing from substrate/well contact to gate	0.25
	4.2	Overlap of active	0.20
	4.3	Overlap of substrate/well contact	0.10
	4.4	Spacing to select	0.30
Contact (to poly or active)	5.1, 6.1	Width (exact)	0.12
	5.2b, 6.2b	Overlap by poly or active	0.01
	5.3, 6.3	Spacing to contact	0.15
	5.4	Spacing to gate	0.10
Metal1	7.1	Width	0.13
	7.2	Spacing to well metal1	0.13
	7.3, 8.3	Overlap of contact or via	0.01
	7.4	Spacing to metal for lines wider than 0.5 μm	0.40
Via1–Via5	8.1, 14.1, …	Width (exact)	0.13
	8.2, 14.2, …	Spacing to via on same layer	0.13

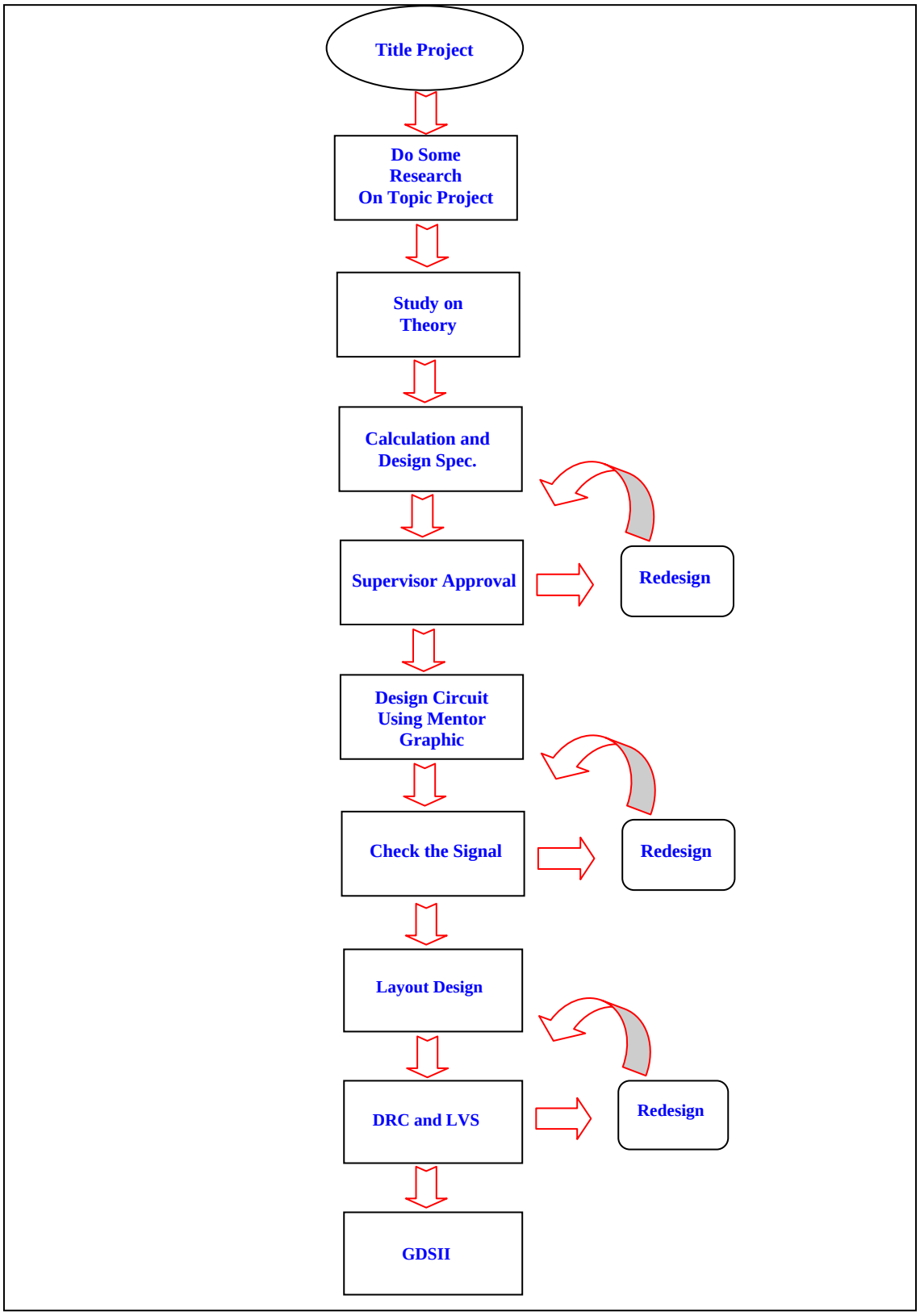
Table Mosis Design Rules (A)

Appendix A (iii).

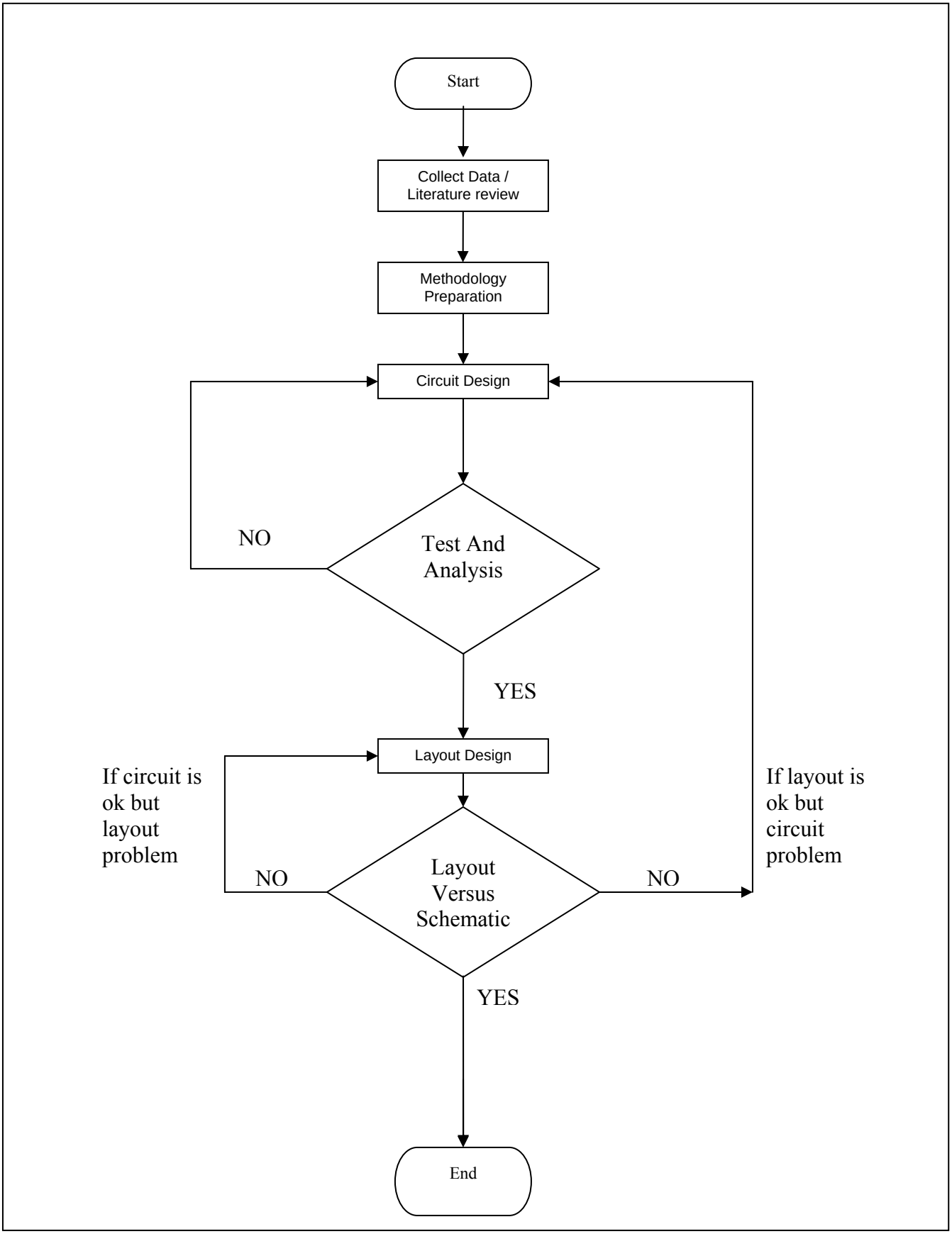
Abbreviated MOSIS design rules					
Layer	**Rule**	**Description**	**SCMOS**	**SUBM**	**DEEP**
Well	1.1	Width	10	12	12
	1.2	Spacing to well at different potential	9	18	18
	1.3	Spacing to well at same potential	6	6	6
Active (diffusion)	2.1	Width	3	3	3
	2.2	Spacing to active	3	3	3
	2.3	Source/drain surround by well	5	6	6
	2.4	Substrate/well contact surround by well	3	3	3
	2.5	Spacing to active of opposite type	4	4	4
Poly	3.1	Width	2	2	2
	3.2	Spacing to poly over field oxide	2	3	3
	3.2a	Spacing to poly over active	2	3	4
	3.3	Gate extension beyond active	2	2	2.5
	3.4	Active extension beyond poly	3	3	4
	3.5	Spacing of poly to active	1	1	1
Select	4.1	Spacing from substrate/well contact to gate	3	3	3
	4.2	Overlap of active	2	2	2
	4.3	Overlap of substrate/well contact	1	1	1.5
	4.4	Spacing to select	2	2	4
Contact (to poly or active)	5.1, 6.1	Width (exact)	2x2	2x2	2x2
	5.2b, 6.2b	Overlap by poly or active	1	1	1
	5.3, 6.3	Spacing to contact	2	3	4
	5.4, 6.4	Spacing to gate	2	2	2
	5.5b	Spacing of poly contact to other poly	4	5	5
	5.7b, 6.7b	Spacing to active/poly for multiple poly/active contacts	3	3	3
	6.8b	Spacing of active contact to poly contact	4	4	4
Metal1	7.1	Width	3	3	3
	7.2	Spacing to metal1	2	3	3
	7.3, 8.3	Overlap of contact or via	1	1	1
	7.4	Spacing to metal for lines wider than 10 λ	4	6	6
Via1–Via(*N*-1)	8.1, 14.1, …	Width (exact)	2x2	2x2	3x3
	8.2, 14.2, …	Spacing to via on same layer	3	3	3
	8.4	Spacing to contacts (if no stacked vias)	2	2	n/a
	8.5	Spacing of via1 to poly or active edge	2	2	n/a
	14.4	Spacing of via2 to via1 (if no stacked vias)	2	2	n/a
Metal2–Metal(*N*-1)	9.1, …	Width	3	3	3
	9.2, …	Spacing to same layer metal	3	3	4
	9.3, …	Overlap of via	1	1	1
	9.4, …	Spacing to metal for lines wider than 10 λ	6	6	8
Metal3 (3-layer process)	15.1	Width	6	5	n/a
	15.2	Spacing to metal3	4	3	n/a
	15.3	Overlap of via2	2	2	n/a
	15.4	Spacing to metal for lines wider than 10 λ	8	6	n/a

Table Mosis Design Rules (B)

Appendix B (i)


Title Project
Do Some Research On Topic Project
Study on Theory
Calculation and Design Spec.
Supervisor Approval
Redesign
Design Circuit Using Mentor Graphic
Check the Signal
Redesign
Layout Design
DRC and LVS
Redesign
GDSII

Appendix B (ii)



Appendix C (i)

```
================================================================================
===========
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:       Thu Mar  8 13:32:16 2007
Calibre Version:           v2004.3_9.21    Thu Sep 30 11:25:17 PDT 2004
Rule File Pathname:        /home/hafizun/layout/_tsmc035.rules_
Rule File Title:
Layout System:             GDS
Layout Path(s):            schenoninput_sce.calibre.gds
Layout Primary Cell:       schenoninput_sce
Current Directory:         /home/hafizun/layout
User Name:                 hafizun
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      schenoninput_sce.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       schenoninput_sce.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  OFFGRID = NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------------
-----------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
-----------
--- ORIGINAL LAYER STATISTICS
---
LAYER N_WELL ................. TOTAL Original Geometry Count = 2  (2)
LAYER POLY ................... TOTAL Original Geometry Count = 3  (3)
LAYER ACTIVE ................. TOTAL Original Geometry Count = 5  (5)
LAYER P_PLUS_SELECT .......... TOTAL Original Geometry Count = 3  (3)
LAYER N_PLUS_SELECT .......... TOTAL Original Geometry Count = 2  (2)
LAYER DIFFUSED_RESISTOR ...... TOTAL Original Geometry Count = 0  (0)
LAYER CONTACT_TO_ACTIVE ...... TOTAL Original Geometry Count = 10 (10)
LAYER HI_RES_IMPLANT ......... TOTAL Original Geometry Count = 0  (0)
LAYER ELECTRODE .............. TOTAL Original Geometry Count = 0  (0)
LAYER METAL1 ................. TOTAL Original Geometry Count = 6  (6)
LAYER CONTACT_TO_POLY ........ TOTAL Original Geometry Count = 3  (3)
LAYER CONTACT ................ TOTAL Original Geometry Count = 0  (0)
LAYER PADS ................... TOTAL Original Geometry Count = 0  (0)
LAYER VIA .................... TOTAL Original Geometry Count = 0  (0)
LAYER METAL2 ................. TOTAL Original Geometry Count = 0  (0)
LAYER CONTACT_TO_ELECTRODE ... TOTAL Original Geometry Count = 0  (0)
LAYER VIA2 ................... TOTAL Original Geometry Count = 0  (0)
LAYER METAL3 ................. TOTAL Original Geometry Count = 0  (0)
LAYER VIA3 ................... TOTAL Original Geometry Count = 0  (0)
LAYER METAL4 ................. TOTAL Original Geometry Count = 0  (0)
```

```
LAYER METAL1.PORT ............ TOTAL Original Geometry Count = 0  (0)
LAYER METAL2.PORT ............ TOTAL Original Geometry Count = 0  (0)
LAYER METAL3.PORT ............ TOTAL Original Geometry Count = 0  (0)
LAYER OVERGLASS .............. TOTAL Original Geometry Count = 0  (0)
LAYER METAL4.PORT ............ TOTAL Original Geometry Count = 0  (0)
---------------------------------------------------------------------------
-----------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK bad_active_area ......... TOTAL Result Count = 0 (0)
RULECHECK bad_contact_poly ........ TOTAL Result Count = 0 (0)
RULECHECK bad_contact_ELECTRODE ... TOTAL Result Count = 0 (0)
RULECHECK bad_contact_active ...... TOTAL Result Count = 0 (0)
RULECHECK bad_contact_gate ........ TOTAL Result Count = 0 (0)
RULECHECK bad_via ................. TOTAL Result Count = 0 (0)
RULECHECK bad_via2 ................ TOTAL Result Count = 0 (0)
RULECHECK bad_via3 ................ TOTAL Result Count = 0 (0)
RULECHECK select_overlap .......... TOTAL Result Count = 0 (0)
RULECHECK bad_nwell ............... TOTAL Result Count = 1 (1)
RULECHECK bad_psubstrate .......... TOTAL Result Count = 0 (0)
RULECHECK bad_pgate ............... TOTAL Result Count = 0 (0)
RULECHECK bad_ngate ............... TOTAL Result Count = 0 (0)
RULECHECK bad_port ................ TOTAL Result Count = 0 (0)
RULECHECK DRC1_1 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC1_2 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC2_1 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC2_2 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC2_3 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC2_4 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC3_1 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC3_2 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC3_3 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC3_4 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC3_5 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC4.1p ................. TOTAL Result Count = 0 (0)
RULECHECK DRC4.1n ................. TOTAL Result Count = 0 (0)
RULECHECK DRC4.2 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC4.3p ................. TOTAL Result Count = 0 (0)
RULECHECK DRC4.3n ................. TOTAL Result Count = 0 (0)
RULECHECK DRC4.4pw ................ TOTAL Result Count = 0 (0)
RULECHECK DRC4.4ps ................ TOTAL Result Count = 0 (0)
RULECHECK DRC4.4nw ................ TOTAL Result Count = 0 (0)
RULECHECK DRC4.4ns ................ TOTAL Result Count = 0 (0)
RULECHECK DRC4.4np ................ TOTAL Result Count = 0 (0)
RULECHECK DRC5_1 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC5_2 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC5_3 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC5_4 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC6_1 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC6_2 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC6_3 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC6_4 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC7_1 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC7_2 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC7_3 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC7_4 .................. TOTAL Result Count = 0 (0)
RULECHECK DRC8_1 .................. TOTAL Result Count = 0 (0)
```

```
RULECHECK DRC8_2 ................. TOTAL Result Count = 0 (0)
RULECHECK DRC8_3 ................. TOTAL Result Count = 0 (0)
RULECHECK DRC9_1 ................. TOTAL Result Count = 0 (0)
RULECHECK DRC9_2 ................. TOTAL Result Count = 0 (0)
RULECHECK DRC9_3 ................. TOTAL Result Count = 0 (0)
RULECHECK DRC9_4 ................. TOTAL Result Count = 0 (0)
RULECHECK DRC11_1 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC11_2 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC11_3 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC11_4 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC11_5 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC11_sel .............. TOTAL Result Count = 0 (0)
RULECHECK DRC12_1 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC12_2 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC13_1 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC13_2 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC13_3 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC13_4 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC13_5 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC14_1 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC14_2 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC14_3 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC15_1 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC15_2 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC15_3 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC15_4 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC21_1 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC21_2 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC21_3 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC22_1 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC22_2 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC22_3 ................ TOTAL Result Count = 0 (0)
RULECHECK DRC22_4 ................ TOTAL Result Count = 0 (0)
------------------------------------------------------------------------
-----------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
CELL schenoninput_input_sce ... TOTAL Result Count = 1 (1)
    RULECHECK bad_nwell .... TOTAL Result Count = 1 (1)
------------------------------------------------------------------------
-----------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 34 (34)
TOTAL DRC RuleChecks Executed:   81
TOTAL DRC Results Generated:     1 (1)
```

Appendix C (ii)

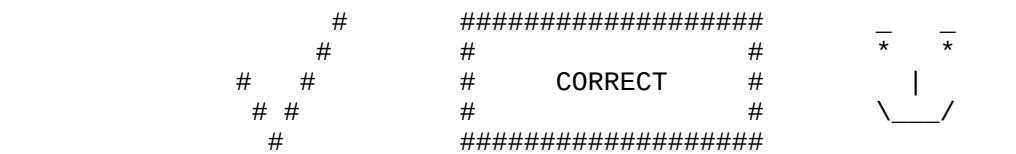
```
                ##################################################
                ##                                              ##
                ##         C A L I B R E    S Y S T E M         ##
                ##                                              ##
                ##             L V S   R E P O R T              ##
                ##                                              ##
                ##################################################


REPORT FILE NAME:         schenoninput_sce.lvs.report
LAYOUT NAME:              schenoninput_sce.lay.net ('schenoninput_sce')
SOURCE NAME:
/home/hafizun/schenoninput_sce/tsmc035a/schenoninput_sce_tsmc035a.spi
('joe_tanpa_input_sce')
RULE FILE:                /home/hafizun/layout/_tsmc035.rules_
CREATION TIME:            Thu Mar  8 13:31:19 2007
CURRENT DIRECTORY:        /home/hafizun/layout
USER NAME:                hafizun
CALIBRE VERSION:          v2004.3_9.21    Thu Sep 30 11:25:17 PDT 2004


                              OVERALL COMPARISON RESULTS


                          #       ###################       _   _
                         #        #                 #       *   *
                    #   #         #     CORRECT     #         |
                     # #          #                 #       \___/
                      #           ###################


*************************************************************************
************************************
                                    CELL  SUMMARY
*************************************************************************
************************************

  Result         Layout                      Source
  -----------    -----------                 --------------
  CORRECT        schenoninput_sce          schenoninput_SCE


*************************************************************************
************************************
                                    LVS PARAMETERS
*************************************************************************
************************************
```

o LVS Setup:

```
   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   // LVS POWER NAME
   // LVS GROUND NAME
   LVS RECOGNIZE GATES                    ALL
   LVS IGNORE PORTS                       NO
   LVS CHECK PORT NAMES                   NO
   LVS BUILTIN DEVICE PIN SWAP            YES
   LVS ALL CAPACITOR PINS SWAPPABLE       NO
   LVS DISCARD PINS BY DEVICE             NO
   LVS SOFT SUBSTRATE PINS                NO
   LVS INJECT LOGIC                       NO
   LVS EXPAND UNBALANCED CELLS            YES
   LVS EXPAND SEED PROMOTIONS             NO
   LVS PRESERVE PARAMETERIZED CELLS       NO
   LVS GLOBALS ARE PORTS                  YES
   LVS REVERSE WL                         NO
   LVS SPICE PREFER PINS                  NO
   LVS SPICE SLASH IS SPACE               YES
   LVS SPICE ALLOW FLOATING PINS          YES
   LVS SPICE ALLOW UNQUOTED STRINGS       NO
   LVS SPICE CONDITIONAL LDD              NO
   LVS SPICE CULL PRIMITIVE SUBCIRCUITS   NO
   LVS SPICE IMPLIED MOS AREA             NO
   // LVS SPICE MULTIPLIER NAME
   LVS SPICE OVERRIDE GLOBALS             NO
   LVS SPICE REDEFINE PARAM               NO
   LVS SPICE REPLICATE DEVICES            NO
   LVS SPICE STRICT WL                    NO
   // LVS SPICE OPTION
   LVS STRICT SUBTYPES                    NO
   LAYOUT CASE                            NO
   SOURCE CASE                            NO
   LVS COMPARE CASE                       NO
   LVS DOWNCASE DEVICE                    NO
   LVS REPORT MAXIMUM                     50
   LVS PROPERTY RESOLUTION MAXIMUM        32
   // LVS SIGNATURE MAXIMUM
   // LVS FILTER UNUSED OPTION
   // LVS REPORT OPTION
   LVS REPORT UNITS                       YES
   // LVS NON USER NAME PORT
   // LVS NON USER NAME NET
   // LVS NON USER NAME INSTANCE

   // Reduction

   LVS REDUCE SERIES MOS                  NO
   LVS REDUCE PARALLEL MOS                YES
   LVS REDUCE SEMI SERIES MOS             NO
   LVS REDUCE SPLIT GATES                 YES
   LVS REDUCE PARALLEL BIPOLAR            YES
   LVS REDUCE SERIES CAPACITORS           YES
   LVS REDUCE PARALLEL CAPACITORS         YES
```

```
   LVS REDUCE SERIES RESISTORS            YES
   LVS REDUCE PARALLEL RESISTORS          YES
   LVS REDUCE PARALLEL DIODES             YES

   // Filter

   LVS FILTER  sch_filter_direct_open  OPEN SOURCE DIRECT
   LVS FILTER  sch_filter_direct_short  SHORT SOURCE DIRECT
   LVS FILTER  sch_filter_mask_open  OPEN SOURCE MASK
   LVS FILTER  sch_filter_mask_short  SHORT SOURCE MASK
   LVS FILTER  lay_filter_direct_open  OPEN LAYOUT DIRECT
   LVS FILTER  lay_filter_direct_short  SHORT LAYOUT DIRECT
   LVS FILTER  v  OPEN
   LVS FILTER  i  OPEN
   LVS FILTER  e  OPEN
   LVS FILTER  f  OPEN
   LVS FILTER  g  OPEN
```

CELL COMPARISON RESULTS (TOP LEVEL)




```
LAYOUT CELL NAME:         schenoninput_sce
SOURCE CELL NAME:         SCHENONINPUT_SCE

------------------------------------------------------------------------
---------------------------------------

NUMBERS OF OBJECTS
------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              2         2

 Nets:               7         7

 Instances:          2         2         MN (4 pins)
                     3         3         MP (4 pins)
                ------    ------
 Total Inst:         5         5


************************************************************************
************************************
                              INFORMATION AND WARNINGS
```

```
*************************************************************************
*************************************

                  Matched    Matched    Unmatched    Unmatched
Component
                   Layout     Source       Layout       Source    Type
                  -------    -------    ---------    ---------    -----
----
   Ports:              2          2            0            0
   Nets:               7          7            0            0
   Instances:          2          2            0            0    MN(N)
                       3          3            0            0    MP(P)
                  -------    -------    ---------    ---------
   Total Inst:         5          5            0            0


o Initial Correspondence Points:

   Ports:        VDD GND


*************************************************************************
*************************************
                                      SUMMARY
*************************************************************************
*************************************

Total CPU Time:      0 sec
Total Elapsed Time:  0 sec
```