DESIGN OF VOLTAGE CONTROL OSCILLATOR (VCO) IN 0.18u CMOS

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by

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APPROVAL AND DECLARATION SHEET

This project report titled Design Voltage Control Oscillator (VCO) in 0.18u CMOS technology was prepared and submitted by Amier Hafizun b Ab. Rashid (Matrix Number: 031030037) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in Universiti Malaysia Perlis (UniMAP).

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MEREKA CIPTA PENGAWAL AYUNAN VOLTAN MENGGUNAKAN TEKNOLOGI 0.18u CMOS

ABSTRAK

Pengayun merupakan keperluan asas bagi kebanyakan sistem elektronik. Konsep asas bagi pengayun adalah ia mengeluarkan keluaran yang berkala tetap, biasanya dalam bentuk keluaran voltan. Pengawal ayunan voltan (VCO) di rekacipta menerusi teknik kasked dan teknik perubahan perbezaan mod asas Dengan pengukuran sehingga peringkat ke-4 pada frekuensi 2.0Ghz dan kuasa disipisi 20mW. Untuk projek tahun akhir ini, spesifikasi yang tertentu telah ditetapkan sebelum sesi makmal dimulakan agar spesifikasi ini boleh dijadikan panduan semasa merekacipta VCO. Antara spesifikasinya ialah frekuensi ditetapkan f_o=2.0GHz dan keluaran arus I_{BIAS} mestilah dua kali ganda bebanding I_{REF}.M3 dan M4 beroperasi dalam keadaan kawasan mendatar, setiap satunya berfungsi sebagai printang boleh ubah yang dikawal oleh V_{BIAS}. Sekiranya nilai Vbias lebih positif, nilai perintang pada M3 dan M4 akan meningkat, ini akan mengakibatkan nilai pemalar masa meningkat pada keluaran dan frekuensi osilator akan menurun. Keluaran VCO akan bersambung dengan masukan PMOS untuk mendapatkan nilai gelombang ayunan. Sebelum proses membina bentangan, perintang telah ditukar kepada transistor PMOS. Nilai kiraan bagi perintang telah dilakukan dan nilai lebar dan panjang juga telah ditentukan agar ia beroperasi seperti perintang. Rekaan dijalankan dengan menggunakan perisian mentor graphic. Bagi ujian dan menganalisa litar, senibina rekaan boleh mengesan kesemua parameter seperti arus, voltan dan kuasa.Seharusnya rekaan bagi hasil bentangan lawan litar (LVS), ianya lebih penting dari hasil pemastian peraturan rekaan (DRC).

ABSTRACT

This VCO are designated using cascade technique and differential common-mode change. The measured are 4 stages at 2.0GHz with power dissipation 20mWatt. For this final year project,mentor grahics software has use for design n simulate the circuit of VCO. VCO have a specification to approach to design a schematic n layout. The specification are the f_o=2.0GHz and the output of I_{bias} must have a double output than the $I_{bias}/2$. $I_{bias} \leq$ 1mA. To fulfill the specification, the value of length (L) and width (W) at NMOS M_1, M_2, M_5, M_6, M_9, M_{10}, M_{14} , and M_{15} and the value of resistor has been change. For example, the differential pair as one stage of ring oscillator has been considering. M_3 and M_4 operate in the triode regions, each acting as a variable resistor controlled by V_{bias} . As V_{bias} become more positive, the on resistance of M_3 and M_4 increases, thus raising the time constant of the output and lowering f_{osc} . The output of VCO will go through to the input of the PMOS to get the oscillation at the output waveform. To start design of VCO resistor has been changes to form of PMOS transistor. Calculation for PMOS transistor can be act as a resistor has been complete.In summary, the negative feedback circuit has a loop gain that satisfies two condition; $|H(j\omega o)| >= 1$ and $+ < H(j\omega o) = 180°$. The systems is then can be implemented in CMOS technologies which is called “Ring Oscillators”. To perform the design, the methods are using the mentor graphic software. This software provides design architecture software and IC design software. For testing and analyze circuit, design architecture can check all the parameter such as current, voltage and gain. Thus, actually for this designing the layout versus schematic (LVS) result is more important than design rule check (DRC) result.

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LIST OF ABBREVIATIONS

μn	Electron Mobility
μp	Hole Mobility
CM	Common-Mode
C_{OX}	Gate Oxide Capacitance per Unit Area
CMOS	Complimentary Metal-Oxide Semiconductor
DRC	Design Rules Check
G_{ND}	Ground
IC	Integrated Circuit
LOCOS	Local Oxidation of Silicon
LVCM	Low Voltage Current Mirror
LVS	Layout versus Schematic
MOS	Metal Oxide Semiconductor
NFET	Negative-Field Effect Transistor
NMOS	N-Metal Oxide Semiconductor
PMOS	P-Metal Oxide Semiconductor
SDL	Schematic Driven Layout
V_{DD}	Supply Voltage
V_{DS}	Drain/Source Voltage
V_{GS}	Gate/Source Voltage
V_{TH}	Threshold Voltage