CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

The core of every research work is about the results and findings. This chapter discusses the design and simulation of the source code and the hardware simulation. Designs are done using Altera Quartus II software while the hardware simulations are using Altera FPGA board on FLEX10K70 chip. The results are discussed either based on simulation or hardware simulation, or compared to each other to see the difference or similarity.

4.2 Source Code Design

The source code is written using Verilog in Quartus II software. The whole code is as in Appendix A. The module's top-level name is version_11, which indicates the eleventh version of the code. The earlier codes were expanded and have limited features, and version_11 is the final version of the code.

4.3 Source Code Simulation

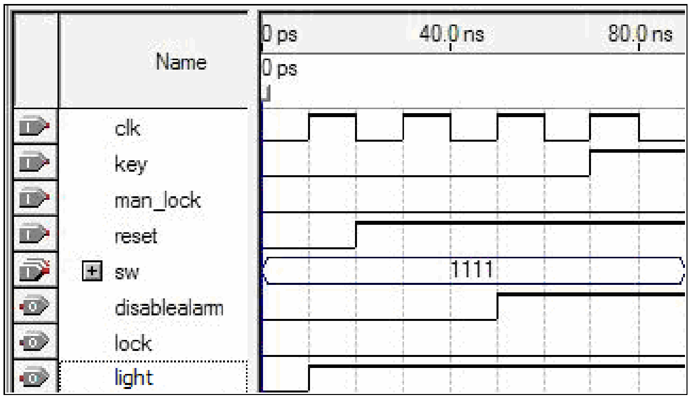

Figure 4.1 Reset and Initial Condition

As the program starts to operate, the outputs will be all Low or zero. Refer to Figure 4.1. The key is exist, thus its giving a Low signal to the input part of the system. As for the manual lock knob, the door is locked, thus driving the *man_lock* signal a Low to the input of the system. The reset button is pressed, thus giving a Low signal. During reset, display is “63”. Only at positive edge trigger, the light signal will be triggered to High. Right after the reset button is pressed, the system will check the condition of the key. This state requires a full clock cycle. Soon after that, the *disablealarm* signal will be disabled.

After the initial and reset of the system occurs, the key is unplugged. To do this, the key button (FLEX Switch 8) is released. The system will wait for input switch to be pressed. The *sw* signal is all 1s at the time since there are no keys pressed at the moment. Note that the pushbuttons are active low, where when they are pressed, it drives Low signal.

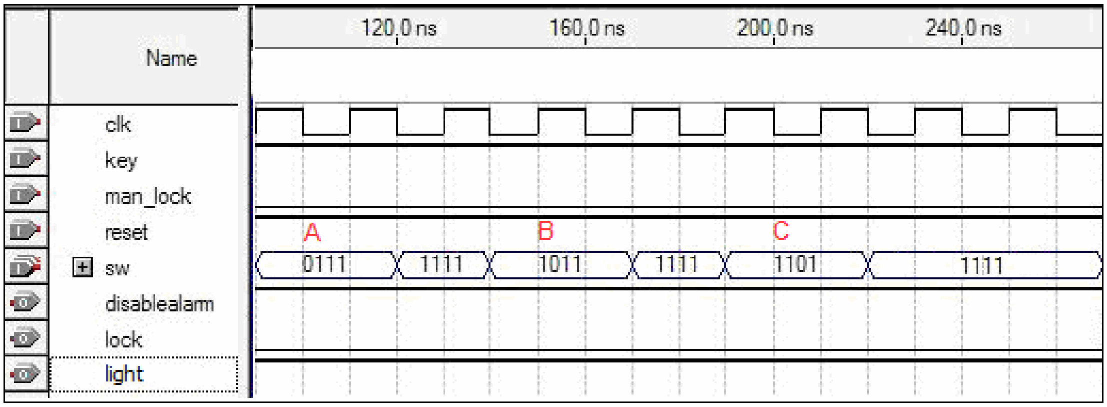

Figure 4.2 Entering Passkeys

Refer to Figure 4.2. As the system waits for user input on the pushbuttons, the seven segments will display “11”. This indicates current state is “waiting”. At the seconds before 120ns, the sw3 button or the A button is pressed. After that, it is released, and the system waits for the next button to be pressed. At this moment, the seven segments display “21”.

The next button pressed is B, where the sw2 button gives a Low signal. Following is button C is pressed. The sw1 signal will drive Low. Note that in Chapter 3, the pre-programmed passkey is A, B and C pressed in sequence. Here, the exact passkey has been entered. The system will determine the passkey by comparing it with the pre-programmed passkey.

The result is as in Figure 4.3. As the entered passkey is approved to be correct, the system will give an unlock signal to the door’s unlocking system, which is mechanically controlled. As the unlock signal goes High, the Lock LED will be turned off. At this rate, the seven segments display will light “32”. This indicates that the system is waiting until the manual lock knob is unlocked.

Note that the manual lock knob has a delay time after the system unlocks the door’s lock. This is due to the system has friction within its operation. Thus, until the door is fully unlocked, the system will wait until the manual lock signal is High or unlocked.

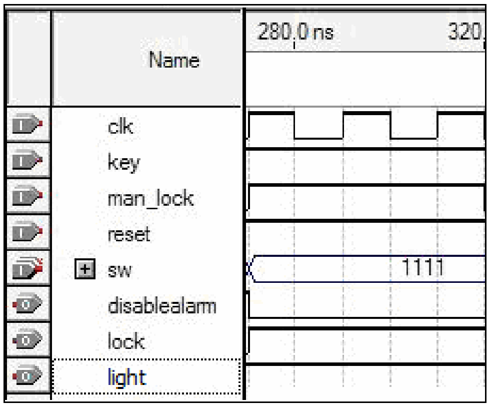

Figure 4.3 Unlocking Door

Upon the manual lock is High, from “zero” to “one” transition, the lock will be disabled. Its signal will be off. As the door is opened, the disarm alarm signal and light will be turned on, indicating the alarm will be disabled, while the light will be turned on. Both signals will be High at the moment. The seven segments display will be displaying “33”. It indicates that the system is waiting until the door is locked again.

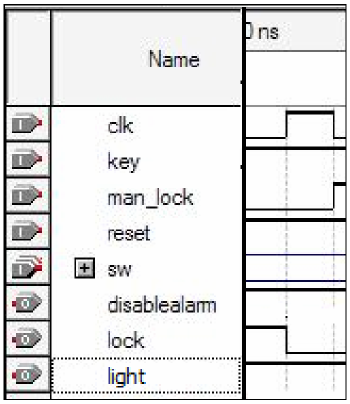

Figure 4.4 Locking Door

Upon locking the door, the system will automatically set the light off by giving it the High signal. The same goes to the disable alarm signal, where it will be turned off as the door is locked again. The system looks at the manual lock knob to see the locking status. This is due to the fact that when the door is properly locked, the manual lock knob will be lowered in position, which gives a Low signal to the system. Seven segments give “11” which indicates the system remains idle.

4.3.1 Source Code Simulation Summary

Up to this level, the system's source code shows the system is working as planned. The signals lights and turn off as it should be. The system is able to give access as the entered password is correct, and cancels as the entered password is false.. All requirements and conditions were met as planned. The system is working fine.

4.4 Hardware Simulation Result

Hardware simulation is based on results on the FPGA board. The methods were explained in Chapter 3. Following is the table showing the results of the hardware simulation. Shown here is the reset pressed condition.

Table 4.1 Initial Condition

	Pins	**Status**
INPUT	Key	No
	Reset	On
	Button A	Off
	Button B	Off
	Button C	Off
	Button D	Off
	Manual Lock	On
OUTPUT	Lock	On
	Disarm Alarm	Off
	Light	Off
	Display	63

The hardware diagram for Table is represented in Figure 4.5. The conditions of the inputs are as in the table.

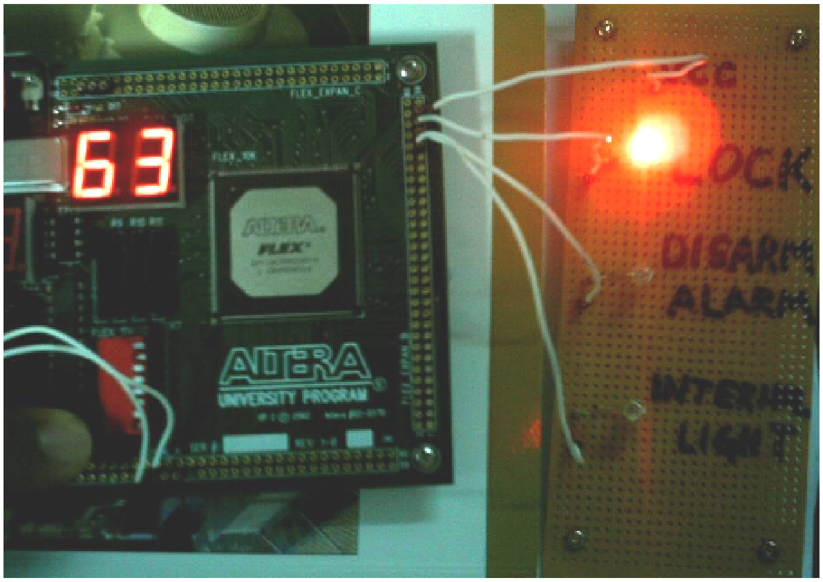

Figure 4.5 Initial Hardware Condition

Later, the system waits for input from user. The display shows "11". Refer to Figure 4.6.

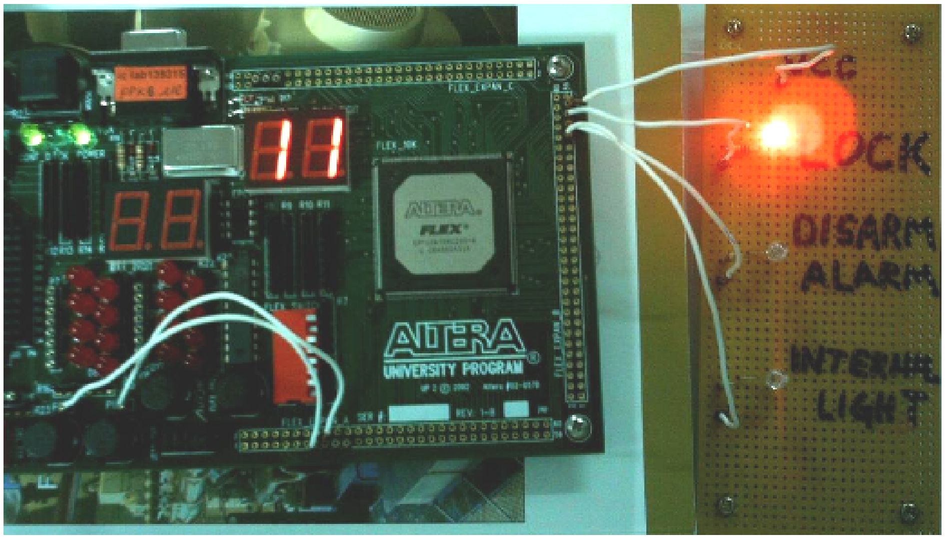

Figure 4.6 Idle Condition

As button A is pressed, the seven segments will display "21". Refer to Figure 4.7 for the diagram aid.

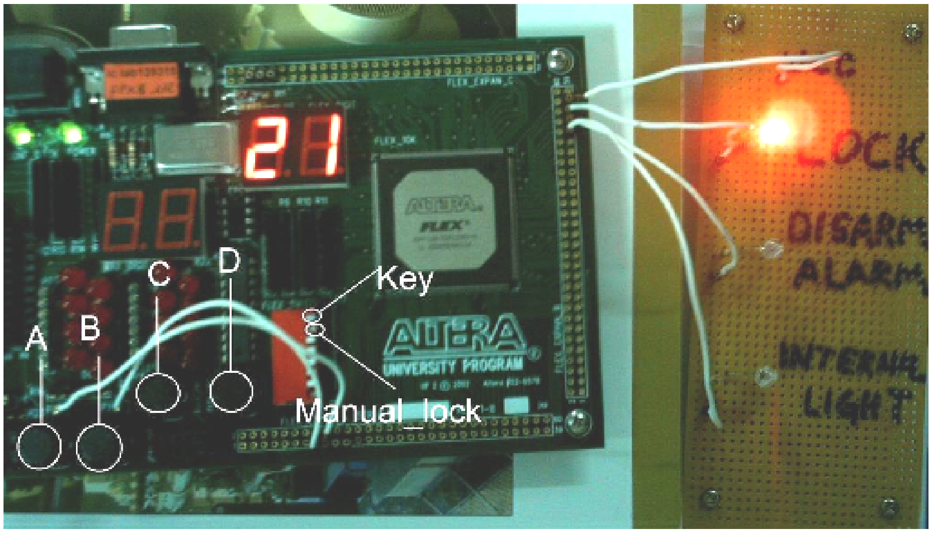

Figure 4.7 Button A Pressed and the Labeling.

As button B is pressed, the seven segments will display “23”. Refer to Figure 4.8 for the diagram aid.

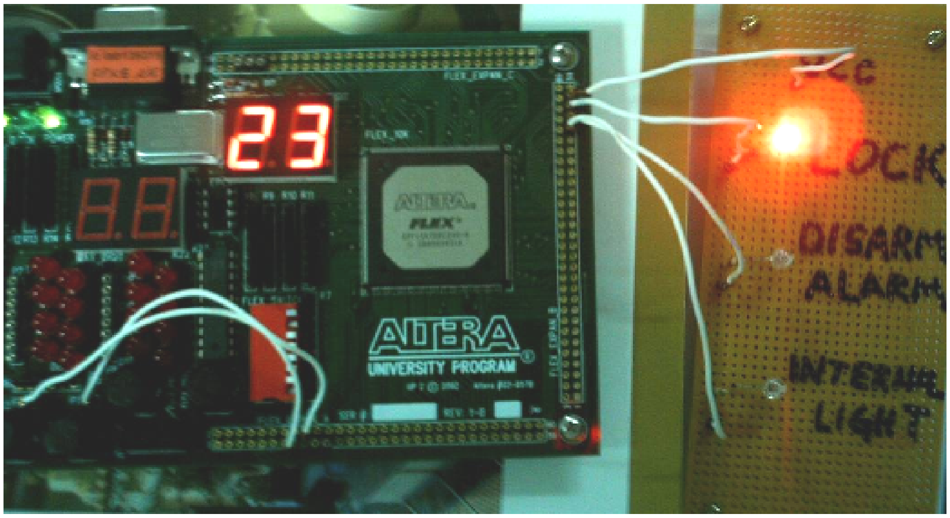

Figure 4.8 Button B Pressed.

As button C is pressed, the seven segments will display “32”. Refer to Figure 4.9 for the diagram aid.

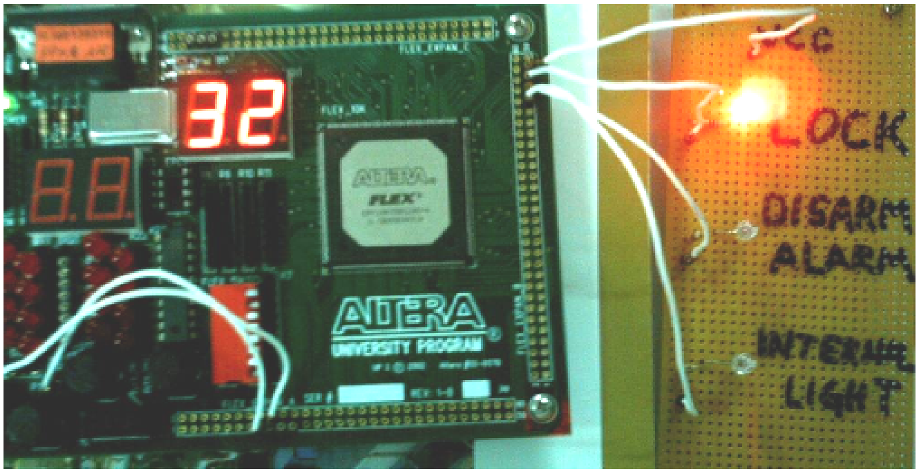

Figure 4.9 After Button C is Pressed.

Then, the manual lock switch is turned off by pulling it up, giving it the High signal. The Lock signal will be off, while the disarm alarm and light signal will be turned on. Refer to Figure 4.10.

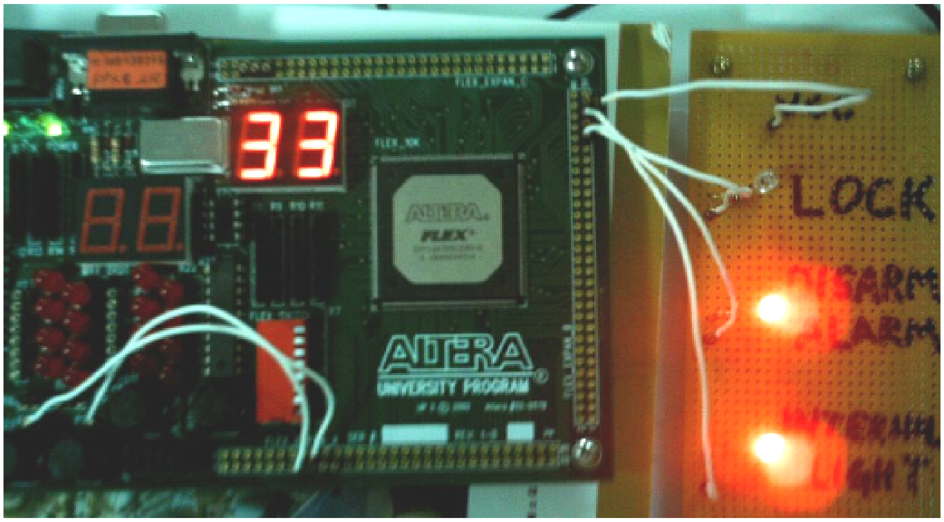

Figure 4.10 Unlocking.

Later, after the system is locked again, the Lock signal will be turned on again while the other two signals will be turned off. The result will be as in Figure 4.6.

4.5 Discussion

The manual lock signal in the Simulator Tool simulation is differ than the FPGA board simulation. Virtually, in the digital world, there is no delay between the time the unlock signal is disabled and the time for the manual lock knob is unlocked. In the waveform setting, the time for the unlock signal rise is the same time as the manual lock signal rise. Even though the time can be delayed, it still gives the same result.

In hardware or reality, there is a significant delay between those times. This is considering the friction of the metals and the joints used to connect the locking system to the manual unlock knob. This is the reason of there is a delay time between the Lock signal to turn off even after correct passkey has been inserted.

The input passkey set here is only A, B and C. This however can be changed via reprogramming the source code. There are only four passkeys available. Considering there are possibilities of some key combinations, there will be 340 possibilities of key combinations. There are still many rooms for end user to make their own passkey.

Overall, the result from the software simulation and the hardware simulation gives the same result and they are as expected.

4.6 Summary

This chapter had explained the results and the discussions over the study. The design of the source code is discussed first, followed by the simulation on the software and the hardware. Software simulation gives the timing simulation in detail while the hardware simulation shows the real working circuit. Finally, comparative results were shown while discussing the difference between Quartus II software simulation and FPGA board simulation.