Science of Advanced Materials
Vol. 3, 233–238, 2011

Fabrication and Characterization of 50 nm Silicon Nano-Gap Structures

Th. S. Dhahi[1,*], U. Hashim[1], and N. M. Ahmed[2]

[1] *Institute of Nano Electronic Engineering, University Malaysia Perlis (UniMAP), Perlis, 01000, Malaysia*
[2] *School of Physics, University Sains Malaysia (USM), 11800, Malaysia*

A simple method for the fabrication of nano-gaps less than 50 nm by using conventional photolithography combined with patterned-size reduction techniques is presented. Silicon material is used to fabricate the nano-gap structure and gold is used for the electrode. Two chrome masks are proposed to complete this work, the first mask for the nano-gap pattern and a second mask for the electrode. The method is based on the control of the coefficients (temperature and time) with an improved pattern size resolution by thermal oxidation. With this technique, there are no principal limitations to fabricating nanostructures with different layouts down to several nanometers in dimension. In this work, the proposed method is experimentally demonstrated by preparing the nano-gaps on a Si–SiO_2 substrate down to dimensions of 50 nm. The optical characterization that is applied to check the nano-gap structure is by using the scanning electron microscope (SEM).

Keywords: Nano-Gap, Pattern-Size Reduction, Nanostructure, Optical Characterization, Photolithography.

1. INTRODUCTION

The development of easy, low-cost and high-throughput techniques for the fabrication of nanostructures has been of great interest for both the possibility to increase the device-packing density and for reducing the power consumption, as well as the creation of a new class of nano electronic devices, like single electron transistors,[1] metal/insulator tunnel transistors,[2] nanowire transistors,[3] nanotube- or nanoparticle-based devices.[4,5] Chemical and biological nanosensors, biochips and nano-bioelectronics are other subjects that are progressing rapidly.[4,6–9] A coupling of biorecognition elements with nanomaterials (nanoparticles, nanotubes, etc.) and nanostructures (e.g., nano-electrodes, nano-transistors, nano-gaps, nanopores, nano-channels) of comparable dimensions might allow the creation of hybrid systems with unique functional and application possibilities.[4,7,10–16] Such functional hybrid systems (i.e., the "marriage" of biomolecules and nano-scaled transducers) provide powerful tools, not only for manipulation and detection, but also for the fundamental research of single biological molecules [DNA (deoxyribonucleic acid), immunospecies, proteins, etc.] and living cells. The realization of different nanometer-sized structures has been demonstrated by advanced high-resolution nanolithographic techniques such as electron- or ion-beam lithography, focused ion-beam milling, scanning tunneling or atomic force microscopy, nano-imprint lithography, and different top-down fabrication techniques, etc. (see e.g., Ref. [17] and references there). Although these techniques provide high resolution in generating different nanostructures, most of them are time-consuming, low-throughput, complicated and expensive. If conventional photolithography could be applied to form nanometer-sized structures including line- and space-patterns, it would be highly advantageous. Therefore, recently, some non-conventional techniques in combination with conventional photolithography have been proposed for the preparation of nano-electrodes, nano-gaps and other nano-scaled devices. These techniques include, for instance, a photoresist thermal reflow and shrinking[18] or photoresist ashing technique,[19] a shadow evaporation process,[20] a controlled size-reduction using the oxidation of Si[21–23] or laser-assisted electrochemical etching,[24] chemical–mechanical polishing,[25] the decrease of separation between metallic electrodes by means of an electro-deposition from an electrolyte solution,[26] methods that utilize a sidewall structure,[27] a self-aligned plasma etching of a silicon dioxide layer and silicon substrate,[28] or a lateral, partial anodic oxidation of the side-edge of a photolithographically-structured metallic film (e.g., Ti),[29] techniques that use a silicon-on-insulator structure,[30] etc. An alternative solution

*Author to whom correspondence should be addressed.

for the fabrication of self-aligned nanostructures by means of conventional photolithography combined with pattern-size reduction techniques has recently been proposed by the authors.[31, 32] The method was experimentally demonstrated by patterning nanostructures with different sizes and layouts on a Si substrate. In this work, the feasibility of the proposed method for the preparation of silicon nano-gaps on a Si–SiO_2substrate less than 50 nm is experimentally demonstrated.

2. RESEARCH METHODOLOGY

2.1. Mask Design

In this research work, a silicon substrate wafer is used to fabricate the nano-gap structure. The first step is to design and produce a mask, where two mask designs are proposed and the silicon nano-gap with a gold electrode process flow are developed. Dry-etching RIE is used to form the silicon nano-gap and wet-etching is used for the gold electrode structure. Anisotropy of RIE is modeled and the etching profiles are simulated. This method is proved to be applicable by analysis and experiments.[33]

The starting material used in this project is a *p*-type, 100 mm in diameter (4-inch) silicon substrate wafer. As for the lithography process, two photomasks are employed to fabricate the nano-gap using conventional photolithography and silicon dry-etching techniques. Commercial chrome masks are to be used in this research for a better photomasking process. This mask is used to develop the gold electrode with a silicon nano-gap. The photomasks are designed using AutoCAD and then printed onto a chrome glass surface.

Figure 1 is the first mask for nanogap electrode formation with a length and width of 5000 μm and 2500 μm, respectively, and the actual arrangement of the device design on the chrome mask. It consists of 160 dies with 6 different designs.

The proposed angle length of the end electrode is taken by 1/6th scale starting from 100 μm until 1100 μm, increasing by 100 μm for each S_d length. This is simply to check the best angle for the best nanogap formation after the etching process. The symbol S_d refers to the dimension of the side angle for the nano-gap design formation. It shows that when S_d is large this means the nano-gap becomes very sharp and less sharp with a smaller dimension of S_d.

Figure 2 is a schematic device design of mask 2 with 1500 μm length and 1500 μm width. The distance between two rectangles is 3500 μm, and the schematic mask is on chrome glass.

2.2. Nanostructure Fabrication

The proposed process steps of the gold electrode with silicon nano-gap fabrication are starting by cleaning the silicon wafer before depositing a 150 nm SiO_2 substrate on the silicon wafer and 200 nm Si layers, respectively,

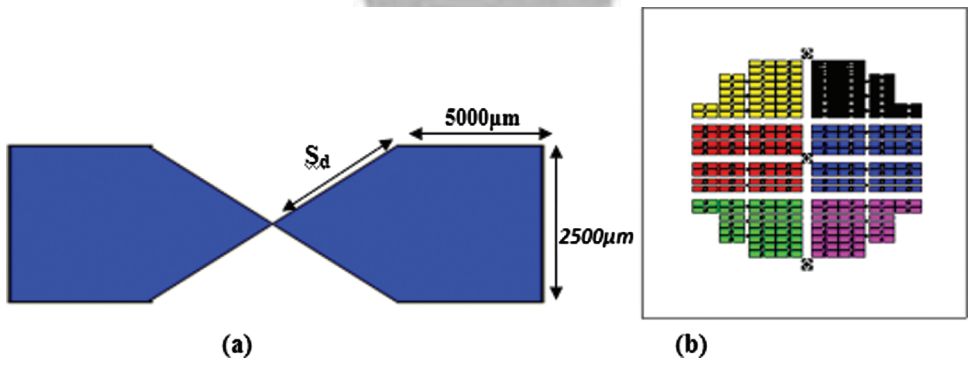

Fig. 1. (a) Design specification of the first mask, (b) Schematic design of the actual mask on chrome glass.

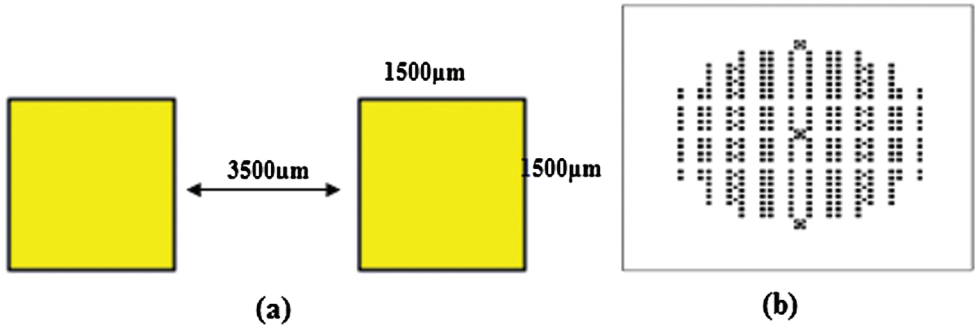

Fig. 2. (a) Design specification for mask2, (b) Schematic for mask2 on chrome glass.

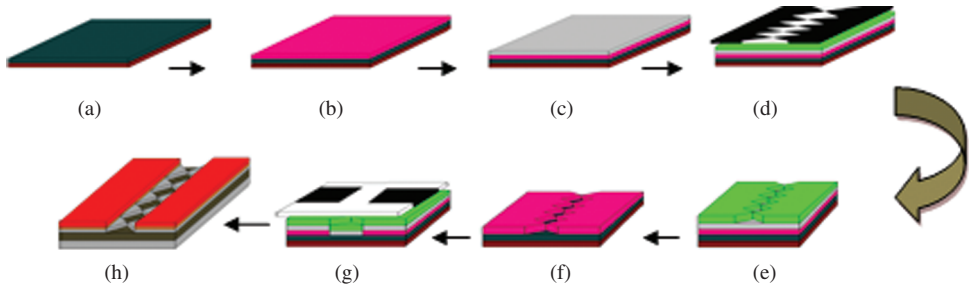

Fig. 3. Silicon nano-gap structure process flow.

by using plasma-enhanced chemical vapor deposition (PECVD) equipment. Then, a layer of 135 nm aluminum substrate as a hard mask using physical vapor deposition (PVD) equipment was performed to avoid damage to the silicon layer during the etching/RIE process. Next, in the photolithography process, a layer of positive photoresist 1200 nm thick is first applied on the aluminum substrate, and then exposed to ultraviolet light through Mask 1 as shown in Figure 3(d). After development only the unexposed resist would remain, and then the wet-etching process of the aluminum layer is performed before removing the resist. After that, the dry-etching process for a layer of silicon was done to fabricate the nano-gap using the size reduction technique as seen in the previous research, then a layer of 100 nm gold substrate is deposited after a 30 nm Ti layer; the resist coating process before exposing Mask2 and developing of the resist as seen in Figure 3(g). Then the wet-etching process of the Ti/Au substrate is performed before removing the resist. Finally, the structure of the gold electrode with a silicon nano-gap is obtained as shown in Figure 3(h).

Before fabricating the electrode, wet-etching for the aluminum layer and dry-etching using a reactive ion etching (RIE) process (a mixture of tetrafluoromethane, CF_4, and O_2 plasma was used), respectively, to pattern the Si layer according to the mask layout. The structured Si layer was oxidized at a temperature of 900 °C in dry O_2 atmosphere to form the oxidation layer. The oxidation time was from 15 to 90 minutes depending on the thickness of the Si layer. The prepared structures were characterized before and after the oxidation process by means of a scanning electron microscopy (SEM) method.

3. RESULTS AND DISCUSSION

The nano-gap structures were patterned via conventional lithography method onto the top of $Si/SiO_2/Si$ layers. Figure 4(a) shows the camera view of the photo mask that was used to transfer the nano-gap patterns during the photolithography process. While, Figures 4(b and c) exemplarily shows the SEM cross-sectional view of an original photo-lithographically-patterned silicon layer before and after applying the oxidation process.

After exposing the chrome mask, as seen in Figure 4(a), and the pattern of the 200 nm thick silicon layer to apply the oxidation at 900 °C for about 15 minutes, the original structure height (2 μm) in Figure 4(b) has been laterally expanded (as seen in Fig. 4(c)) by about 600 nm. Such overlapped structures have further been used for the preparation of nanostructures, whereas, after etching the oxidation layer using a buffered oxide etching (BOE) solution, which means etching and stripping the Si surface.

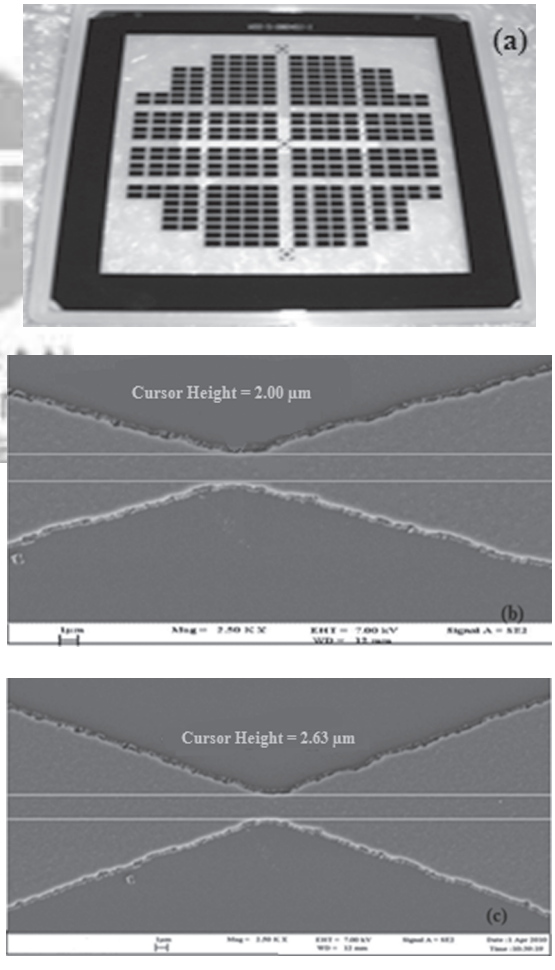

Fig. 4. Photo mask and SEM pictures of fabricated silicon pattern; (b) before using thermal oxidation process with a width of 2 μm, (c) after oxidation process with a width of 2.63 μm.

Therefore, in a further step, the oxidation layer has been deposited as a reducing material to form the nano-gap after etching the oxidation layers.

In this experiment, the original gap height before the oxidation etched was about 2 μm. After the thermal oxidation of the silicon layer at 900 °C for 15 minutes, and some of its thickness converted to SiO_2, a self-aligned nano-gap with the reduced height of about 600 nm has been formed. Thus, a pattern-size reduction by about 6× times has been achieved. The precise control of nanostructure dimensions is a crucial point for a reproducible fabrication. The layer-reduction or pattern-size reduction technique can generate an excellent reproducibility in controlling the layer diminution after the oxidation of the semiconductor layer, owing to the nature of the thermal oxidation process. Thus, the nano-gap size can be precisely controlled by the oxidation conditions (temperature, time) as well as by the thickness of the semiconductor layer. In order to investigate the dependence of the pattern-size reduction on the oxidation time of the patterned Si layer, the SEM photographs of the prepared nano-gap structures have been made after each fifteen minutes of oxidation. Figure 5 demonstrates SEM photographs of a patterned Si layer after the thermal oxidation process for 15_minutes (a),

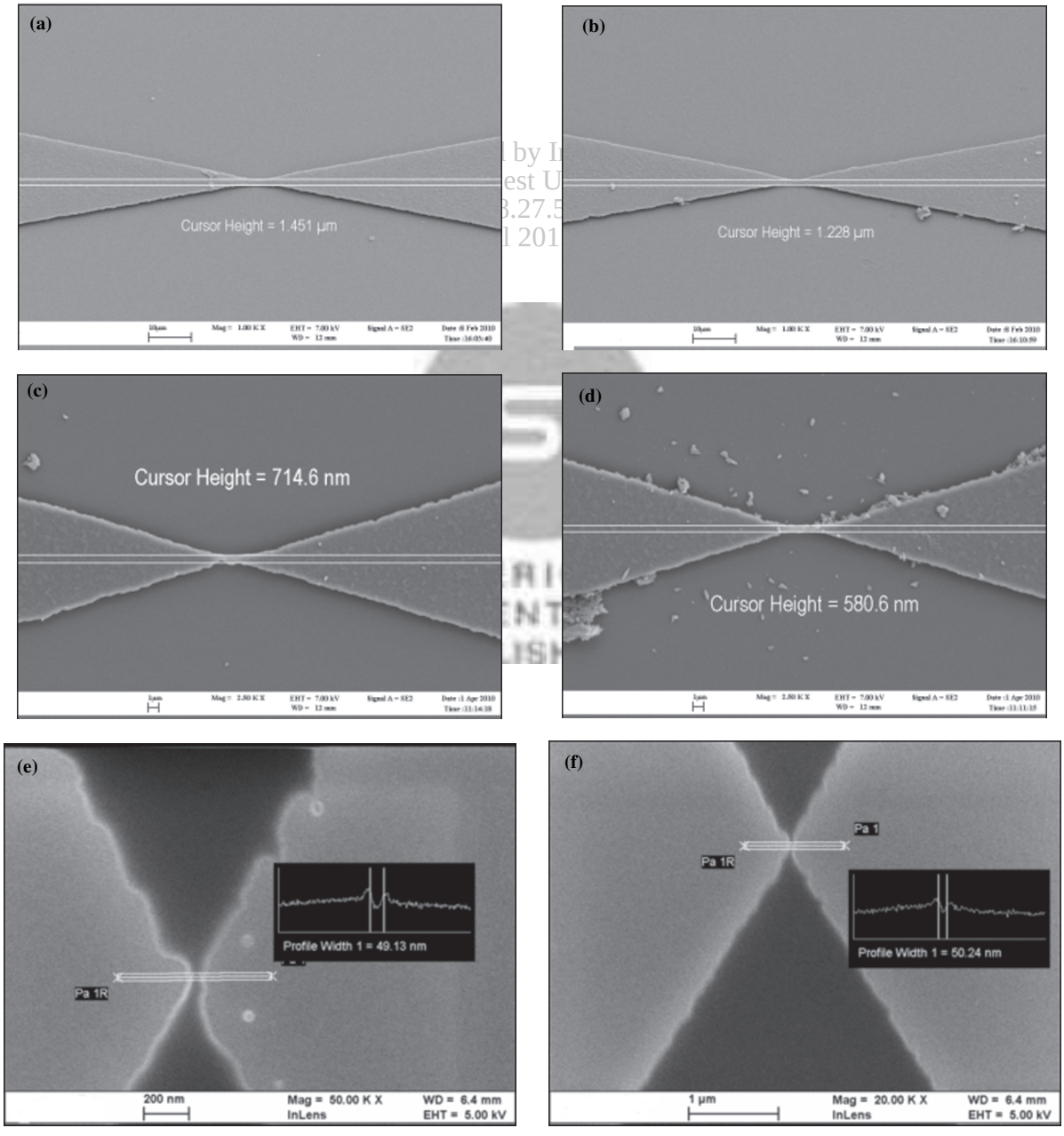

Fig. 5. SEM image for the reducing of the height of the gap and pattern of the nano-gap structure after thermal oxidation process for: (a) 15 min, (b) 30 min, (c) 45 min, (d) 60 min, (e) 75 min and (f) 90 min.

30_minutes (b), 45_minutes (c), 60_minutes (d), 75_minutes (e), and 90_minutes (f). In this experiment, the original (photo-lithographically-patterned) gap size before the oxidation was about zero. As can be seen, with the increasing of the oxidation time, the pattern height is decreased from the original value of 2 μm to 500 nm and a gap width of 50 nm and 48 nm starts to form after oxidation for 75 minutes and 90 minutes, respectively. Thus, a pattern-size reduction by more than 6× times has been achieved. Further increasing of the oxidation time does not lead to a significant reduction of the gap size. This means that after 90 minutes of oxidation, the silicon layer has been completely oxidized.

In this research, the dry oxidation used to apply the thermal oxidation process means the oxygen source is O_2 gas and after controlling other factors (temperature, pressure, dopant type and concentration with the Si-crystal orientation), can be defined as the oxidation growth rate. When the oxygen starts to reacts with silicon, it forms a silicon dioxide layer, which separates the silicon atoms from the oxygen molecules. When the oxide has just started to grow and the oxide layer is very thin (<50 nm), oxygen molecules can penetrate the oxide with few collisions in the oxide layer and reach the silicon, to react and continue to grow on the silicon dioxide layer, where Figure 6 shows the gradual rising curve between the oxidation thickness and the time of the oxidation process.

The oxide thickness was controlled in the range of less than 100 nm to avoid exceeding the consumption of the top silicon layer during the oxidation process. Showing the increasing in the oxidation thickness, we need to increase the time that's required to develop the oxidation layer.

Figure 7 clearly shows the rising curve between the oxidation time and the size of the gap, whereas, an increase in the time of the thermal oxidation process leads to an increase in the growth of the oxygen molecules, which collide and interact with the silicon atoms, creating the silicon dioxide layer, where the silicon dioxide thickness is proportional to the oxidation growth time.

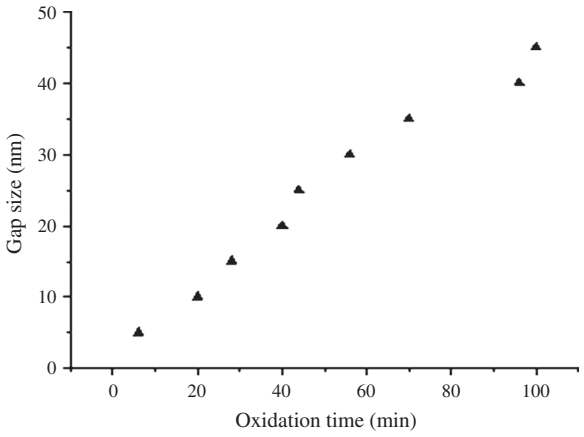

Fig. 7. The gap size (nm) curve increasing with the oxidation time (min).

Thus, after application of wet-etching to remove the oxidation layer using a BOE solution, where the BOE solution strips the silicon atoms that were acting with the oxygen molecules to reduce the thickness of the silicon layer, and increases the size of the gap as we see from Figure 7. The same procedure has happened when an increase in the oxidation thickness will help to increase the size of the gap[34] as seen in Figure 8.

The size reduction technique starts with the thermal oxidation growth to the desired thickness. The thickness of the silicon consumed is approximately 0.5 of the total oxide thickness. This means that for every 10 nm of the oxide layer, 5 nm of the silicon is consumed. The sample is then dipped into the BOE to remove the entire oxide layer. The detailed dimensions for the size reduction of the silicon nano-gap using SEM imaging are shown in Figure 5. After each oxidation process, the width profile decreases about 200 nm. This is reasonable because the oxide is consumed from the right and left side of the silicon nano-gap structures.

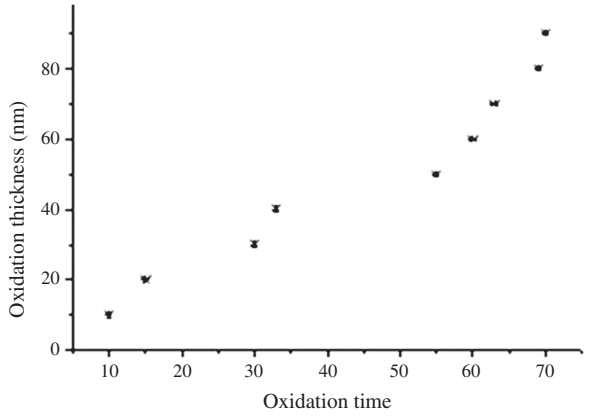

Fig. 6. The oxidation thickness (nm) rising curve with the oxidation time (min).

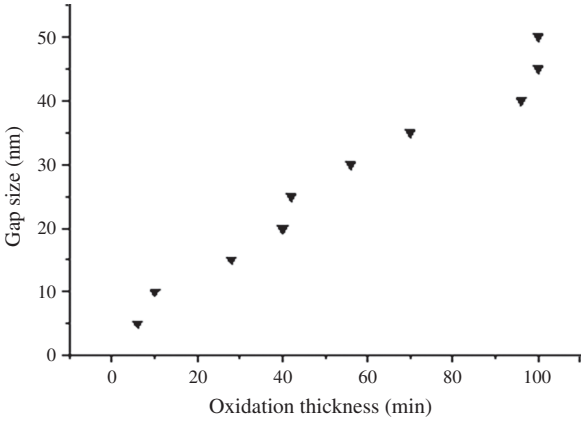

Fig. 8. The size of the gap (nm) curve increasing with the oxidation thickness (nm).

4. CONCLUSION

A simple method for the preparation of nano-gaps less than 50 nm using silicon material on a Si–SiO_2 substrate without the use of nanolithography techniques is presented. The method combines conventional photolithography with pattern-size reduction techniques, and is based on reduction of the pattern semiconductor height using a thermal oxidation process. The proposed method has been experimentally demonstrated by preparing lateral nano-gaps down to 50 nm dimensions. By applying thicker silicon layers, even smaller gaps, down to a few nanometers as well as closed nano-compartments could be formed. Moreover, this technique might possibly precisely control the fabrication of an array of nano-gaps with various dimensions and layouts on the same substrate. Future experiments will focus on building up nano-biosensors by coupling biomolecules within the nano-gaps with dimensions close to their persistence length.

Acknowledgments: We are grateful for fruitful discussions with our collaborators at the Institute of Nano Electronic Engineering (INEE) at University Malaysia Perlis (UniMAP). This work was supported by INEE at UniMAP, through the Nano Technology project. The views expressed in this publication are those of the authors and do not necessarily reflect the official view of the funding agencies on the subject.

References and Notes

1. H. Namatsu, Y. Watanabe, and K. Yamazaki, *J. Vac. Sci. Technol. B* 21, 1 (**2003**).
2. R. Sasajima, K. Fujimaru, and H. Matsumura, *Appl. Phys. Lett.* 74, 3215 (**1999**).
3. A. Marchi, E. Gnani, and S. Reggiani, *Solid-State Electron.* 50, 78 (**2006**).
4. B. L. Allen, P. D. Kichambare, and A. Star, *Adv. Mater.* 19, 1439 (**2007**).
5. Y. P. Ding, Y. Dong, A. Barat, and J. D. Nowak, *IEEE Trans. Electron. Dev.* 53, 2525 (**2006**).
6. M. J. Schöning and A. Poghossian, *Electroanal.* 18, 1893 (**2006**).
7. U. Yogeswaren and S. M. Chen, *Sensors* 8, 290 (**2008**).
8. T. C. Yih and I. Talpasanu, Artech-House, Inc., London (**2008**).
9. A. Poghossian, M. J. Schöning, and C. A. Grimes, Encyclopedia of Sensors, 9, American Scientific Publishers, Stevenson Ranch, USA (**2006**), pp. 463–534.
10. J. Tang, E. P. de Poortere, and J. E. Klare, *Microelectron. Eng.* 83, 1706 (**2006**).
11. G. J. Zhang, J. H. Chua, and R. E. Chee, *Biosens. Bioelectron.* 23, 1701 (**2008**).
12. G. Sigalov, J. Comer, and G. Timp, *Nano Lett.* 8, 56 (**2008**).
13. J. Gun, M. J. Schöning, and M. Abouzar, *Electroanal* 20, 1748 (**2008**).
14. C. Tsai, Y. H. Tsai, and C. C. Pun, *Microsyst. Technol.* 11, 91 (**2005**).
15. X. Liang and S. Y. Chou, *Nano Lett.* 8, 1472 (**2008**).
16. Y. H. Cho, S. W. Lee, and T. Fujii, *Microelectron. Eng.* 85, 1275 (**2008**).
17. Y. Chen and A. Pepin, *Electrophoresis* 22, 187 (**2001**).
18. C. C. Meng, G. R. Liao, and S. S. Lu, *Electron. Lett.* 37, 1045 (**2001**).
19. K. S. Kim, K. N. Lee, and Y. Roh, *Thin Solid Films* 516, 1489 (**2008**).
20. T. Ishida, M. Horikawa, and M. Nakano, *Jpn. J. Appl. Phys.* 44, L465 (**2005**).
21. Y.-K. Choi, J. Zhu, and J. Grunes, *J. Phys. Chem. B* 107, 3340 (**2003**).
22. S. Hashioka, H. Tsuritani, and T. Obata, *Jap. J. Appl. Phys.* 44, 4213 (**2005**).
23. Y. H. Cho, S. W. Lee, and B. J. Kim, *Nanotechnology* 18, 465303 (**2007**).
24. R. Juhasz and J. Linnros, *Microelectron. Eng.* 61–62, 563 (**2002**).
25. C. Lee, E. H. Yang, and N. V. Myung, *Nano Lett.* 3, 1339 (**2003**).
26. A. F. Morpurgo, C. M. Marcus, and D. B. Robinson, *Appl. Phys. Lett.* 74, 2084 (**1999**).
27. K. H. Chung, S. K. Sung, and D. H. Kim, *Jpn. J. Appl. Phys.* 41, 4410 (**2002**).
28. G. Georgiev, M. Muller, and A. Georgieva, *J. Vac. Sci. Technol. B* 21, 1361 (**2003**).
29. S. Hashioka, T. Mogi, and H. Masumura, *Jap. J. Appl. Phys.* 42, 4169 (**2003**).
30. S. Strobel, K. Arinaga, and A. Hansen, *Nanotechnology* 18, 295201 (**2007**).
31. J. Platen, A. Poghossian, and M. J. Schoning, *Sensors* 6, 361 (**2006**).
32. A. Poghossian, J. Platen, and M. J. Schoning, *Electrochim. Acta* 51, 838 (**2005**).
33. Y. Liu and Z. Zhao, *Proceedings of the 2nd IEEE International Conference on Nano/Micro Engineeres and Molecular Systems*, Bangkok, Thailand, January (**2007**), pp. 753–758.
34. H. Spelthahn, A. Poghossian, and M. J. Schoning, Electrochimica Acta 54, 6010 (**2009**).

Received: 1 December 2010. Accepted: 13 December 2010.