CHAPTER 4

RESULTS, ANALYSIS AND DISCUSSIONS

4.0 Masking

Producing masks that are compatible for fabrication has to adhere to certain quality aspects. Since the dimensions of the device are critical, the masks must be able to contain and aid in the transfer of precise and accurate designs. There is no compromise over dimensional errors and also quality of printing.

Most of the printers, bubble jet or laser based produce images with smudges that are harmful in photolithography. They may cause shorts and opens in the design that will catastrophically alter the functionality of the device. The capability of producing images with high resolution is the determining factor to the dimensions of the design.

Since commercial printers cannot accommodate the device's dimensions, a film plotting company was assigned to produce the designs on transparent films. Their minimum tolerance in resolution was the benchmark for designing the device. A photo mask was produced.

4.1 Wafer Preparation

4.1.0 Wafer Measurements

The wafers that come from the supplier normally follow consistent specifications. However, they may vary within a given tolerance. Prior measurements are made to verify the specifications of the wafer before the actual fabrication process.

The wafer is measured of its thickness on 5 random points. The mean is taken.

4.1.1 Native Oxide

The wafer might carry a certain amount of oxide called native oxide due to its exposure to oxygen dissolved in moisture. At room temperature, it has a growth rate of approximately 15 Å per hour. Oxygen molecules that are dissolved in water penetrate into the silicon surface causing oxidation to occur.

This oxide prohibits the usual electrical characteristics of the silicon wafer as SiO_2 is not conductive. It disrupts the performance and reliability of the wafer. Sometimes, it may even carry metallic impurities that further contaminate the chemical properties of silicon.

To remove this, the wafer is immersed into Buffered Oxide Etch for approximately 5 minutes.

Table 4.1: Silicon dioxide thickness on wafer before and after BOE measured using Spectrophotometer

Location	Oxide thickness before BOE (Å)	Oxide thickness after BOE(Å)
1	155.9	50.0
2	143.2	50.0
3	150.4	50.0
4	164.7	50.0
5	149.0	50.0
Mean	**152.64**	**50.0**

4.1.2 Wafer type

The type of wafer used is checked, whether it is p or n type as to determine the type of dopant, phosphorus or boron. A PNT conduction gauge is used to do this. The wafer is confirmed p-type, boron doped.

4.1.3 Sheet resistance

The sheet resistance of the wafer is measured using a 4 point probe on 5 different points and the mean is calculated.

Table 4.2: Sheet resistance of wafer measured using Four Point Probe

Point	Resistance (Ω)
1	5.24
2	4.85
3	5.33
4	5.79
5	4.81
Mean	**5.20**

4.1.4 Wafer specification and Wafer Measurements

Table 4.3: A comparison of **w**afer specifications by supplier (data sheet) and measured values

	Wafer Specification	**Measurement**
Diameter	100mm	100mm
Type	p-type	p-type
Orientation	<100>	<100>
Thickness	510µm	492µm
Resistivity	1-20Ω/cm	5.15Ω/cm
Grade	Test wafer	Test wafer

4.2. Photolitography: Mask 1 Pattern Transfer

This process is for transferring the pattern for etching silicon to form grooves for electrodes and channels for fluid. Two methods were employed to form these trenches, Reactive Ion Etch (RIE) and wet etch. Each process would require different sacrificial masks.

For the dry etch method, to etch 10µm of silicon, a 10µm thick silicon dioxide or silicon nitride mask is required as the etch selectivity is low. It would not be practical to grow that much of oxide thermally as it would be very costly. Plasma Enhanced Chemical Vapour Deposition (PECVD) would also be very costly. Besides, after RIE, mask (made up of silicon dioxide, silicon nitride or photoresist) leave a residue that is impossible to be stripped.

An alternative method is to use a thick layer of aluminium as mask. Based on some pre-project experiments carried out, a 300Å thick aluminium is needed for a 0.4µm etch before it completely diminishes. Arithmetically, it requires 0.75µm thick aluminium masking, which brings to 25 rounds of aluminium physical vapour deposition as each

deposition yields 300Åm of deposition. Wafer A is coated with aluminium for this purpose.

30 rounds of aluminium PVD was conducted on the wafer. The thickness of the deposition was measured using the Surface Profiler. A mean thickness of 1.1µm was successfully deposited.

Alternatively, for wet etch in 25% KOH (Potassium hydroxide), a thermal oxide is grown in the wet oxidation furnace for 2 hours. Thermal oxide was chosen as it has better strength over PECVD oxide and it has a faster growth rate compared to dry oxidation. Wafer B is thermally treated for oxidation. 2 hours of oxidation yielded the following thickness:

Table 4.4: Thermal silicon dioxide thickness measured using a Spectrophotometer

Point	Thermal Oxide Thickness (Åm)
1	5539.0
2	5194.5
3	5835.2
4	5742.0
5	5281.0
Mean	**5518.3**

4.2.1 Photoresist Coating

The Photoresist used in photolithography in this project is PR1-2000A. Photoresist will be the temporarily contain the pattern for the sacrificial mask etch. Since the photoresist is positive type, the mask must carry the exact image of pattern that has to be transferred onto the mask. Mask 1 carries the image for aluminium electrodes and fluid channel formations.

The following parameters were used for spin coating throughout the project:

- ✓ 700rpm for 5 seconds
- ✓ 3000rpm for 25 seconds
- ✓ 0 rpm for 5 seconds

A low ramp up speed was used for the distribution of resist throughout the surface of the wafer. High speed at this time would gravitate too much of resist away from the wafer to the spinner's chamber. This would be a waste. The higher speed would determine the thickness of coating. Higher spin speed produces thinner coatings due to larger centrifugal forces. The length of time decides uniformity of coating. The parameters were set in regard to this and after a few experiments.

4.2.2 Soft Bake

The photoresist is in liquefied state. It has to be solidified by driving out majority of the solvents. This improves its adhesion on the wafer and will be more stable for high resolution photo-solubalisation through UV radiation. The wafer is soft baked for 90 seconds at 90^{o}C.

The wafer is left to cool to room temperature. This is an important measure as 1^{o}C difference would cause 0.5μm difference on silicon due to thermal expansion effect.

4.2.3 Exposure

The mask is properly aligned to the wafer on the mask aligner. Contact printing method is used here, where the wafer makes direct contact on mask. This allows

minimum light to diffract and distort the dimensions of the images. The light penetrates through the clear areas on the mask and a photochemical reaction takes place in that area. Areas that are covered do not get photosolubalised. However, it was difficult to ensure complete contact due to curvatures on the wafer. The exposure was done for 100 seconds.

4.2.4 Post-Development Bake

Since the design dimensions are very critical, prone for overdevelopment, and a peel of easily, the photoresist is baked for another 60 seconds. This would harden the resist and further enhance its adhesion on the wafer.

4.2.5 Development

The wafer is immersed into the developer solution. Developer is a liquid chemical that dissolves the soluble regions of resist. Development is sensitive to temperature. It is important to ensure the wafer and the developer solution remains in a constant temperature.

Some problems may arise during development. Under development is a phenomenon where the photoresist is not completely removed, where either slopped resist walls form or residual resist still remain on the open area. In an underdeveloped image, lines appear narrower and poorly defined. Another scenario that posts equal problem is overdevelopment. In this case, the unexposed resist also starts to dissolve in the developer. Lines would appear broader than they were meant to be. The time for development depends on the concentration of the developer solution (developer to de-

ionized water ratio), agitation, and the number of times it has been used prior to this process.

In this project, developing the pattern was a very difficult task. The development rate was not uniform. After 1 minute, certain sectors were overdeveloped and the rest were underdeveloped. The miniscule dimensions of the device made it practically impossible to obtain perfect development. It took approximately 50 rounds of repetition of the photolithography processes to finally obtain some perfectly developed patterns.

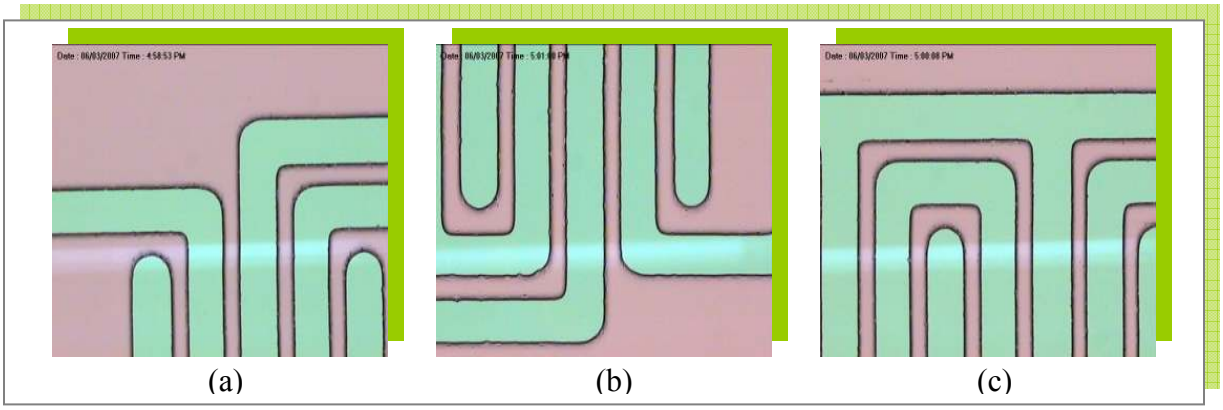


Figure 4.1: Wafer B After development process before BOE.

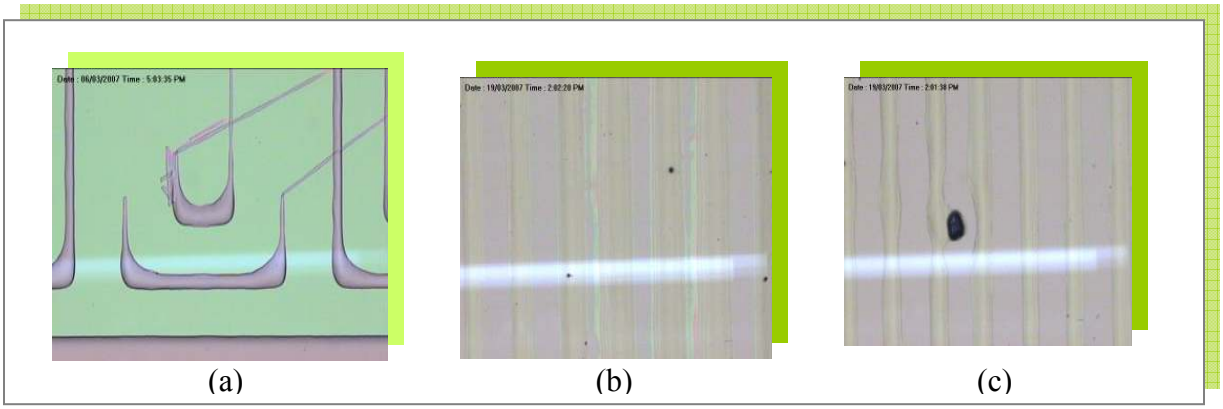


Figure 4.2: Common Defects on during Development.(a)Resist peel from oxide surface, (b) underdevelopment and overdevelopment at the same time, (c) Particle contamination

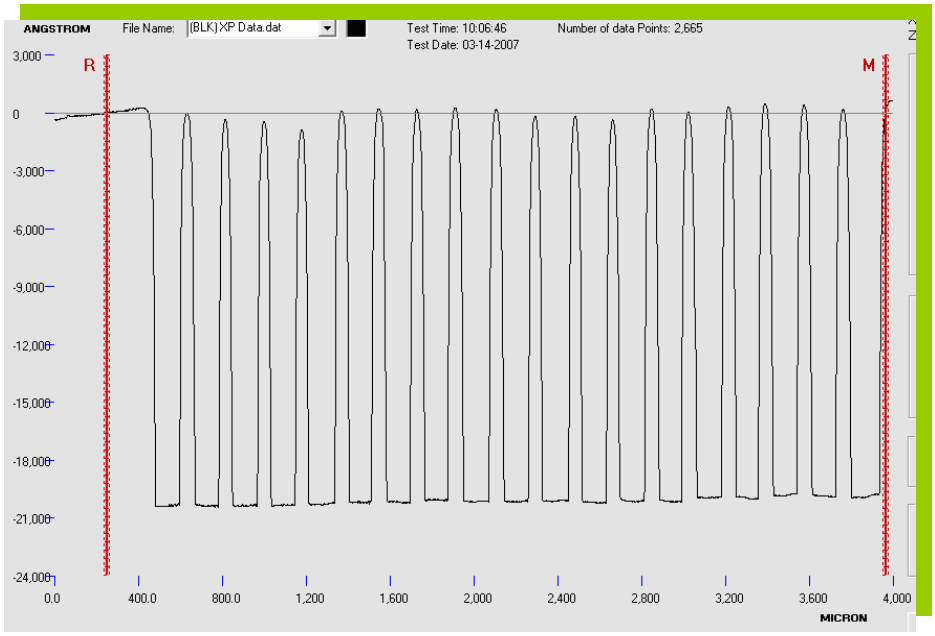


Figure 4.3: Surface Profile after development

The adhesion of the photoresist to the oxide is not strong. Since the device dimensions were very small, the PR strips that formed the barriers of the channels peeled easily under minimum fluid agitation. Some areas of the pattern would develop perfectly within 1 minute, but some areas may still be underdeveloped. By the time these areas develop, the earlier formed strips peel off from the surface of the silicon dioxide. One way to combat this would be to use HMDS, an adhesion promoting substance that increases the adhesion strength of the resist.

Particles have always posted a challenge in the fabrication industry. In this project, many traces of particles were found. These particles hinder the flow of UV, causing some open areas to be closed. To resolve this, the wafer was frequently washed in running DI water before every process. This reduced the number of particle deposition on the wafer tremendously.

To control the development of the images, the device was immersed sector by sector. This prevented uneven and overdevelopment from occurring. When attention is given to individual devices at a time, it was mush easier to control the development rate.

The developer is diluted in DI water at a ratio of 2:1 developer to DI water to reduce the development speed to allow better control of the process.

When the image is developed on the wafer coated with aluminium, the developer begins to etch aluminium in the open area. This makes the development process for wafer A very critical. The wafer can only be developed once as some aluminium is etched together. There is no room for rework. The exposed resist has to be carefully developed to prevent overdevelopment.

4.2.6 Hard Bake

Hard bake is done for 180 seconds at 90^{o}C to remove the remaining solvent in the photo resist. It is also to improve its adhesion on the wafer and to increase its strength to withstand Buffered Oxide Etch (BOE). The resist becomes more resistant to BOE. Residual developer and DI water used for wafer cleaning is also evaporated during this heat treatment. Over baking the resist may cause a reduction in resolution. Too high a temperature would lead to flow of resist that may distort the image. In the other extreme, resist may not achieve its required strength.

4.2.7 Visual Inspection

To ensure that the photo resist is developed well and if the pattern transfer was successful, the developed wafer is inspected under a high power microscope. This process would be essential to make sure the device dimensions were formed correctly without under or over development. At this stage, mistakes are reversible. In case the device patterns show distortion, the resist can be stripped using acetone, spin dried and the photolithography proper is reworked. The pattern transfer process is irreversible after etch. It is also irreversible for the case of Wafer A, where aluminium was used as mask.

4.2.8 Silicon dioxide etch

The thermally grown silicon dioxide serves as mask for Potassium hydroxide's silicon etch. The pattern is now in the photoresist layer. To transfer the pattern to he silicon dioxide mask, the wafer is immersed into Buffered Oxide Etch (BOE). The photoresist prevents etch on the oxide beneath it. The rest of the open areas are etched. The etch rate of the BOE is 400Å per minute. It is sufficient to visually inspect the wafer to determine if any oxide is still left on the wafer. Once the oxide is stripped the chemical does not adhere on the silicon wafer. To verify this, the oxide thickness is measured using the spectrophotometer.

4.3 Etching Process for Mask 1

Two methods are employed to transfer to etch the trenches. Wafer A goes through RIE for trench formation with aluminium as mask whereas Wafer B goes through KOH immersion at 60^{o}C. Both etch should provide anisotropic profiles. Due to critically small dimensions, the two methods are attempted. The better technique would be employed.

4.3.1 Wafer A (RIE using aluminium as mask):

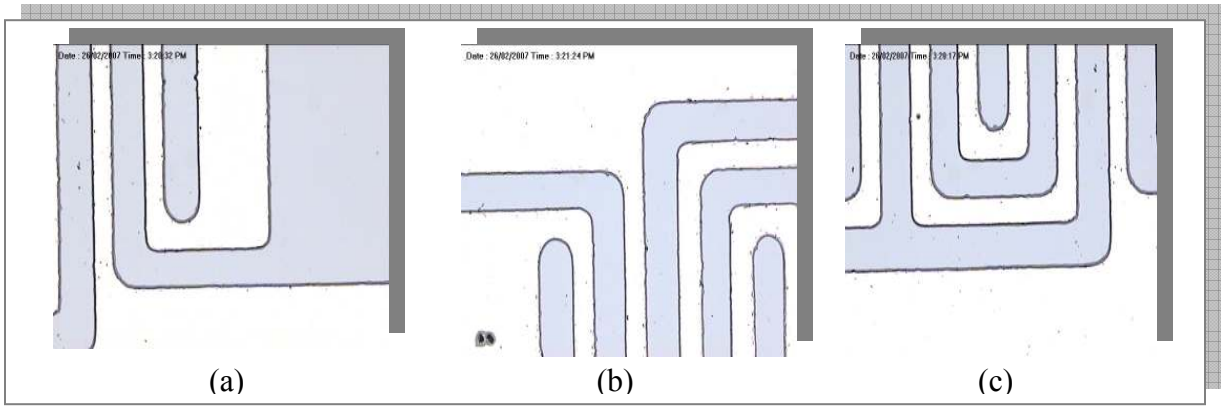


Figure 4.4: Wafer A after development and aluminium etch

Unwanted aluminium, in the areas where the trenches have to be formed is removed in Aluminium etch at room temperature. This process takes about 35 minutes to completely etch away the areas where the electrodes and fluid channels are to be formed.

Aluminium is used as mask for Reactive ion etch (RIE). The etch depth needed is 10μm. Due to the low selectivity of silicon and silicon dioxide, to etch a trench that deep would require a similar thickness value of silicon dioxide to the depth. In practice, it would cost a lot to grow (Thermally) or deposit (via plasma enhanced) 10μm thick silicon dioxide. Besides, the reaction of CF_4 and O_2, the main etchant in the RIE mechanism chemically reacts with glass and produces a residual by-product deposition that is irremovable. This calls off the use of SiO_2 as mask for RIE.

Photoresist are also commonly used in RIE. Prior experiments were carried out using PR as mask in RIE. It had low resistivity to the plasma etch and was etched away very fast. It also poses the similar problem as silicon dioxide where residual by product from the chemical reaction between the gases and PR cause polymerization. The PR is also irremovable after RIE. Using a thick layer of photoresist is the answer for this. It would stand for an adequate time and be removable through chemical etchants. But, transferring pattern in a thick layer of PR poses other risks like resolution and image distortions.

Tests were carried out to etch silicon using RIE with aluminium as mask. With a single physical vapour deposition (which yields approximately 300Å of aluminium), and RIE for 5 minutes, a mean of 6000Å of silicon was etched.

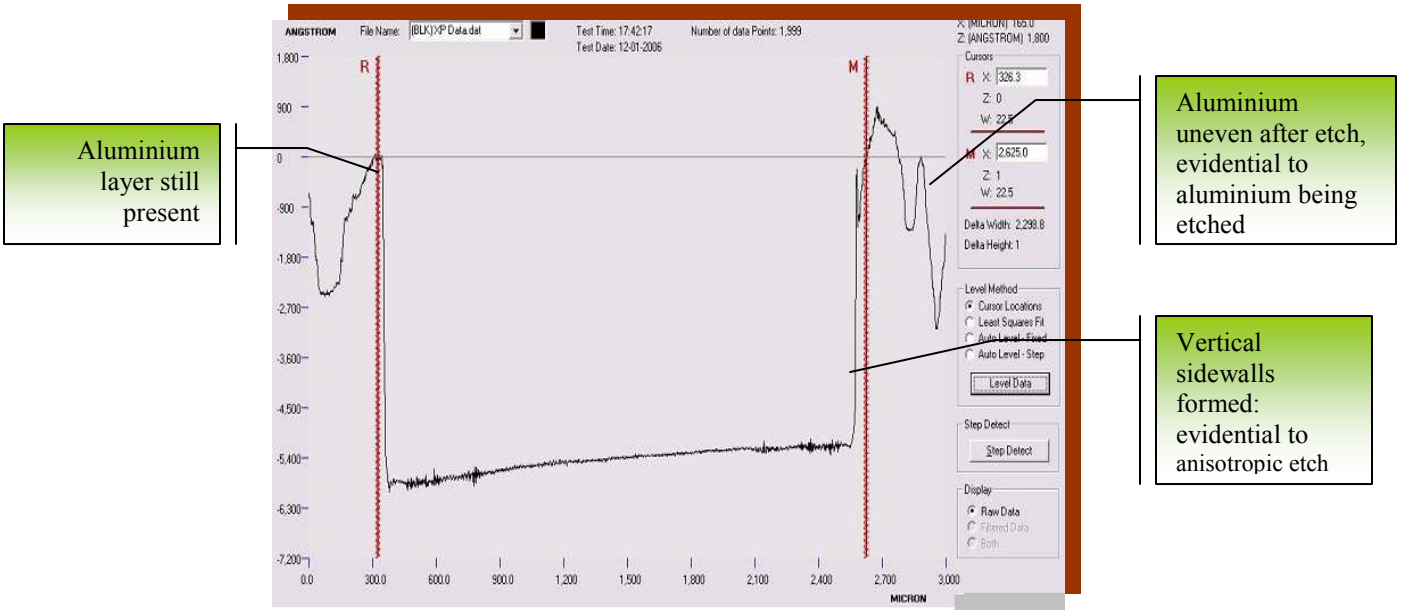


Figure 4.5: Depth after 15 minutes RIE with Aluminium mask on test wafer

After the RIE, the mirror like image of aluminium deposition turned pale white on random locations on the surface of aluminium. This may be a residue or by product of aluminium's reaction with the RIE etchants. An EDX was conducted on the test wafer to see the elements present on after RIE. Originally, only aluminium and silicon is seen. After RIE, a small percentage of fluorine was present. This may attribute the pale whitish substance on the aluminium as aluminium fluoride. The aluminium was later stripped using Piranha Etch as aluminium etch could not remove the aluminium fluoride. The fluoride is one of the gasses used in plasma etch. In the bombardment, CF_4 breaks into free radicals that easily react with aluminium to produce aluminium fluoride (AlF_3).

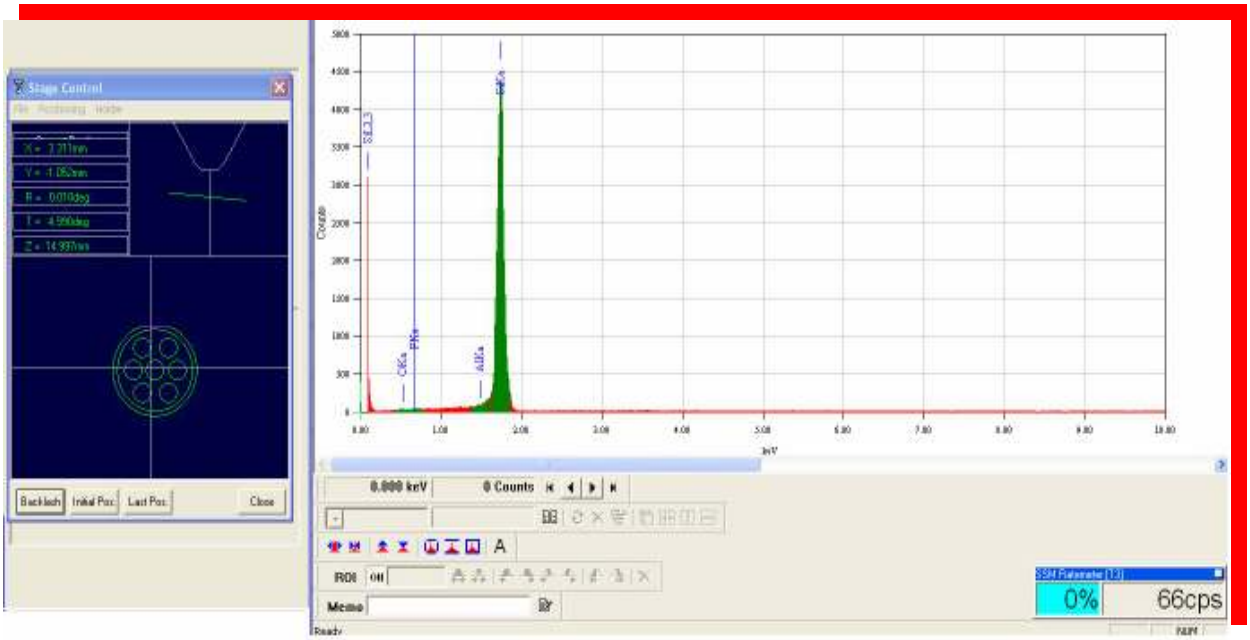


Figure 4.6: EDX on wafer with aluminium mask after RIE

Table 4.5: X-ray results on Elements present on wafer before RIE

Element	Energy (keV)	Mass (%)	Error (%)	At (%)	K
O	0.525	1.31	4.88	2.28	0.6886
Al	1.486	3.44	1.29	3.54	3.4961
Si	1.739	95.24	1.27	94.17	95.8153
Total		100		100	

Table 4.6: X-ray results on Elements present on wafer after RIE

Element	Energy (keV)	Mass (%)	Error (%)	At (%)	K
O	0.525	0.64	7.00	1.12	0.3258
F	0.677	0.30	2.47	0.44	0.1057
Al	1.486	1.93	1.81	2.00	1.9234
Si	1.739	97.13	1.75	96.45	97.6451
Total		100		100	

Wafer A that is deposited with 1.2μm of aluminium was subjected to 5 minutes RIE. The recipe used is: 45% CF_4, 5% O_2 with 50V. After RIE, the sample was examined. Similar observations were obtained. Whitish residues were found deposited throughout the wafer. The aluminium could not be stripped. This technique is proved to be not applicable. Aluminium cannot be used as mask as it is also etched at a high rate in RIE. This method is therefore called off.

4.3.2 Wafer B (KOH using Silicon dioxide as mask):

A pre-test is carried for silicon etch in potassium hydroxide with photo resist as mask. The following surface profile was obtained. Photoresist was etched faster than silicon. This proves its unsuitability as mask for KOH mask. Thermal oxidation is used instead as mask.

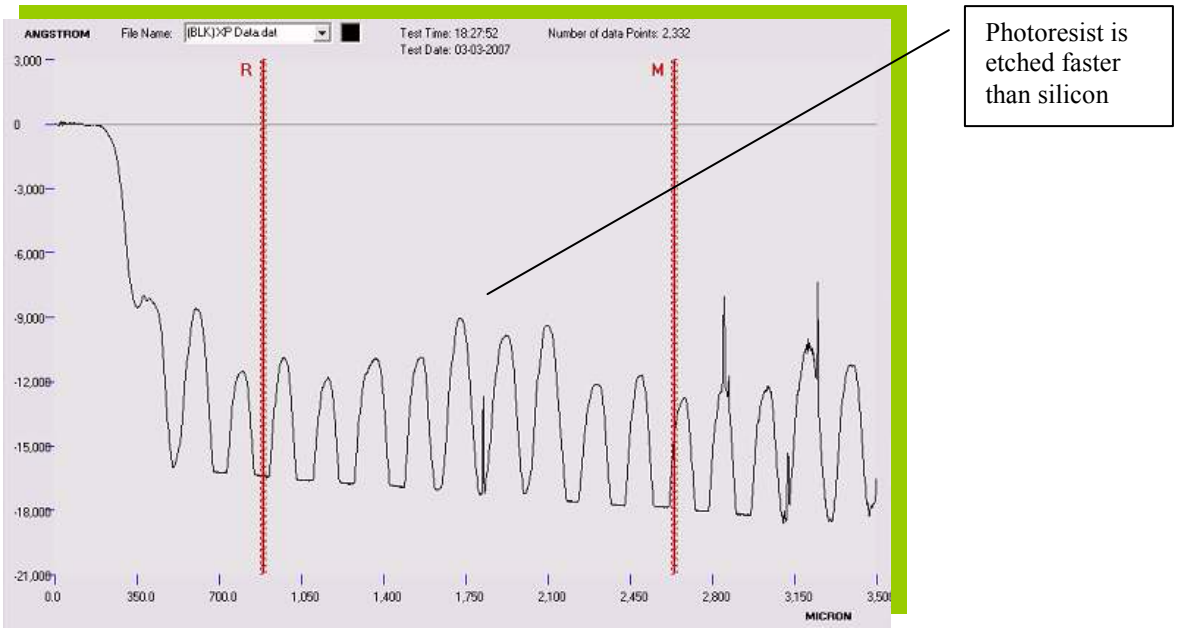


Figure 4.7: Surface profile after 5 minutes immersion in KOH for silicon etch with photo resist as mask

Wafer B has acquired approximately 5000Å of thermal silicon dioxide. The photoresist used for pattern transfer is stripped with acetone and then spin dried.

Low temperature and low concentration KOH has better selectivity conditions. It also produces vertical sidewalls (anisotropic etch). Higher temperatures produce smoother sidewalls but the walls may slant to 80^0 for a <100> orientation wafer. It may also have low selectivity with reference to silicon dioxide. Above 80^oC, non-uniformity of etch rate becomes considerably worse. So, 25% KOH aqueous at 60^oC is used for silicon etch. Wafer B, which carries silicon dioxide as mask is immersed into the solution. KOH is a hazardous substance and may cause blindness if it comes into contact. Extra caution has to be taken when working with this substance.

A lot of hydrogen bubbles will be released during this process. These hydrogen bubbles which are produced in the reacted surface hinder chemical contact with the solution causing a very rough surface on the wafer. By adding a little IPA, the surface roughness can be reduced. Since IPA was not readily available, the etch process was continued without IPA.

The etch process took 30 minutes and the etch rate is calculated. The etch rate is 3750Å per minute.

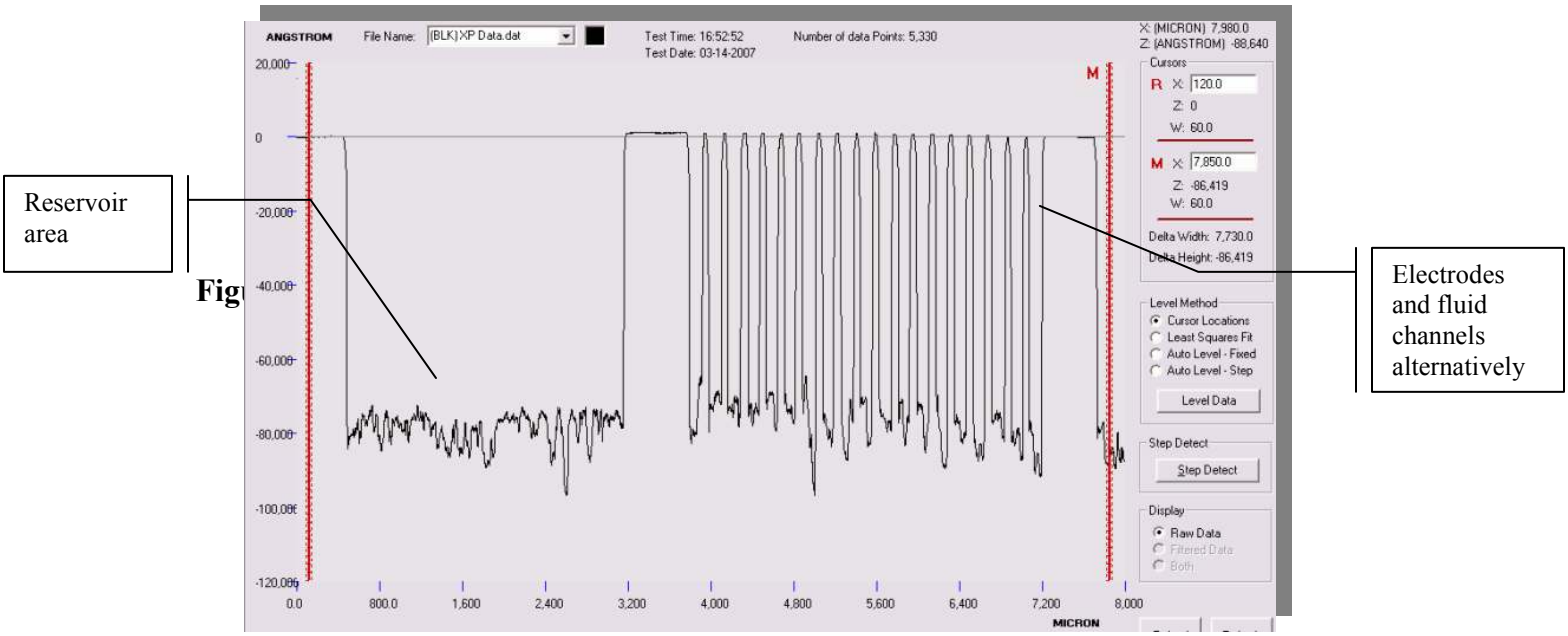


Figure 4.8: Surface profile of wafer B after 20 minutes in KOH 25% at 60°C

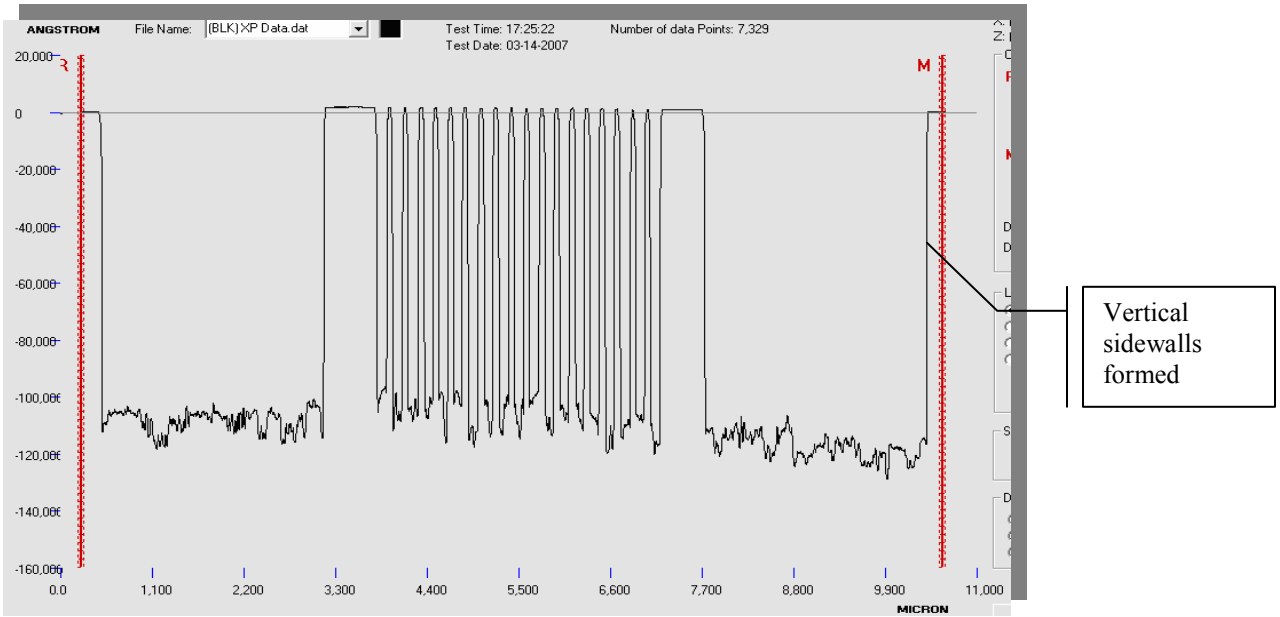


Figure 4.9: Surface profile of wafer B after 30 minutes in KOH 25% at 60°C

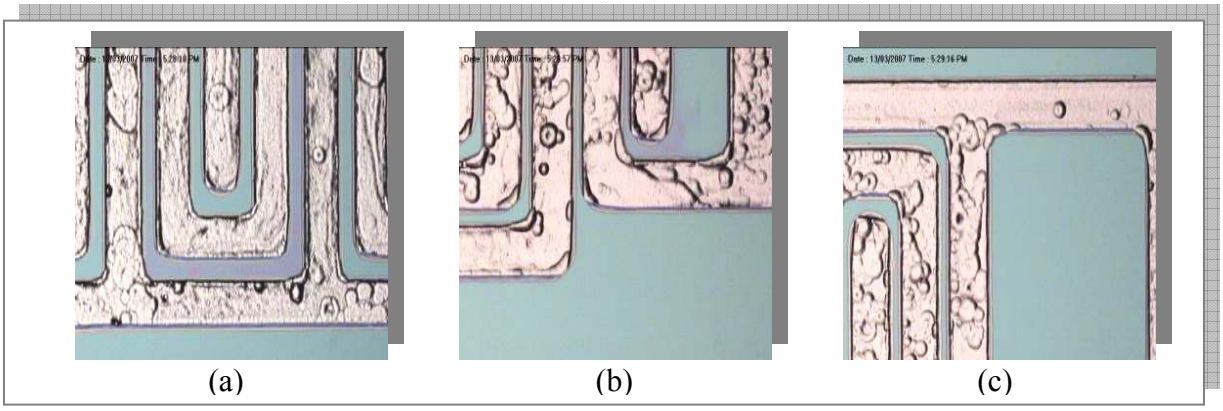


Figure 4.10: Visuals of channels after KOH etch captured under high power microscope. A rough surface forms due to the production of hydrogen bubbles that hinder the KOH reaction on the silicon surface.

The thickness of silicon oxide mask was etched at a very slow rate, 50Å per minute. After 30 minutes of immersion into KOH solution, the silicone oxide thickness reduced to 4538Å. This proves that at 60^{o}C, 25% KOH aqueous has very good selectivity between silicon and silicon dioxide.

A major disadvantage of using KOH is the presence of alkaline ions, which are detrimental to the fabrication of sensitive electronic parts. In this project, the fabrication of capacitor, this would not be a threat to its electrical functionality. A layer of thermal oxide is grown to insulate the etched surface.

4.4 Thermal oxidation for insulation

A layer of thermal oxide is grown as insulation on the sidewalls. Since the wafer has low resistivity, there might be inter-electrode conductivity through the substrate instead of the fluid. This thermal oxide will hinder this from happening. It will cover the entire surface and channels where the electrodes and fluid will reside. Silicon dioxide has

better wetability compared to silicon. This would be an added advantage to promote capillary action.

The trench-etched wafer is oxidized thermally at 1000^{o}C for 2 hours. This process yielded approximately 5400Å of oxide on the silicon surface. The wafer has a slight purplish green hue. The following table depicts the silicon dioxide thickness obtained via spectrophotometer.

Table 4.7: Silicon dioxide thickness on wafer after thermal oxidation

Point	Thermal Oxide Thickness (Åm)
1	5418.0
2	5440.2
3	5740.2
4	5209.7
5	5254.8
Mean	**5412.2**

4.5 Aluminium Physical Vapour Deposition

Now that the trenches are formed and shielded with a layer of thermal oxide as insulation, it is now ready for aluminium deposition. This aluminium will act as a conduction element for electroplating, to allow electron flow from current to aluminium ions. The wafer with an oxide layer on its surface is not electrically conductive.

Three rounds of PVDs are done for approximately 1nm thick deposition using 3 (1 inch X 1 inch) aluminium strips.

4.6 Electroplating

Electroplating is done using 50% aluminium nitrate aqueous as electrolyte, aluminium strips as anode and wafer as cathode. A 0.1A current and 2V supply is given to the system and left for 10 minutes.

A lot of bubbles were seen on the wafer surface throughout the electrolysis processes. After 10 minutes, the wafer was observed. A layer of uneven deposition with smudges of brown is seen on random locations of the wafer. Since there were no means to measure the thickness of aluminium, the process was called off.

4.7 Mask 2 Pattern Transfer

With the aluminium deposited on the wafer, mask 2 pattern is transferred. This mask will cover areas where the electrodes were supposed to remain. The rest of the area will be exposed for aluminium etching process next.

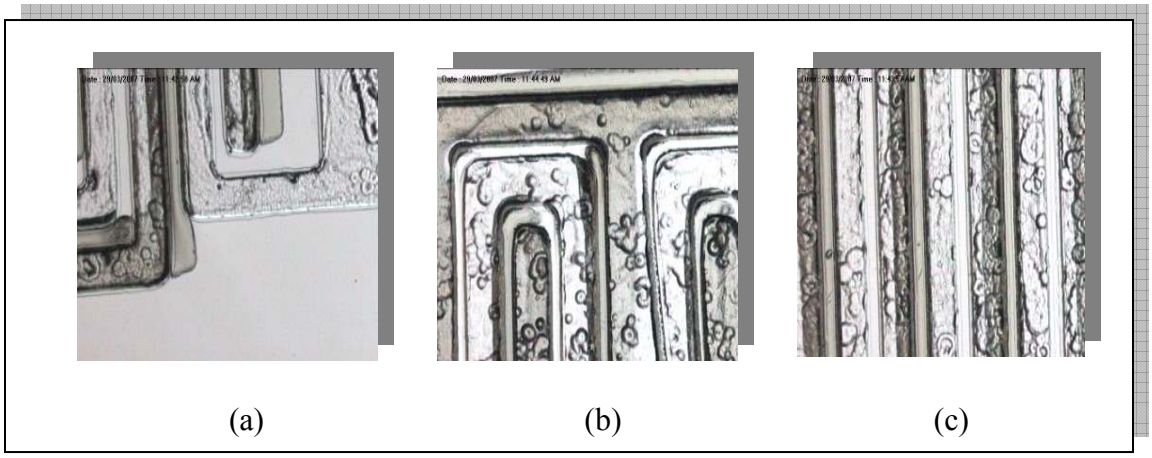
The wafer is coated with photoresist using the following spinner parameters:

- ✓ 700rpm for 5 seconds
- ✓ 3000rpm for 25 seconds
- ✓ 0 rpm for 5 second

Soft bake, exposure and development were made using the same parameters used while transferring pattern for mask 1. Mask alignment was relatively simple as the image was seen clearly. Developing however posted another setback. Aluminium was etched away at the same time during development in the developer solution. One of the crucial substance in the developer is phosphoric acid, which is also the active ingredient for aluminium etch. This factor only becomes a problem if mask 2 is misaligned. Aluminium

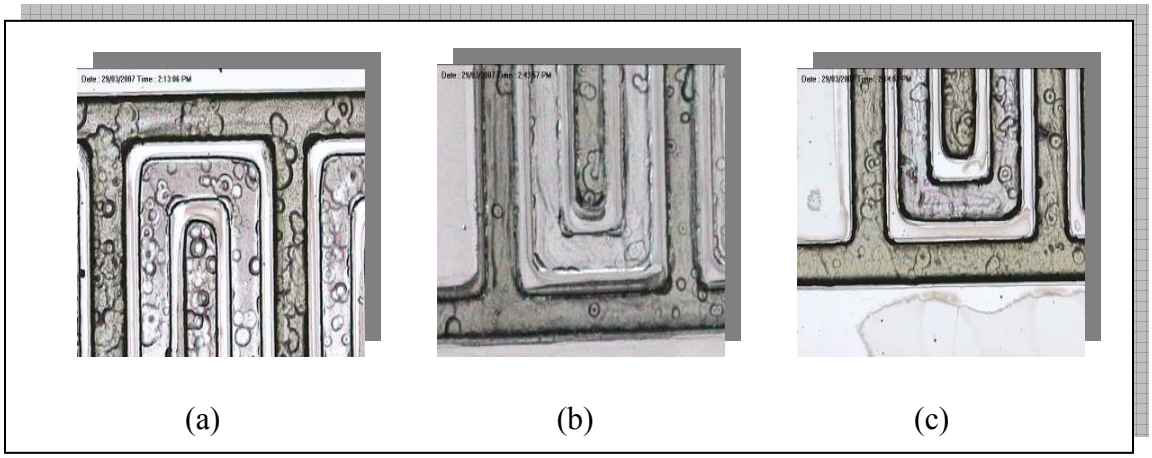
deposition process has to be repeated each time there is a misalignment as part of the aluminium is etched.

After development, the image was not clear. Only slight traces of yellowish resist were noticeable. The wafer was visualised under a high power microscope.



(a) (b) (c)

Figure 4.11: Misalignment during the first attempt of mask 2 pattern transfer in aluminium



(a) (b) (c)

Figure 4.12: Successful Mask 2 Pattern transfer on wafer

The dark areas are coated with photo resist whereas the bright channels are not. Figure 4.10 shows misalignments They are not suitable. In such case, the resist is tripped using aluminium and a new layer of aluminium is deposited using PVD before the second attempt to transfer the pattern. The second attempt was successful.

Photo resist will ac as mask for aluminium etch. So, it is hard baked at 90^{o}C for 3 minutes.

4.8 Aluminium Etch

With photoresist as mask, aluminium is etched. This process yields aluminium only where the electrodes are to be present. It took approximately 20 minutes for complete etch of aluminium in unwanted areas. The image is visualized under a high power microscope.

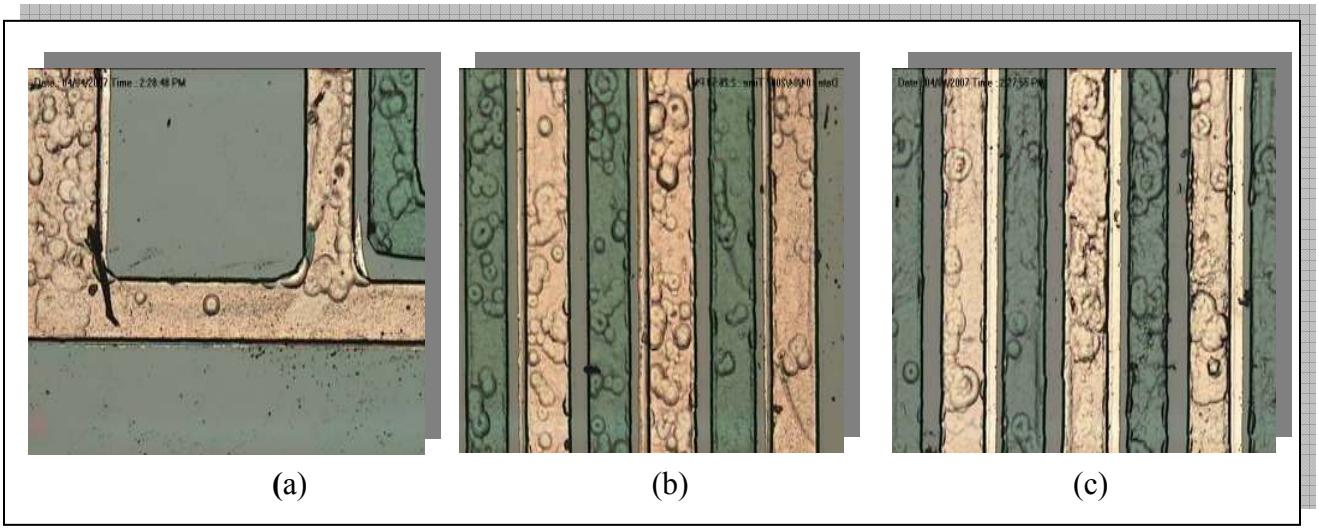


Figure 4.13: Image of surface after aluminium etch and Photo resist strip. The green areas is the oxide whereas the pinkish orange is aluminium (forming the electrode)

4.9 Anodic Bonding

This process is to bond glass and silicon using high voltage. But this process could not be done as the circuit for doing this task did not function. The lid will act as extra surface to promote capillary effect to induce flow of fluid via the channels without causing shorts. Improper bonding causes water to creep into the electrode area

4.10 Electrical Characterization

The fabricated device goes through a series of test its determine its electrical properties. Two main tests were carried out. using the Curve Tracer and Spectrum Parametric Analyzer.

A curve tracer is a special device dedicated to electrical characteristic analysis of discrete semiconductor devices. A voltage sweep is applied to the device under test (DUT) and its I-V characteristics are displayed on the oscilloscope.

A test is run on the device without fluid to check for shorts and the I-V characteristics. The probes are connected to the electrodes of the capacitor. The following elliptical curve is obtained.

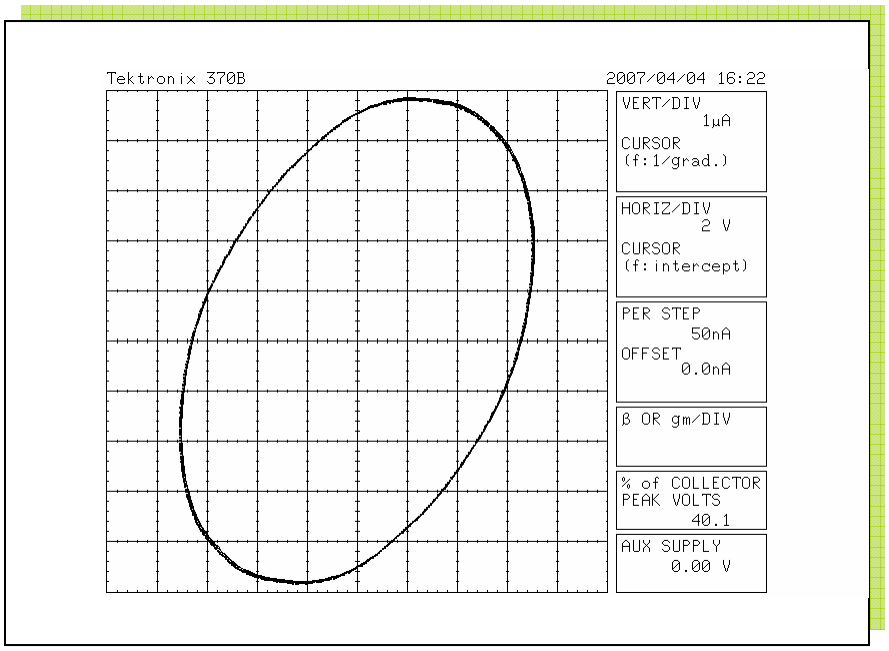


Figure 4.14: I-V Curve obtained on the Curve Tracer

This curve shown in the above figure is evidential that there are no shorts between electrodes and it is a perfect capacitor.

Another test is carried out using a spectrum parametric analyzer. This gadget also introduces a voltage sweep at specific intervals to the device under test. The I-V curve of the device is then plotted. The following depicts the images obtained plotted on Excel Sheet.

4.11 Capacitance

To determine capacitance, permittivity of silicon and silicon dioxide are essential. Permittivity refers to the degree to which a material allows the establishment of electrostatic fields. Materials with high electrostatic field readily allow electrostatic fields to be established within them. The lowest permittivity currently known is that of a vacuum, which is absence of matter. This is called permittivity, represented by the symbol ε_0 whose value is a constant at $8.85^* 10^{-12}$ F/m.

Capacitance is the measure of the ability to store charge. It is defined as:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

Where C=capacitance

ε_o = absolute permittivity

ε_r= dielectric constant

d= distance between the plates

A= overlapping area of the capacitor plates

The dielectric constant is defined as the ratio between the permittivity of the material and absolute permittivity. The area of the device is:

A = depth * surface area of electrode

= 10μm [9(20mm) + 4(0.2mm) + 3(0.6mm) + 0.4mm]

= 0.01 mm (183mm)

= 1.83 mm^2

d = 0.2 mm

Two types of insulation material is present dielectric; silicon (ε_r=11.8) and a 5000Å thick silicon dioxide (ε_r=4.42) which is negligible as it is very thin. Calculating the capacitance produces the following:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

$$C = (8.85*10^{-12})(11.8)(1.83*10^{-6}) \div (0.2*10^{-3}) = 9.55*10^{-13}\, Farad$$

Theoretically, the capacitance should be 0.955 pF which can be approximated to 1pF.

The charge up energy within the capacitor is as follows:

Energy stored, $W_{stored} = \int_0^Q \frac{q}{C} dq = \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2} CV^2 Joules$

$$W_{stored} = \frac{1}{2}\varepsilon_0 \varepsilon_r \frac{A}{d} V^2 Joules$$

$$= 0.5(8.85*10^{-12})(11.8)\frac{1.83*10^{-6}}{0.2*10^{-3}}(5)^2 = 1.19*10^{-11}\, Joules$$

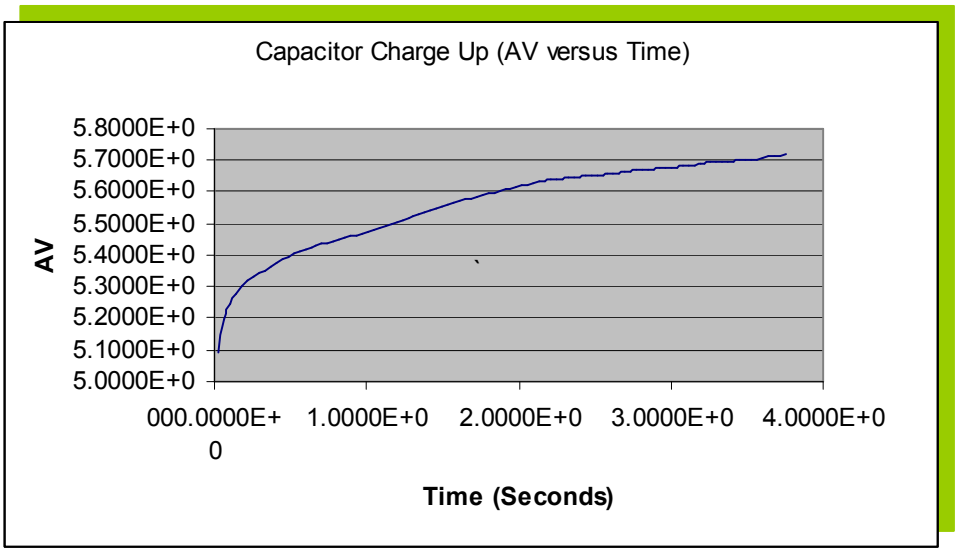


Figure 4.15: Capacitor Charge Up (AV versus time) obtained from the Spectrum Parametric Analyzer

4.12 Surface Analysis under Scanning Electron Microscope

A device is cross-sectioned and prepared for Scanning Electron Microscope viewing. The device is scribed through the middle of the device and is mounted on a holder. It is then polished to remove the micro cracks. This process also smoothens out the surface to obtain better surface images.

A 1 cm by 1 cm sample is prepared with a cross section of the device on one side. The sample is polished using 3µm texmet for approximately 1 minute. The sample is viewed under low power microscope to see if the creases and lines are still present. One minute polishing was adequate to remove them. Another step of polishing is done to remove tiny lines and micro cracks using 1µm texmet for 1 minute. Then, the sample is aligned into the SEM chamber. The following were the images obtained:

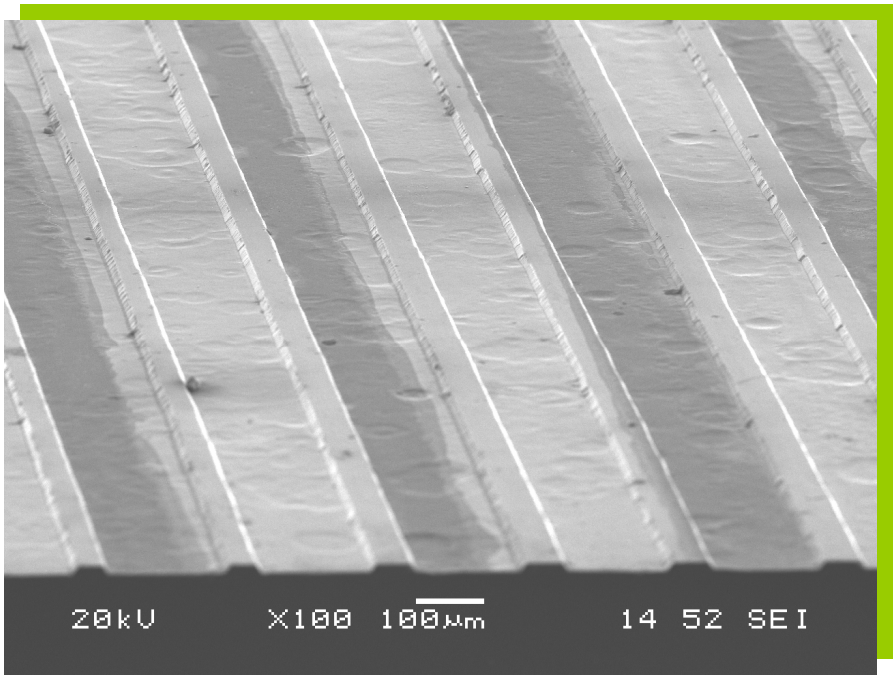


Figure 4.16: 100 times magnification of surface.

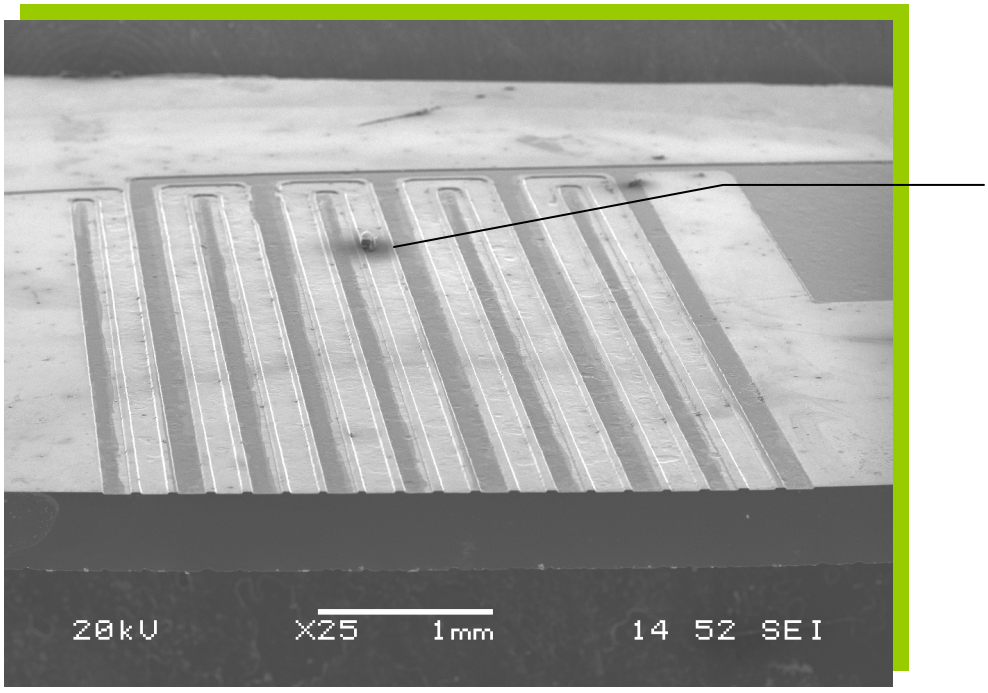


Figure 4.17: 25 times magnification of device surface showing the channels etched for aluminium electrodes and fluid channels.

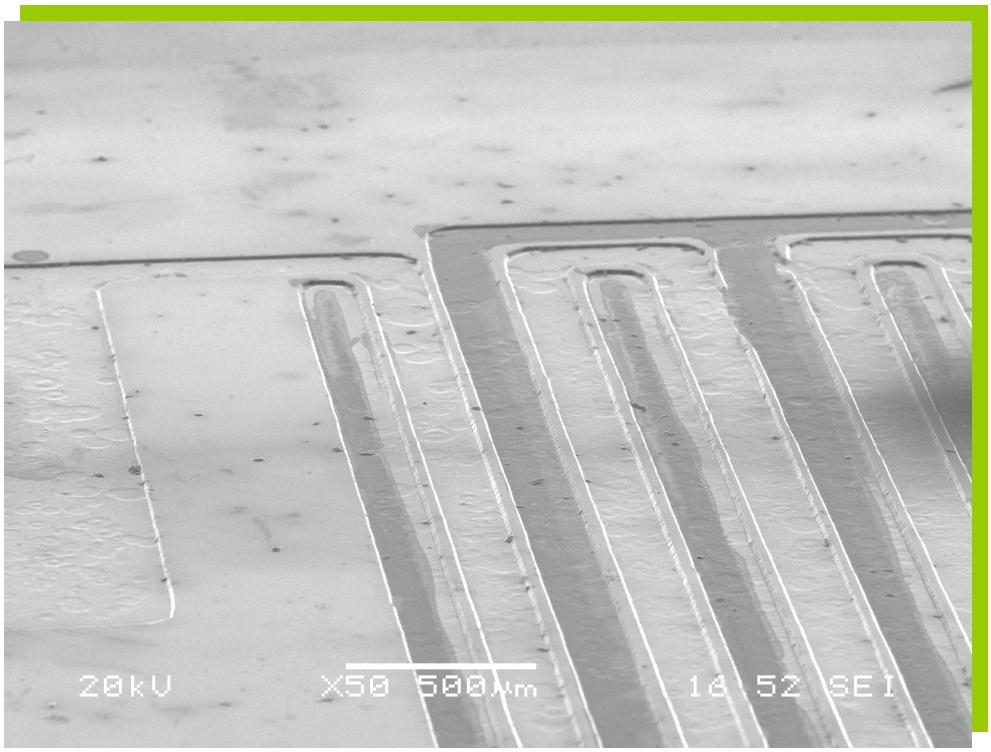


Figure 4.18: 50 times magnification of device surface. The channel boundaries are formed well.

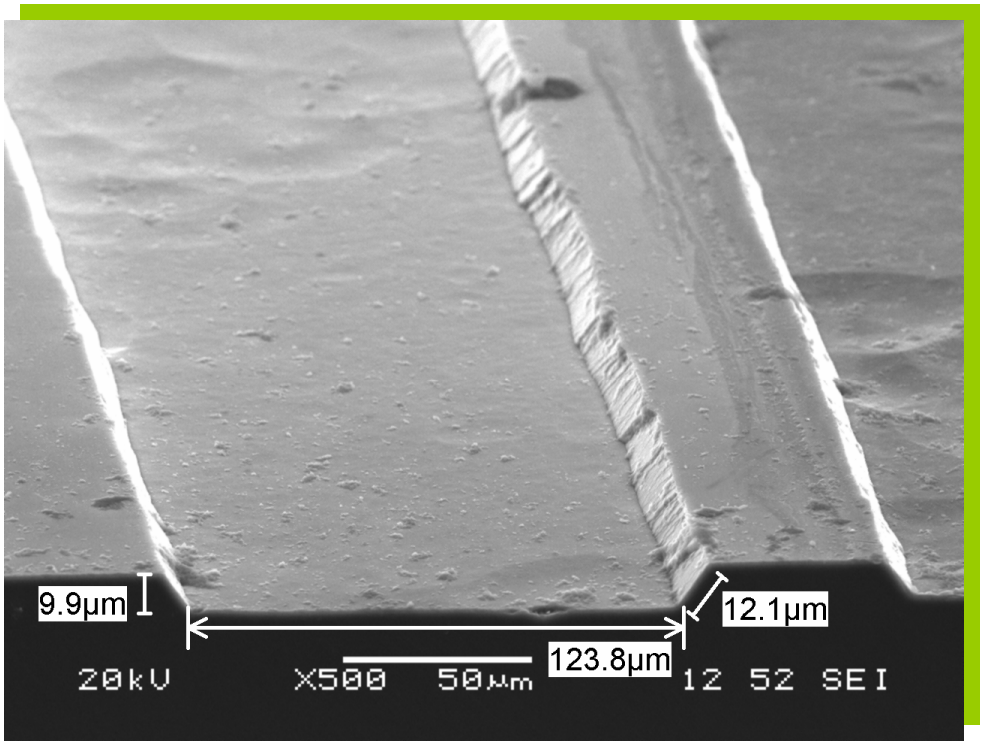


Figure 4.19: Dimensions of the channels formed. The V-groove is obtained when <100> orientation wafer is used and KOH is used as etchant.

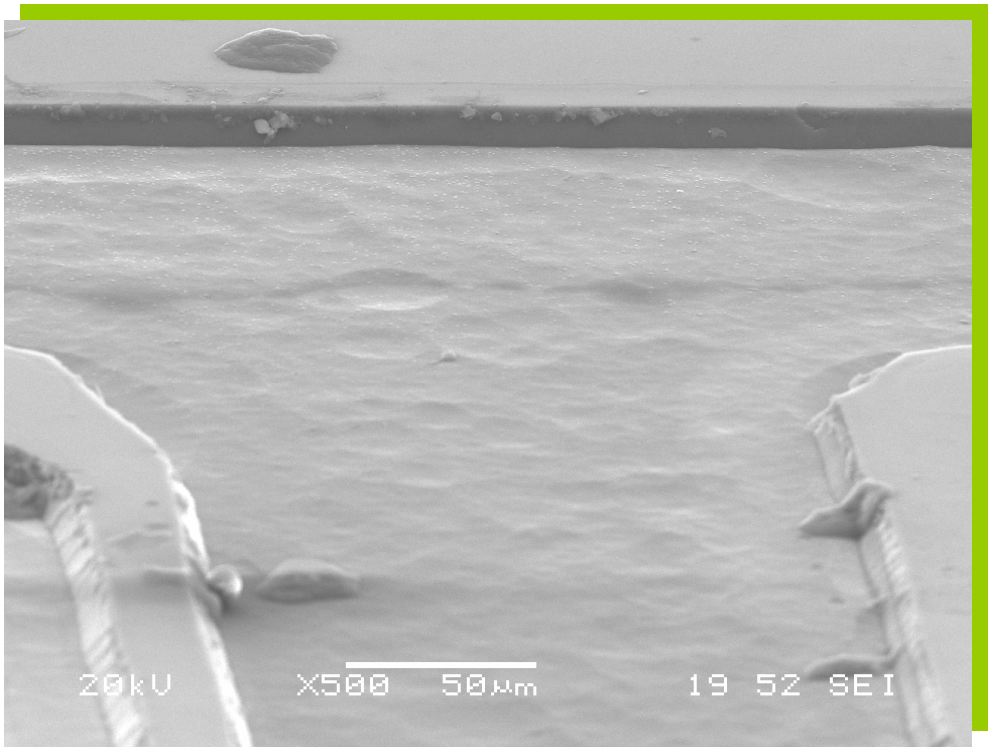


Figure 4.20: The side walls formed are not smooth. However, this profile does not disrupt the normal functionality of the capacitor. The Laminar Flow based on Reynold's number may change due to the rough etch profile.