



Implementation of 128/256 Bit Data Bus Microprocessor Core on FPGA

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Abstract

This paper shows the implementation of a large data bus size microprocessor core of 128/256 bits on an Altera Stratix 2 FPGA using a superscalar architecture of 3 parallel pipes with 4 stage pipeline as shown in Figure 1. The system level implementation utilizing the implemented microprocessor core on FPGA is shown in Figure 2. The micro-architecture of the microprocessor core architecture of Figure 1 is implemented using four pipe stages of fetch, decode, execute and writeback with a shared register file for all 3 parallel pipes, as shown in Figure 3.

Keywords: Large data bus size microprocessor, VLIW, FPGA

1. Introduction

Microprocessors have grown in its data bus size since the early days of the invention of a microprocessor. Today, most microprocessors in the market are at 32 bits, while the latest microprocessors from IBM, Intel and AMD are at 64 bits. To further enhance the capability of a microprocessor to process more data bits per clock cycle, there are two possible paths:

1. Increase the bit size of the microprocessor to 128/256 bits. The larger the bit size, the more data can be crunched in a single clock cycle
2. Implement multiple microprocessor cores in a single microprocessor unit. For example, Intel's Pentium 4 Dual Core and AMD's Athlon Dual Core both have two microprocessor cores within a single microprocessor unit. And latest from both Intel and AMD are new microprocessors with quad core. Many articles and white paper have been published by Intel, AMD and IBM on multiple core microprocessors as referenced in "References" Section of this paper.

The two methods of increasing data bus size of a microprocessor and using multiple microprocessor cores to increase the processing capability both have

its advantages and disadvantages. Both methods yield different design issues and different engineering limitations. Using a multiple core microprocessor allows a proven existing single microprocessor core to be used in a dual or quad configuration as opposed to redesign of a microprocessor for large data bus size of 128/256 bits. Multiple core microprocessor does not need major rewriting of software OS as compared to the need to do major software OS recoding for 128/256 bits microprocessor. However multiple microprocessor core have the disadvantage of sharing the memory bus between multiple core compared to a 128/256 data bus size microprocessor. Thermal dissipation is also more severe on a multiple core microprocessor as compared to a 128/256 data bus size microprocessor. This paper looks into implementation of a 128/256 bit data bus microprocessor core on an FPGA. An obvious method to increase the data crunching capability of microprocessors is by increasing its data bus size. This allows the microprocessor to crunch more data in a single clock cycle, and is ideally suited for data mining applications.

When the data bus size is doubled from 64 to 128, power consumption increases. Thermal management becomes more complicated due to the increase in power consumption. The die area of the microprocessor also increases due to:

- a. Paths and logic have to be duplicated to cater to the larger data bus size. This would lead to more logic and larger die size.
- b. Having 128/256 bits data bus size means that the amount of metal routing on silicon for that bus will have to be increased to 128/256. This will increase the physical layout area of the design and results in larger die size. As the die size increases, the probability of having defects per wafer also increases. This means that yield will drop therefore further increasing the cost of the large bit size microprocessor.



Increasing the data bus size from 64 bits to 128/256 means that the internal core logic of the microprocessor will also need to increase its computation capability to accommodate 128/256 bits. This means more logic and hence slower and larger design.

When the bit size increases, software and OS support must be updated to take advantage of the additional data bus size. Most software and OS today only supports 32 bits and 64 bits operations. To fully utilize the crunching capability of 128/256 bits, the software and OS must be updated to address the larger data bus size.

The remainder of the paper is organized as follows: Section (2) focuses on the top level architecture and micro-architecture of the microprocessor core, Section (3) focuses on the detail implementation results of a 64 bit data bus VLIW microprocessor core on an Altera FPGA, with its data bus expanded to 128/256 bits, and Section (4) concludes the findings of this paper.

2. Top Level Microprocessor Architecture and Micro-architecture for FPGA Implementation

A 64 bit custom instruction set microprocessor core is implemented on Altera's Stratix 2 FPGA (EP2S180F1508I4) using a minimal customized instruction set of 16 instructions targeted for basic Boolean functions and barrel shifting functions:

1. nop
2. add
3. sub
4. mul
5. load

6. move
7. read
8. compare
9. xor
10. nand
11. nor
12. not
13. shift left
14. shift right
15. barrel shift left
16. barrel shift right.

Altera's EP2S180F1508I4 FPGA is used as it needs to have adequate elements and enough usable IO pins for implementation of the microprocessor core.

The implemented microprocessor core is a 4 stage pipeline, 3 parallel pipes superscalar VLIW microprocessor. VLIW is chosen as opposed to CISC/RISC due to the ease of scalability of a VLIW microprocessor. The microprocessor core is designed with a shared register file with 16 registers accessible by all 3 pipes. Each register's width is the same as that of the data bus. Figure 1 shows the top level block diagram of the microprocessor core.

Figure 2 shows the system level implementation utilizing the microprocessor core implemented on FPGA. The cache, prefetch, branch prediction is implemented external to the microprocessor core on the system level as the FPGA (implemented microprocessor core) has limited resource that can only fit so much logic.

Figure 3 shows the micro-architecture of the 4 stages (fetch, decode, execute and writeback and shared register file).

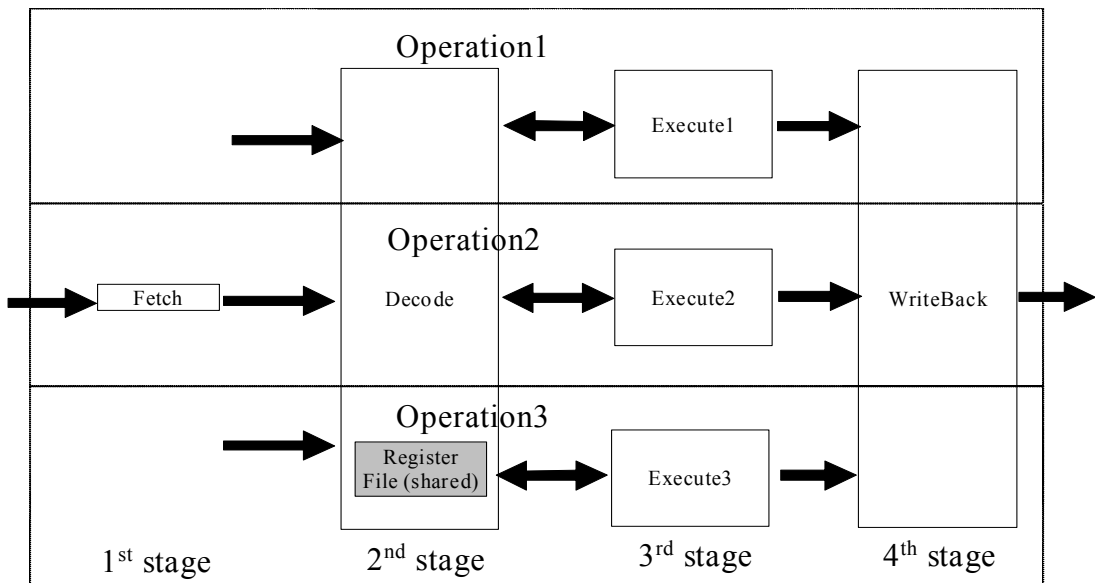


Figure 1. Top level block diagram of superscalar pipeline VLIW microprocessor core



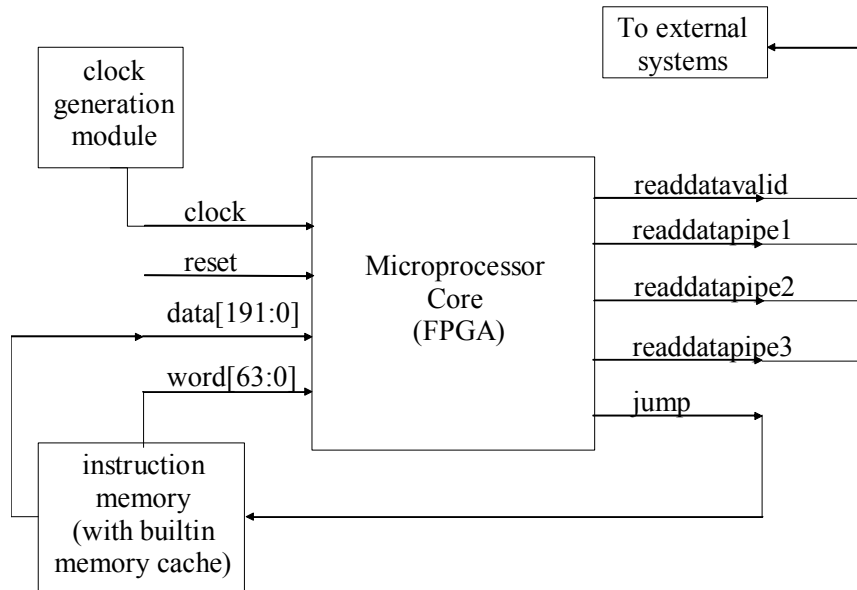


Figure 2. System level implementation utilizing microprocessor core on FPGA

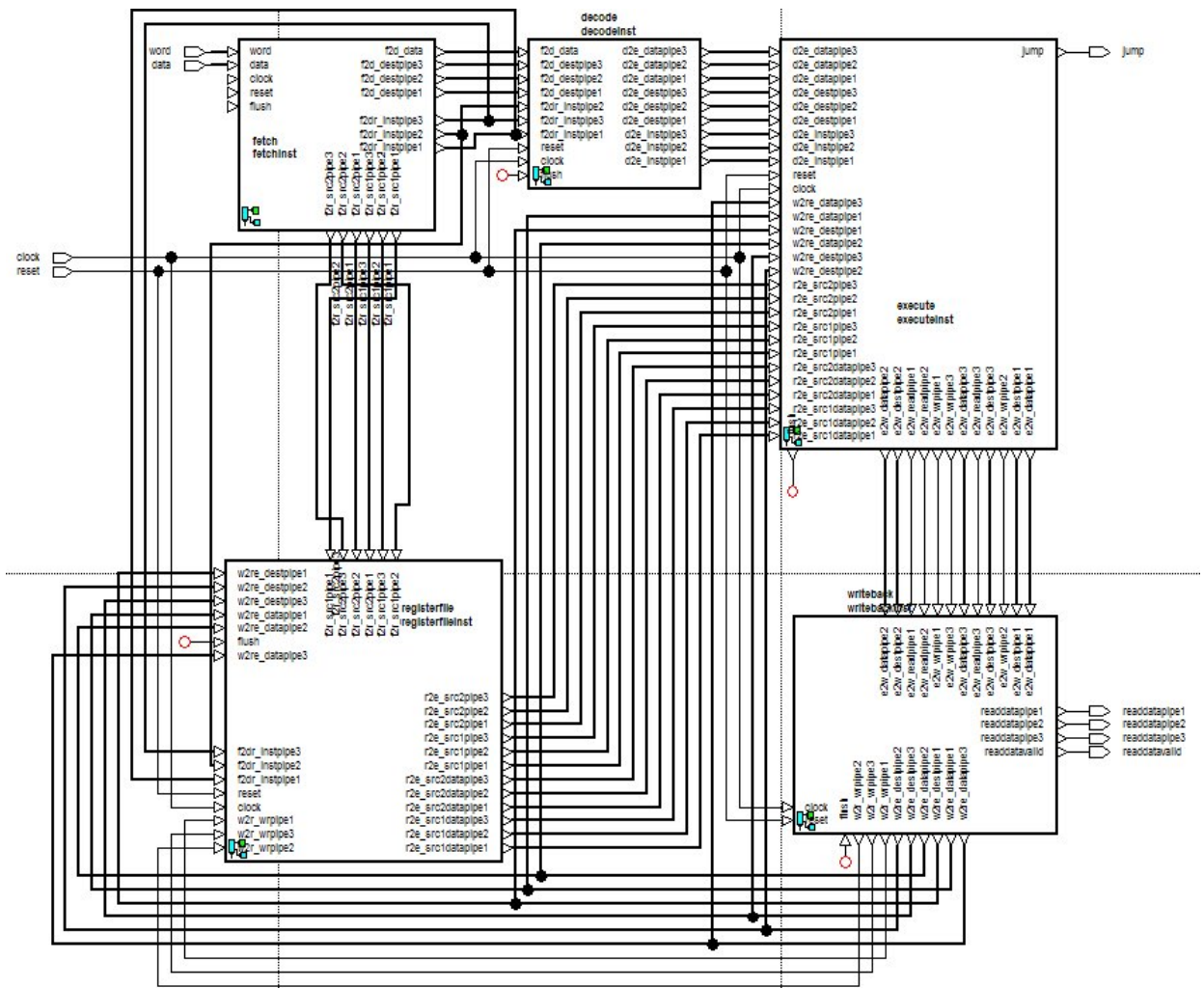


Figure 3. Micro-architecture diagram showing 4 pipe stages (for 1 parallel pipe) of superscalar pipeline VLIW microprocessor core



The execute stage of all 3 parallel pipes are also designed with register bypass mechanism to cater for all cases of instruction dependency. For an n (n=3 to 6) pipe superscalar pipeline microprocessor, the register bypass mechanism must cater for a total of y number of conditions that require register bypassing.

$$\text{Intra-pipe register bypass conditions} = n(n + 2)$$

$$\text{Inter-pipe register bypass conditions} = n^4 + n^2 - 2n$$

$$\text{Total conditions} = y = n^4 + 2n^2 = 81 + 15 = 99$$

Register bypass logic is implemented for all 15 conditions of intra pipe and 84 conditions of inter pipe bypass, resulting in a total of 99 bypass conditions implemented.

3. Implementation of a 64 Bit Data Bus Microprocessor Core on FPGA

Each pipe stage for all 3 parallel pipes in the microprocessor core are designed in verilog RTL and synthesized onto Altera's EP2S180F1508I4 FPGA using Altera's Quartus II full version 6.0 (synthesis, fitting, P&R) while verilog RTL simulation is done using Mentor Graphics's Modelsim version 6.1.

The verilog RTL is written using only combinational logic and sequential logic and does not use any IP components or library components from Altera's MegalPCore Library. For the microprocessor core in 64 bit data bus, the critical path delay, FPGA cell element usage and power consumption is analyzed.

The microprocessor core on the FPGA is then expanded to larger data bus size of 96/128/160/192/224/256 bits and the same data is collected for each implementation. When the

microprocessor core's data bus size is expanded from 64 bits to larger data bus size, the internal core logic as well as the system level logic is expanded to accommodate the microprocessor core's larger data bus size.

From the results obtained, the normalized power-delay product for each data bus size implementation is calculated and plotted as shown in Figure 4. Referring to Figure 4, the power-delay product increases by 3x when the data bus size is increased from 64 to 128 bits. When the data bus size is increased from 64 to 256 bits, the power-delay product increases by 13x. This shows a steep increase in power-delay product when the data bus size is increased fourfold to 256 bits.

The FPGA cell element usage is plotted and shown in Figure 5. Referring to Figure 5, ALUTs' increases by 1x when data bus size increased from 64 to 128 bits. It however increases by 5x when the data bus size is increased from 64 to 256 bits. The sequential elements (registers) increases by 1x when data bus size increased from 64 to 128 bits. It increases by 3x when the data bus size is increased from 64 to 256 bits. The DSP 9 bit block element increases by more than 2x when data bus size increases from 64 to 128 bits. It however increases by almost 10x when the data bus size increases from 64 to 256 bits. The steep increase in DSP 9 bit block element is due to larger ALU that requires computation of larger chunks of data as the data bus size is increased. For the total FPGA cell elements usage, it increases by 1x when data bus size increase from 64 to 128 bits. However when data bus size increase from 64 to 256 bits, the total FPGA cell elements usage increases by 4.6x.

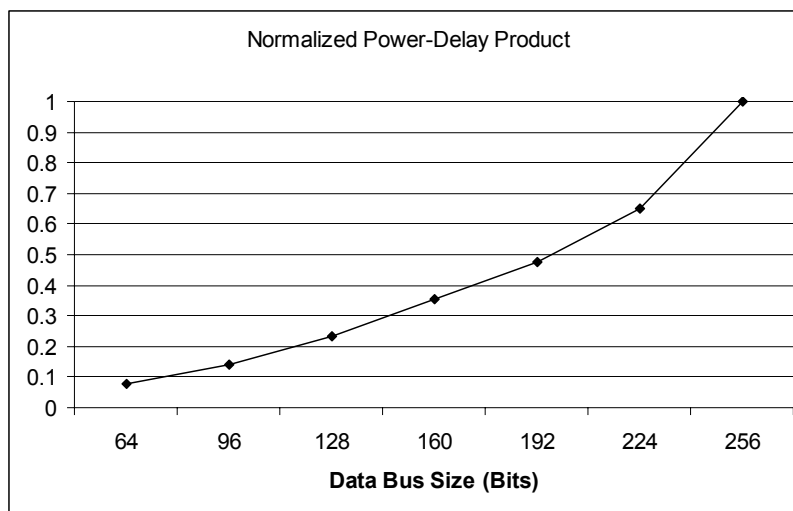


Figure 4. Normalized power delay product for microprocessor core on different data bus size



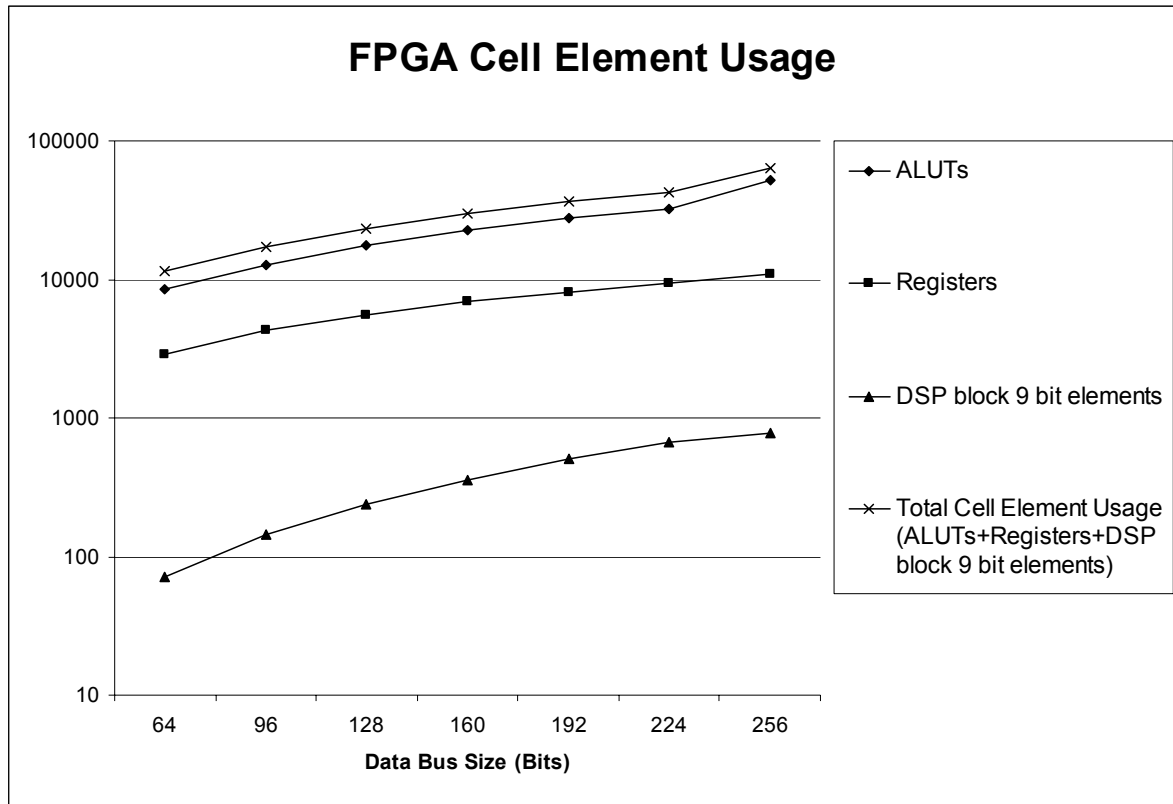


Figure 5. FPGA cell element usage for microprocessor core on different data bus size

4. Conclusion

From the results of the implemented microprocessor core on FPGA as shown in Figure 4 and Figure 5, increasing the data bus size comes at a certain cost. To double the data bus size from 64 bits to 128 bits results in an increase of 3x in power-delay product and an increase of 1x in total FPGA cell elements usage. However when the data bus size is quadrupled to 256 bits, there is an increase of 13x in power-delay product and an increase of 4.6x in total FPGA cell elements usage.

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