

## **High efficiency, good linearity, and excellent phase linearity of 3.1-4.8 GHz CMOS UWB PA with a current-reused technique**

### **Abstract**

This paper describes the design of 3.1 to 4.8 GHz CMOS power amplifier (PA) for ultra-wideband (UWB) applications using 0.18- $\mu\text{m}$  CMOS technology. The UWB PA proposed here employs cascode topology with a current-reused technique to enhance the gain at the upper end of the desired band, an inter-stage inductor, and a resistive feedback at the second stage to obtain the flatness gain. The measurement results indicated that the input return loss ( $S_{11}$ ) was less than -5 dB, output return loss ( $S_{22}$ ) was less than -8 dB, and average power gain of 10.3 dB with a flatness about 0.8 dB. The input 1 dB compression point about -2 dBm and excellent phase linearity (group delay) of  $\pm 135$  ps across the whole band were obtained. Moreover, a very high power added efficiency (PAE) of 40.5% at 4 GHz with 50 $\Omega$  load impedance was achieved with a power consumption of 24- mW.