THERMAL-MECHANICAL ANALYSIS OF BONDING PAD IN INSULATED GATE BIPOLAR TRANSISTOR

by

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LIST OF ABBREVIATIONS

BOL	Bond-On-Lead
CTE	Coefficient of Thermal Expansion
Cu-TSV	Copper-filled Through-Si Vias
DCB	Direct Copper Bonded
ELK	Extremely-Low-k
ESTRN	Equivalent Strain
fcFBGA	fine-pitch Flip chip Ball Grid Array
FEA	Finite Element Analysis
HVPT	High Voltage Planar Technology
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IMC	Intermetallic Compound
JBS	Junction Barrier Schottky
LF	Lead-Free
PCB	Printed Circuit Board
PP	Press Pack
SBD	Schottky Barrier Diode
SOC	System On Chips
TIM	Thermal Interface Material
UBM	Under Bump Metallization
WLUF	Wafer-Level Underfill Film

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LIST OF SYMBOLS

Al	Aluminium
Cu	Copper
Ni	Nickel
Si	Silicon
SiC	Silicon Carbide
SnAg	Tin-Silver

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Transistor Bipolar Bertebat Berdasarkan Analisa Pakej untuk Kedua-dua Mechanikal dan Terma

ABSTRAK

Dalam pembangunan teknologi interkoneksi cip yang tersusun, analisis haba pada cip tersusun biasanya terlibat dalam produk semikonduktor. Walau bagaimanapun, isu-isu terma bukanlah kriteria utama untuk konfigurasi cip tersusun, tetapi membawa kepada kajian kesan tegasan ini adalah bergabungan terma dan mekanikal. Memandangkan kewujudan pelbagai cip dan bahan lain dengan pekali pengembangan terma yang berbeza, pemuatan terma-mekanikal dan kesannya terhadap kegunaan perlu dikaji untuk reka bentuk interkoneksi dan konfigurasi cip. Tujuan penyelidikan ini adalah: a) analisis terma-mekanikal pada pencantuman dengan interkoneksi cip tersusun dengan menggunakan analisis elemen kecil, b) kajian satah pencantuman cip tersusun untuk memperbaiki interkoneksi. Penyiasatan dilakukan dengan memodelkan Transistor Bipolar Insulated-Gate (IGBT) dengan wirebonds berdasarkan penyelidikan yang dijalankan Dudek et al. 2015. Model ini berfungsi sebagai asas untuk perbandingan. Model ini mengalami pemanasan dan penyejukan kitaran dengan delta suhu 150K dan tekanan yang dialami oleh model pada antara sambungan antara ikatan dawai dan plat asas dicatatkan pada setiap pemanasan dan kitaran penyejukan. Ujian ini diulang menggunakan model IGBT dengan ikatan dawai yang diganti dengan ikatan planar, dan keputusan tekanan dibandingkan. Hasil pemodelan terma sepadan dengan pemodelan Dudek et al, menunjukkan daya maju model. Analisa mekanik menunjukkan tekanan dalam interkoneksi antara ikatan dawai dan plat asas adalah tertinggi di pinggir sambungan dan analisa ini sama untuk ikatan planar. Keputusan analisis menunjukkan tegasan tinggi dalam cip tersusun pada suhu rendah. Kaedah satah pencantuman menawarkan penambahbaikan yang ketara berbanding dengan pencantuman tradisi dari segi tegasan interkoneksi dan oleh itu berdaya maju untuk meningkatkan tekanan terma-mekanikal dalam cip tersusun.

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Insulated Gate Bipolar Transistor (IGBT) Based On Package Analysis For Both Mechanical and Thermal

ABSTRACT

In development of the die stacking interconnection technology, the thermal analysis on stacked dies are commonly engaged in semiconductor products. However, thermal issues are not the main criteria for stack die configuration and thus the combined effects of thermal and mechanical stresses are overlooked during the design of the stacked dies. As there are existence of multiple dies and other materials with different Coefficient of Thermal Expansion (CTE), thermo-mechanical loading and its effect on reliability needs to be studied for optimum the interconnection design and die configuration. The focus in this thesis is a) thermal-mechanical analysis on the wirebond interconnection of stacked die by using element analysis, b) the study of planar bonding of stacked die to improve of interconnection. The investigation is carried by modelling an Insulated-Gate Bipolar Transistor (IGBT) with wirebonds based on an investigation carried out Dudek et al. 2015. This model serves as a basis for comparison. The model undergoes cyclic heating and cooling with a temperature delta of 150K and the stress experienced by the model at the bonding interface between Wirebond and Baseplate is recorded at the of each heating and cooling cycles. The test is repeated using a model IGBT with the wirebond replaced with a planar bond, and the stress results are compared. The results of the thermal modelling matches the model by Dudek et al, showing the viability of the model. Thermo-mechanical analysis shows stress in the interconnection between wirebond and baseplate is highest at the edges of the interconnection and is the same for the planar bond. The results of the analysis show that the stresses in a stacked die are highest at low temperature. The planar bonding method offers a marked improvement over the wirebond in terms of interconnection stress and thus is a viable for improving the thermo-mechanical stresses in a stacked die.

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CHAPTER 1: INTRODUCTION

1.1. Introduction

In recent years, new interconnection technologies have been developed and introduced in semiconductor application to achieve the requirements of higher energy efficiency and to be able to operating at harsh environments (Haiwei Jin, 2016). Due to the faster the processing system in silicon devices, higher switching power loss and higher temperatures are generate which reduced the reliability and robustness of the powered devices.

Several researchers and companies are focused on bonding techniques for a low temperature bonding process to reduce stress. The purpose of the studies are to identify the thermal characteristic and mechanical performance of a stacked dies. Realistic transient temperature loadings as well as mechanical stress are simulated by thermo-mechanical finite elements analysis for multi stack dies. (Iniewski, 2011), (Kei Murayama, 2015), (Tan, 2012).

Considering the die bonds of the powered devices, thermo-mechanical performance are simulated with theoretical investigations. The results of the analysis are observed by some of the failure modes. The application of the methodology for analysis of the interconnection are performed by using the example of Insulated Gate Bipolar Transistor (IGBT). (Vanessa Smet, 2011), (HuaLu, 2009), (R. Pittini, 2011), (Z.Khatir, 2004) et al. The properties of selected materials are applied to the geometry of the design for evaluation. The temperature and stress changes of the designed devices are evaluated and discussed based on their respective characteristic using non-linear finite element analysis.

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In the thesis, the latter technologies is the so called “planar technology” which mainly to replace the bonding wires are discussed. It is because this new technology is possible to overcome the fatigues of interconnection in silicon devices. (R. Dudek R. D., 2017), (Rahimo, Kopta, & Linder, 2006).

1.2. Problem Statement

The inefficiency of the current interconnection inside powered devices had brought out the discussion of this thesis. The purpose of this assessment is further narrowed down to the thermo-mechanical loading stress on the interconnection of an IGBT and stacked die. The thermo-mechanical study can investigate the effects of the temperature changes which directly affects the loading stress of the wirebond of IGBT. The weakness of the wire bond as the interconnection also needs to be reviewed for further improvement purposes. A solution is provided by changing the design of the interconnection of stacked die from wirebond to planar bond to reduce the fatigue failure. A planar bond is introduced to improve the reliability of the bonding when loading stress happen due to the changes of temperature.

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1.3. Objectives

Improvement on the reliability of thermo-mechanical design of interconnection technology is the subject to this thesis. The focus of the study is simulation of thermal stress on IGBT interconnection and the analyses of the results of the framework. New design of interconnection is introduced to overcome the weakness of conventional joining technology.

Particularly, the study has the following objectives:

1. To validate the IGBT module design with previous studies according thermo-mechanical analysis
2. To perform thermo-mechanical analysis on the interconnection between wirebond and base plate on an IGBT package and investigate the effects of thermal stress on the interconnection.
3. To repeat the thermo-mechanical analysis on a planar bond to investigate its improvements to fatigue performance on the interconnection.

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CHAPTER 2: LITERATURE REVIEW

2.1 Introduction

The literature review shows the past studies are mainly focused on understanding and modeling thermo-mechanical analysis on the Insulated Gate Bipolar Transistor (IGBT) package and stacked dies. What has been missing in the past studies is a comprehensive and structured approach in managing the construction of this research. The overall goals of this chapter are to evaluate the different methodologies used in past research discussion to identify the appropriate approach for investigating the problem statement of this research.

The literature are gathered from conference proceeding, journal articles, book section and periodic articles in websites. The review is representing the comparable results with different scopes and hypotheses which are assumed by experiments and researchers. Although the literature is not the main relevance in the research but it used to understand the results obtained from past and consider implications of the findings.

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2.2 Electro-Thermo-Mechanical Analyses on Silver Sintered IGBT-Module Reliability in Power Cycling

With the increase in the need of electronics used in harsh environments, or in higher efficiency, improvements in technology are being developed to meet these demands. For example, new interconnection technologies such as silver sintering or High Voltage Planar Technology (HVPT) (Dudek, et al., 2015) are being developed to replace soft solder interconnections. Pointed out by Wang et. l., new interconnection technologies may lead to new failure mechanisms and thermal issues (Huai Wang, 2014) and thus there is an increasing need to be able to predict the reliability of such new technologies under

thermo-mechanical loading. Figure 2.1 shows the geometry of the design, where double symmetry of the molded module is assumed in paper.

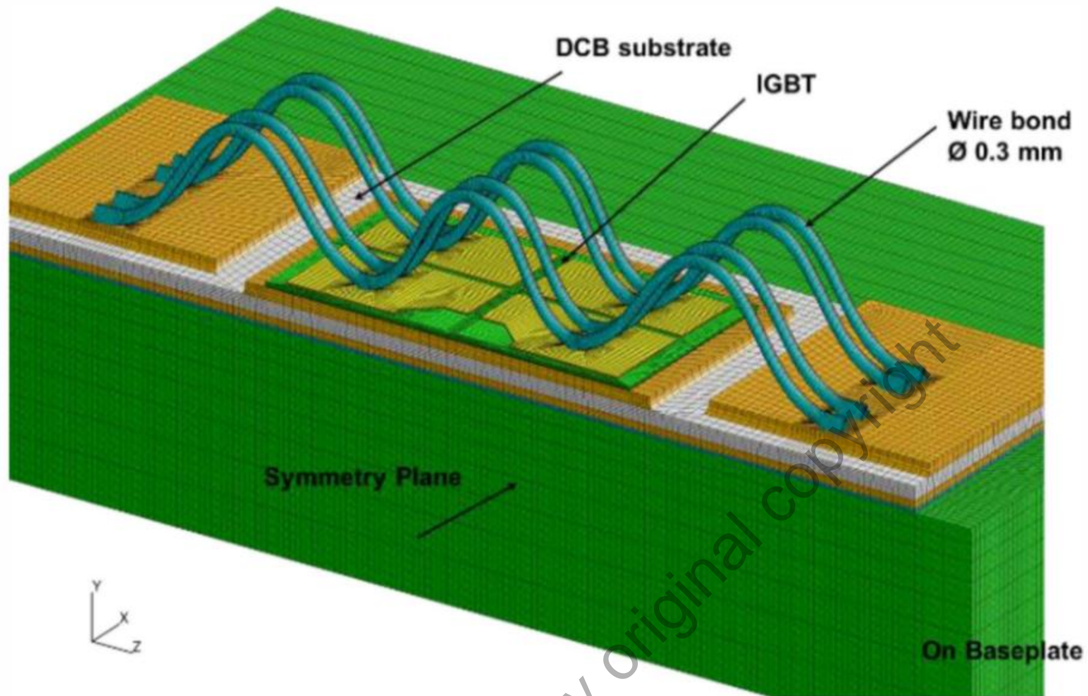

Figure 2.1 The resultant temperature field from parametric power cycling. Source: Dudek, et al. (2015).

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Frequently, Finite Element Analysis (FEA) is done to simulate the new technologies. FEA was carried by Dudek et. al. to study silver sintered die bond in comparison with soft solder die bonding. The study simulated an IGBT module under active power cycling, with particular attention at interconnect between baseplate and die.

The results of this study shows that stress and strain in an IGBT-module differs when differing bonding techniques are used (Dudek, et al., 2015). In particular, silver sintered baseplate suffer much less plastic strain as compared to soldered baseplate, which the study deduced to be due to the stronger coupling by the silver sintered bond. Figure 2.2 shows the stress distribution pattern at the baseplate after cooling down in the first cycle.

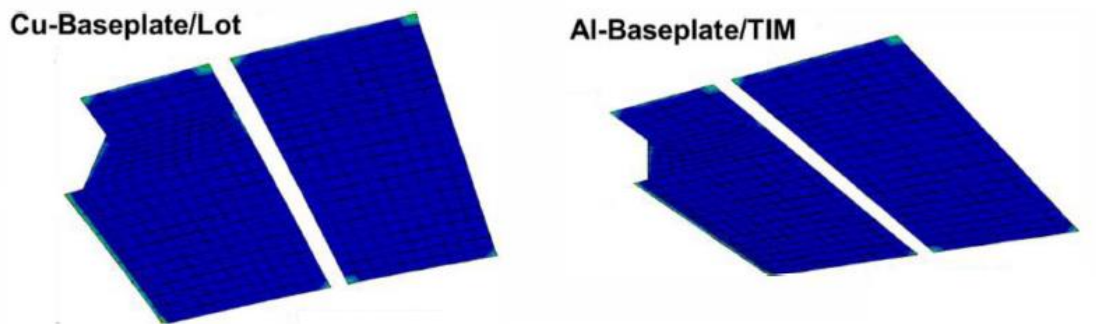

Figure 2.2 Equivalent plastic strain in the metallization chip on die top. Source: Dudek, et al. (2015).

However, the arrangement also resulted in higher stress in the stack, with greater risk of brittle fractures and greater sensitivity to initial in homogeneities or manufacturing defects (Dudek, et al., 2015).

2.3 Non-linear finite element analysis on stacked die package subjected to integrated vapor-hygro-thermal-mechanical stress

A research paper from Jing Wang examined the vapour-hygro-thermal-mechanical stress on stacked die packages by using non-linear finite element analysis. A micromechanics based vapour pressure model was used to predict the moisture distribution under a constant temperature. Using this result, finite element analysis was then performed to combine the effects of vapour pressure, thermo-mechanical stress and hygro-mechanical stress. The paper shown the properties of thermal expansion, moisture diffusion and vapour pressure could affect the stacked die package when undergo the soldering process (Wang, 2016). Figure 2.3 shows the geometry of the stacked die package which Jing Wang was established in the finite element model.

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Figure 2.3 Schematic of the stacked die package. Source: Wang (2016).

The simulations results shown the highest Von-Mises stress is observed at the junctions of mold compound, die attach and bottom substrate. The fracture mechanics analysis determined the rate of strain energy released shows nonlinear growth against temperature during reflow, and varies with increasing initial crack lengths cause by induced stress (Wang, 2016). Figure 2.4 shows the effect of temperature on strain energy release rate with different initial crack lengths of 0.2 mm, 0.5 mm, 1.0 mm, 1.5 mm and 2.0 mm.

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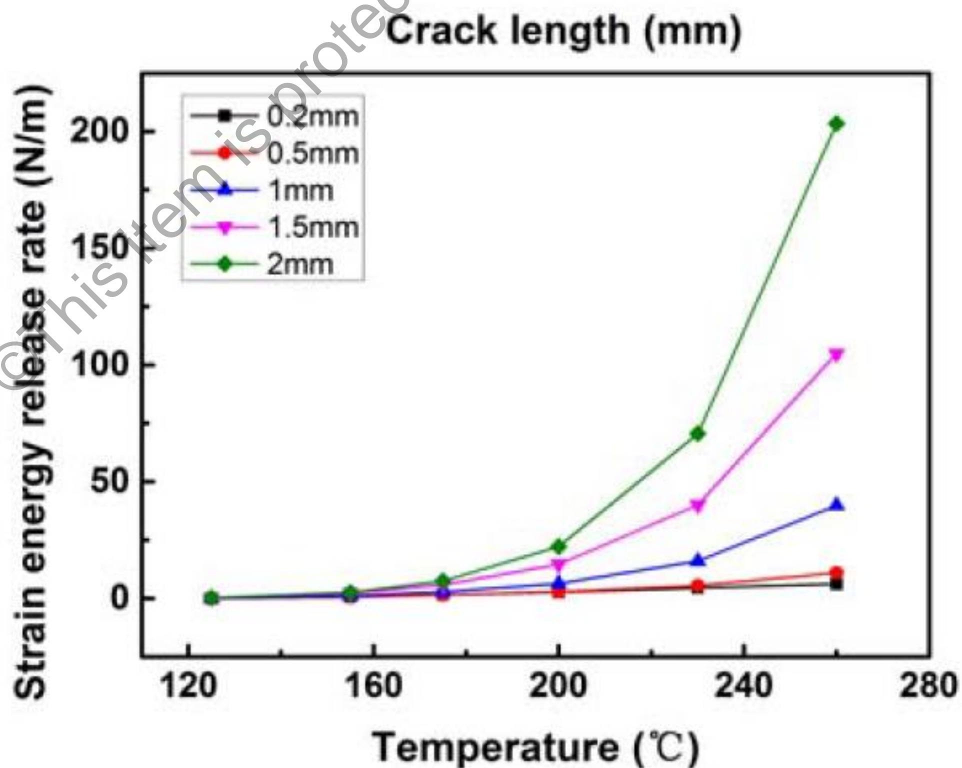

Figure 2.4 Effect of temperature on strain energy release rate. Source: Wang (2016)

However, the results of the study were limited due to the diffusion modelling being valid only under constant temperature and humidity conditions, which cannot be applied to the reflow process that contains time-dependent thermal loading.

2.4 Thermal Stress and Die-Warpage Analyses of 3D Die Stacks on Organic Substrates

The study of die-warpage in stack die assemblies by thermal stress was conducted using multi-layered beam theory. The initial experimental was tested on the 70 µm thick top dies and interconnection through metallic vias (Cu-TSVs) with 40 µm pitch full-area-array interconnection on organic laminates at several temperatures (Sayuri Kohara, 2012). Figure 2.5(a) shows the assembly of the stack die which consist of full-area-array 40 µm pitch lead-free solder joints with Cu-TSVs on Si interposer. Figure 2.5(b) shows the structure of the solder joints between the Si dies and Si interposer.

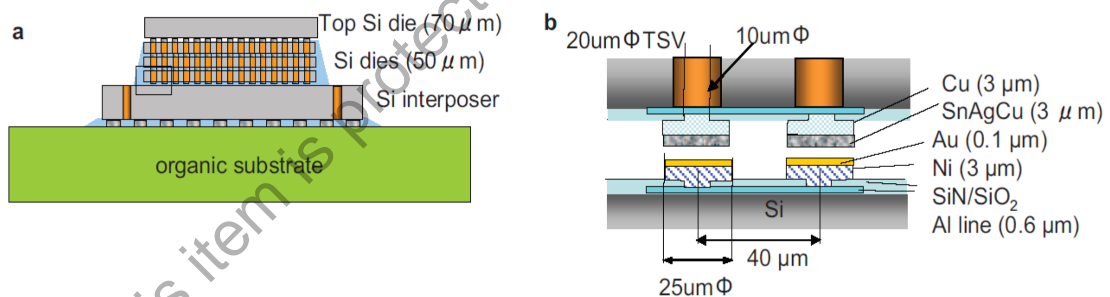

Figure 2.5 Structure of silicon stack dies with lead-free solder joints. Source: Sayuri Kohara (2012).

The low-stress intersection is simulated with silicon-dies with thickness of 50µm-100µm and is it found that the low-elasticity high CTE (coefficient of thermal expansion) bottom side encapsulation material is preferable in the die stack package over high-elasticity low-CTE material due to the better flow-ability (Krishna Tunga, 2016). The study also evaluated the intersection distances of 20 µm, 40 µm and 80 µm to show that

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the thin layer die stack with low-elasticity bottom side encapsulation materials are less vulnerable to separation at the die-edge compare with high-elasticity materials.

The die-warpage of multiple layers in the stack dies were measured to find the difference stresses between the die corners and die center. Figure 2.6(a) shows the structure of 3-layer and 4-layer of Si dies. Figure 2.6(b) shows the measurement results of warpage percentage on top surface of the contours of the solder joints. The measurement showed the silicon die was warped due to CTE disparity between top-level die without metallic vias and intermediate-level thin die with metallic vias. Thus, the analyses suggested the thickness of top-level dies needs to accommodate for the CTE disparity to decrease the die-warpage in stack packaging.

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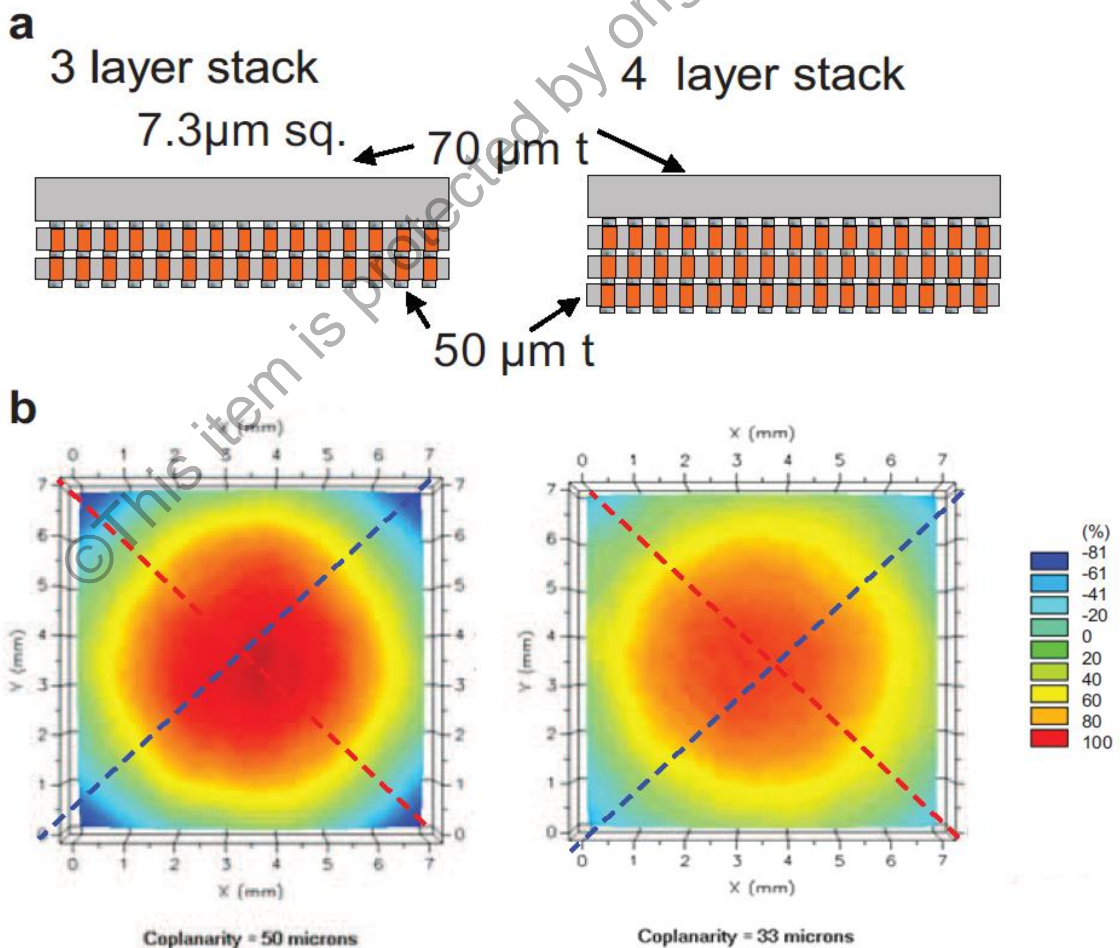

Figure 2.6 Warpage measurement results: a) Schematic drawings of die stacks b) Contours of the stress analysis of the top surface. Source: Sayuri Kohara (2012).

Nevertheless, this study is not able to show the results of how the variations of temperature affected the heat transfer between the stack dies with multiple layers of different material and how the properties of the material taken into account to cause the die-warpage when reaching the maximum temperature.

2.5 Evaluation of Cu/Ni/SnAg Microbump Bonding Processes for Thin-chip-on-chip Package using a Wafer-level Underfill Film

A novel technology of wafer-level underfill film (WLUF) was developed to study the reliability of the stacked dies of 3D integrated circuit (ICs). Figure 2.7 shows the geometry modelling of flip-chip bonding with WLUF. The purpose of this study is to resolve the interconnection of device layers without reduce system performance (Chang-Chun Lee, 2012). The warpage of stacked thin dies has represented by non-linear finite element analysis to analyses the effect of thermo-mechanical stress on the System-On-Chip (SOC).

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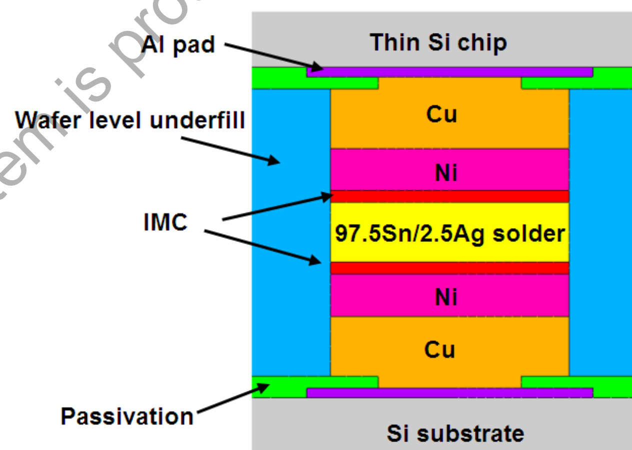

Figure 2.7 Finite Element Analysis model for thin stack dies on packaging structure. Source: Chang Chun Lee (2012).

The results of this research is closed to as discover by Sayuri Kohara in 2012 which it found that the thickness of the top dies in silicon interposer had influenced the warpage of packaging. Figure 2.8 shows the results of stress occurs on the region between

IMC layer and SnAg solder at the packaging structure. Figure 2.9 shows that max von Mise strain increase as the CTE of WLUF increases.

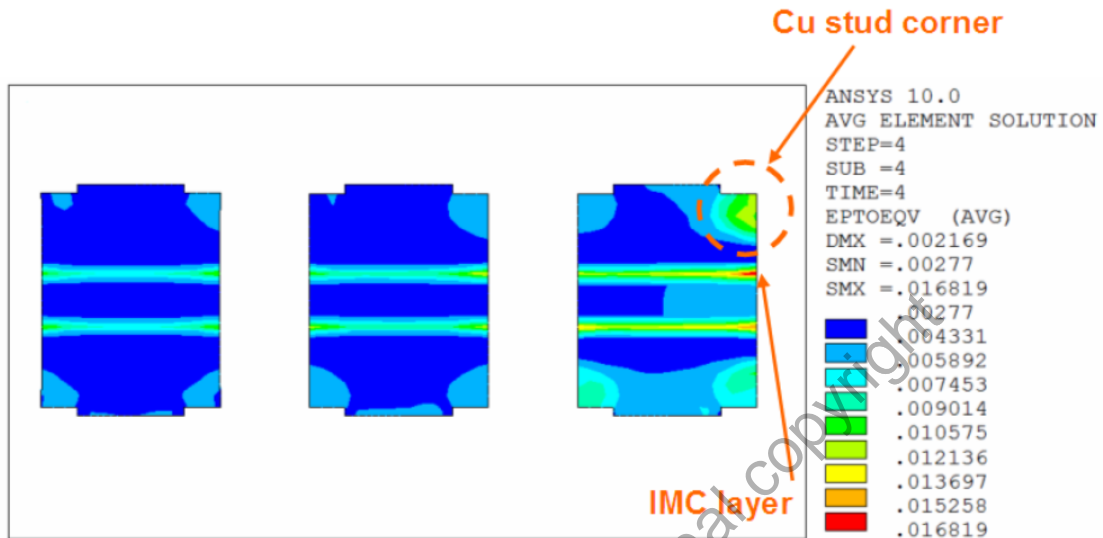

Figure 2.8 The Von Mise stress contour at a chip corner with a bonding load of 2 kg from bonding tempetature at 250 °C to ambient temperature 25 °C. Souce: Chang Chun Lee (2012).

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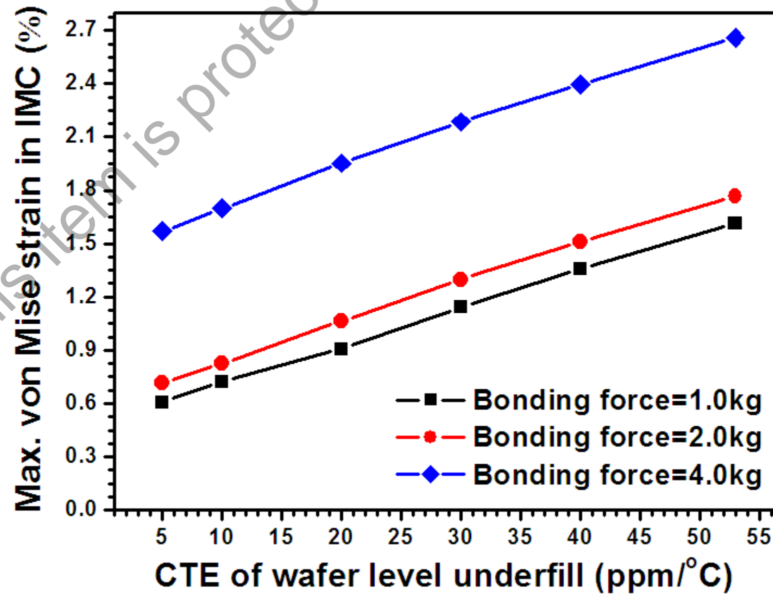

Figure 2.9 Max. von Mise strain of a chip-on chip package with a 50 μm chip thickness when a CTE change of wafer level underfill at different bonding forces is performed. Souce: Chang Chun Lee (2012).