Low Power Reconfigurable Sub-Band Filter Bank ASIC For MP3 Decoder

Abstract

There is an ever demanding need to develop low power audio devices using MP3 technology. From the profiled results of MP3 algorithm on ARM processors, it has been observed that the synthesis filter bank in the audio decoder consumes maximum power. Hence, to reduce the power consumption of the filter bank, we developed an IEEE 754 single precision floating-point runtime reconfigurable architecture. The proposed architecture consumes less power at run time as the last 12 bits of the mantissa part of the synthesis filter coefficients are zero most of the time and, hence, the corresponding multipliers will be switched off. Since the active multipliers during inverse polyphase quadrature mirror filter banks (IPQMF) are less, we are able to achieve low powered decoding process without significantly compromising on the accuracy and speed. We synthesised and simulated the architecture using 0.35 m process technology under synopsys environment. A uniform worst case power reduction of 23.7% has been achieved in the frequency range from 1 MHz to 20 MHz when all the multipliers are in active state.

Keywords

Low power reconfigurable pipelined architecture; MP3 decoder; Single precision multiplier; Synthesis filter banks