Design and Fabrication of A Wideband CMOS Continuous-Time Integrated Baseband Active Filter For A Synthetic Aperture Radar Receiver

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A thesis submittteed in fulfillment of the requirements for the degree of Doctor of Philosophy in Microelectronic Engineering

School of Microelectronic Engineering

UNIVERSITI MALAYSIA PERLIS

2016

UNIVERSITI MALAYSIA PERLIS

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Academic Session : 2015/2016

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ACKNOWLEDGEMENT

Alhamdulillah, all praise to Allah the Almighty, for giving me strength, patience and perseverance to finish up this thesis. Special appreciations to Aalto University, Finland, Professor Kari Halonen and Dr. Ville Saari for helping me with the research and giving me permissions to use the publications published when I was there. To my supervisors, Dr. Sohiful Anuar Zainol Murad and Associate Professor Dr. Rizalafande Che Ismail, thank you so much for the support and guidance. I would like to thank Universiti Malaysia Perlis (UniMAP) for giving me the chance to pursue my study here. Especially to my husband Dr. Muzamir Isa, and children, Zahirah, Sakinah and Ahmad Faheem, thank you very much for the time, space and doa. I could never repay you for all the sacrifices you have done. Thank you for believing in me. Not forgetting my parents Latifah Hassan and Abu Bakar Yahaya, my parents in law Che Nah Jusoh and Isa Sabu; your doa is one of the reason for what I am today. Last but not least, to all my friends and colleagues in UniMAP especially in School of Microelectronic Engineering and Department of Electronic Engineering Technology, Faculty of Engineering Technology, thank you for the laughter and fun time spent together for it motivates me to finish writing up this thesis.

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
APF	All Pass Filter
BER	Bit Error Rate
BB	Baseband
BiCMOS	Bipolar-Complementary-Metal-Oxide-Semiconductor
CAD	Computer Aided Design
CMFB	Common-Mode Feedback
CMFF	Common-Mode Feedforward
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DCR	Direct-conversion Receiver
DRC	Design Rules Check
DUT	Design Under Test
ESA	European Space Agency
GBW	Gain Bandwidth
GHz	GigaHertz
HD2	Second-order Harmonic Distortion
HD3	Third-order Harmonic Distortion
IC	Integrated Circuit
ICP	Input Compression Point
IDAC	Current-Steering Digital to Analog Converter
IF	Intermediate Frequency
IIP2	Second-order Input Intercept Point
IIP3	Third-order Input Intercept Point
IMD	Intermodulation

LNA	Low Noise Amplifier
LO	Local Oscillator
LOS	Line-Of-Sight
LPF	Low Pass Filter
LSB	Least Significant Bit
LVS	Layout Versus Schematic
MHz	MegaHertz
MIM	Metal-Insulator-Metal
NMOS	N-type Metal Oxide Semiconductor
OBUF	Output Buffer
OFDM	Orthogonal Frequency Division Multiplexing
PCB	Printed Circuit Board
PMOS	P-type Metal Oxide Semiconductor
PVT	Process Variations and Temperature
RAR	Real Aperture Radar
RF	Radio Frequency
RMS	Root Mean Square
SAR	Synthetic Aperture Radar
SAW	Surface Acoustic Wave
SC	Switched-Capacitor
SFB	Source Follower Based
SFG	Signal Flow Graph
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
UWB	Ultra Wideband
VGA	Variable Gain Amplifier
VNA	Vector Network Analyzer

LIST OF SYMBOLS

°	degree
λ	wavelength
ω	angular frequency
ω_{P1}	low frequency pole
ω_{P2}	high frequency pole
$e^{j\theta\omega}$	phase response
θ	phase
$\tau_{(int)}$	integrator time constant
$\bar{V}_{n,BB,in}$	integrated noise of the baseband referred to the baseband input
a_n	voltage gain from the circuit input at the *n* stage
A	amplitude
A_{DC}	DC gain
$A_{V,RF}$	RF gain
B	bandwidth
B_{RF}	RF noise bandwidth
C	capacitance
dB	decibel
D	width of antenna
$D(\omega)$	group delay
$D(s)$	denominator
f	frequency
f_1	frequency of tone 1
f_2	frequency of tone 2
f_s	spurious response frequency
g_m	transconductance

g_m-C	transconductance-C
g_o	output conductance
G	conductance
G_n	power gain expressed in absolute values of the *n*th receiver block
$\|H(j\omega)\|$	magnitude response
$H_{int(s)}$	integrator transfer function
$H(s)$	filter transfer function
I	current
Im	Imaginary number
$IIP3_n$	third-order intercept point in Watts
$IIP3_{tot}$	total third-order input intercept point
k	Boltzmann's constant $(1.38e^{-23} J/K)$
k_0	DC offset
k_1	gain of the circuit associated with a linear circuit theory
k_2	second order nonlinear component
k_3	third order nonlinear component
L	inductance
M	positive number greater than 1
n	natural number
N	positive number greater than 1, order of the filter
$N(s)$	numerator
NF_{RF}	RF noise figure
NF_{RX}	overall noise figure of the receiver
p_i	transfer function poles
P_1	input signal power
P_2	output signal power
P_{dBm}	power in dBm

$P_{in,min}$	sensitivity of the receiver
P_{IN}	fundamental input signal power
$P_{IMD2,IN}$	input-referred second-order intermodulation power
$P_{IMD3,IN}$	input-referred third-order intermodulation power
$P_{IMD3.OUT}$	output third-order intermodulation product
P_{OUT}	fundamental output signal power
$Q_{1,eff}$	effective quality factor of the first stage
Q_{int}	integrator quality factor
R	Resistance
Re	Real number
R_L	load resistance
R_S	source resistance
SNR_{min}	minimum signal to noise ratio
t	time
T	absolute temperature $(290\ K)$
$T(j\omega)$	magnitude
$T(s)$	filter transfer function
v_{IMD2}	second order intermodulation term
v_{IMD3}	third order intermodulation term
V	voltage
V_{dBV}	voltage in dBV
V_{in}	input voltage
V_{out}	output voltage
$V_{OFF,TOT}$	total offset voltage
z_i	transfer function zeros

Pembangunan Penapis Aktif Jalur-lebar Laluan-rendah CMOS untuk Penerima Radar Bukaan Sintetik (SAR)

ABSTRAK

Tesis ini mempersembahkan rekabentuk dan fabrikasi penapis aktif jalur-lebar laluan-rendah CMOS untuk penerima integrasi penuh Radar Bukaan Sintetik (SAR). Penapis tersebut adalah sebahagian daripada penerima bistatik yang mempunyai litar yang kurang kompleks berbanding dengan monostatik SAR. Bistatik SAR memisahkan litar penghantar dengan litar penerima. Sel penerima terdiri daripada banyak bukaan, maka adalah menguntungkan sekiranya penerima SAR direkabentuk secara bersepadu menggunakan teknologi 'ultra deep submicron' yang boleh digunakan di tempat yang terhad. Dalam penerima SAR ini, isyarat operasi jalur telah ditapis di panel radiator. Namun, adalah penting untuk menapis sekali lagi isyarat tersebut di jalur dasar untuk memastikan laluan isyarat bersih daripada isyarat gangguan dan menghadkan hingar jalur. Penapis laluan-rendah ini perlu direkabentuk di atas cip dan mempunyai frekuensi potong di 50 MHz sehingga 160 MHz. Ini adalah mencabar di dalam teknologi "ultra deep submicron CMOS" di mana voltan bekalan di dalam lingkungan 1.2 V digunakan. Penapis tersebut juga perlu mendapat riak yang rendah ±0.75 dB sehingga ±1 dB di laluan lulus dan gandaan dalaman untuk memenuhi spesifikasi jalur asas. Penapis tersebut perlu juga mempunyai penurunan sambutan frekuensi yang paling curam kerana ia terletak sebelum penukar analog kepada digital (ADC), untuk mengelakkan pertindihan hingar dan isyarat luar jalur yang tidak diperlukan di dalam sampel isyarat. Objektif utama tesis ini adalah untuk merekabentuk dan mengfabrikasi penapis laluan-rendah bersepadu di jalur asas dengan frekuensi potong 50 MHz sehingga 160 MHz sebagai sebahagian daripada penerima bersepadu SAR. Penapis tersebut perlu mempunyai riak laluan lulus sebanyak ±0.75 dB sehingga ±1 dB sebagai litar tunggal, dan memenuhi kejatuhan -20 dB di 220 MHz. Penapis tersebut perlu menyediakan gandaan sebanyak 20% hingga 30% daripada gandaan jalur asas keseluruhan. Kemudian, keupayaan fungi penapis itu dibuktikan melalui eksperimen sebagai satu litar tunggal. Seterusnya, penapis tersebut bersama-sama dengan litar lain dibuktikan melalui eksperimen sebagai satu penerima SAR berintegrasi penuh. Rekabentuk telah dijalankan dalam dua fasa, dengan menggunakan Cadence dan Eldo sebagai alat rekabentuk dan alat simulasi. Penapis jalur-rendah susunan 5 g_m-C telah dibangunkan menggunakan teknologi 130 nm CMOS. Penapis tersebut dibangunkan menggunakan prototaip kehilangan. Topologi pengkamiran-pseudo telah digunakan bersesuaian dengan voltan punca 1.2 V yang rendah. Litar rintangan negatif telah untuk memastikan gandaan pengalir-trans tetap pada 26 dB. Suis matrik-kapasitor 5 bit telah dibangunkan untuk mengawal lebar jalur penapis. Penukar digital-ke-analog kawalan-arus 9-bit (IDAC) jug dibangunkan untuk menyahkan pergerakan DC. Keputusan eksperimen penapis selaku litar tunggal dan juga bersama-sama dengan blok penerima yang lain telah membuktikan penapis-penapis tersebut yang mempunyai frekuensi potong 160 MHz dan 50 MHz, masing-masing mencapai kepadatan hingar rujukan masukan sebanyak 4.9 nV/√Hz dan 7.7 nV/√Hz . Kedua-dua penapis mempunyai gandaan dalaman sebanyak 8 dB dan riak di jalur lulus sebanyak ±1 dB sebagai litar tunggal. Walaupun spesifikasi fasa linear tidak dapat dipenuhi, sambutan fasa boleh dilinearkan menggunakan penapis laluan-semua yang telah dicadangkan untuk dibangunkan di masa hadapan.

Design and Fabrication of a Wideband CMOS Continuous-Time Integrated Baseband Active Filter for a Synthetic Aperture Radar Receiver

ABSTRACT

This thesis presents the design and fabrication of CMOS continuous-time low-pass integrated baseband filters intended for a fully integrated multiband Synthetic Aperture Radar (SAR) receiver. The low-pass filters are part of a bistatic SAR receiver which exhibits less complexity of circuit implementation compared to its monostatic type of antenna counterpart. The bistatic SAR separates the transmit circuits from the receive circuits which is divided into sub-apertures. Since a large number of channels are required, it is very desirable to design integrated receivers in modern ultra deep submicron technologies which can cope with a limited space. In this SAR receiver, the band of operation is bandpass filtered in the radiator panel. However, it is important to have filtering again in the baseband to keep the signal path clean from interfering signals and to limit the noise bandwidth. This continuous-time baseband filter needs to be on-chip and the cutoff frequency must be at 50 MHz up until 160 MHz. This is very challenging in ultra deep submicron Complementary Metal Oxide Semiconductor (CMOS) technologies in which a low supply voltage around 1.2 V is demanded. In addition, the integrated low-pass filter is targeted to have low ±0.75 dB to ±1 dB passband ripple and embedded gain to cater the requirement of the baseband. At the same time, the filter needs to be the most selective since it is located before the Analog to Digital Converter (ADC), to avoid the aliasing noise and unwanted out-of-band signals in the signal sampling. The main objective of this work is to design and fabricate a low-pass continuous-time integrated baseband filter circuit with cutoff frequency of 50 MHz up to 160 MHz as part of a fully integrated SAR receiver. The filter should exhibit passband ripple from ±0.5 dB to ±1 dB as a standalone circuit and -20 dB attenuation at 220 MHz. The filter is targeted to provide gain of 20% to 30% from the whole baseband gain. The filter's functionality is to be proved by means of experimental results, at first as a standalone structure. Then, the measurement of the filter together with the other block as a complete SAR receiver is to be executed to prove the functionality of the filter in the receiver. The design activity has been done in two phases using Cadence and Eldo as the design and simulation tools respectively. 5^{th}-order Chebyshev g_m-C low-pass filters were implemented in 130 nm CMOS technology and were synthesized using a lossy prototype. Since a low supply voltage of 1.2 V was targeted, a pseudo-differential topology transconductor has been designed. A negative resistance circuit was utilized as a means of Q-control circuit, which ensured the DC gain of the transconductor fixed to the targeted 26 dB. A 5-bit switched capacitor matrices has been developed to tune the filters' bandwidth. In addition, a 9-bit current-steering digital-to-analog converter (IDAC) was designed in the baseband to compensate the DC-offset. Measurement results of the filters as a standalone structure and also together with the other receiver blocks have proved the functionality of the circuits. The performances of the filters meet the specifications, in which with cutoff frequencies of 160 MHz and 50 MHz, 4.9 nV/√Hz and 7.7 nV/√Hz input referred noise density is achieved by the former and later, respectively. Both the filters have embedded gain of 8 dB and have a gain flatness of ±1 dB as a standalone circuit. Although the phase linearity specified was not met, the phase response may be linearized with an all-pass filter, which is recommended for future work.

CHAPTER 1

INTRODUCTION

1.1 Introduction

This chapter presents an introduction to the research work in this thesis. The background and the problem statement are presented and the objectives of this research work are given in the next section. Then, the organization of this thesis is explained.

1.2 Background

In (Berens, 2006; Cherniakov, 2007; Torre, 2013), a radar or radio detection and ranging is defined as an electromagnetic sensor used for the detection and location of reflecting objects. In most cases of the radar system in which an antenna is the physical object, it is called a real aperture radar (RAR) (Sullivan, 2004). In the case where the antenna moves to cover a synthetic aperture, it produces a technique called a synthetic aperture radar (SAR). The principle of SAR was formed in 1951 in the US at the Goodyear Company by Carl Wiley (Sullivan, 2004; Richards, 2005, Cumming, Wong, 2004, Lancomm, 2011).

SAR is produced based on a desire to achieve finer resolution in an airborne or a spaceborn ground-mapping radar. Although the image quality obtained from SAR is not as good as the image resolution captured by photographic systems, the attribute of SAR that is the insensitive to weather conditions is an advantage (Berens, 2006). SAR can

image a scene through clouds and rough (inclement) weather due to the propagation of the RF waves. In addition, SAR can also image at any time regardless of day and night because it provides its own light via transmitted pulse and does not rely on the sun for illumination.

Classical SAR systems use an active antenna comprised a lot of active transmit and receive cells (Cherniakov, 2008). Each of the cells transmitted signals and received signals from individual antenna elements (or a group of elements). In order to create and steer the transmitted and received beam, the amplitude and phase of individual signals are adjusted under the control of a digital bus, integrated within the antenna structure (Sullivan, 2004). This architecture is called a monostatic SAR. This system enables beam steering and the selection of parts of the swath (target area) for high resolution measurements. It also allows lower resolution measurements of a larger area of the swath.

However, in circuit implementation point of view, such an active antenna implementation is highly complex (Muff, 2015). It requires the integration of microwave transmit power circuits, low noise microwave receive circuits, digital control circuits and bias supplies. In the case of a spaceborne SAR, its next generation will utilize digital beam forming techniques to improve performance and flexibility (Cherniakov, 2008). For this application, early downconversion and digitization at subarray (sub-apertures) level will be needed. Thus, the current system architecture cannot provide high resolution and wide coverage simultaneously, adequate for the expanding of the earth observation as well as the user community. It is also complex, poses a critical technology challenges and thus places a high financial expense on the market area.

A novel instrument overcomes the classical SAR limitations by using separated transmit and receive apertures. It is called a bistatic SAR (Cherniakov, 2008). The transmit aperture is smaller compared to that of conventional SAR. It determines the

swath width and the azimuth resolution. The larger receive only aperture which is divided into sub-apertures compensates the lower gain and the poor ambiguity performance of the transmit aperture. In the receive cell, a time frequency variant digital beam forming is applied to focus the receive gain on the transmitted pulse as it runs over the earth's surface (Ludwig et al 2003).

Each receive panel of a SAR receiver could consist typically around 30 elements or even more, depending on the radar configuration. A typical antenna could have more than thousand elements (Cherniakov, 2008). The number of receiver and digital channels is the same if digital beam forming is fully applied, on the element level.

Since a large number of channels are required, it is very desirable to design integrated receivers in modern ultra deep submicron technologies which can cope with a limited space. Accommodation, mass, noise and especially electrical power dissipation are all critical parameters. In this case, fully integrated receivers are very attractive to fit in the limited space and also to simplify manufacturing processes by reducing part count. The constraint is that the large number of channels requires low power implementation in order to keep the overall power consumption within the limits while high bandwidth is needed.

Radar system design has a strict limitation. The legal issues are decided at international conference which fix the bandwidth as well as the frequencies authorized (Massonet, Souyris, 2008). In the case of Synthetic Aperture Radar, the bandwidth and the authorized frequencies are shown in Table 1.1. The targeted band for this SAR receiver are C band, L band and X band. Hence, the RF bandwidth in the radar receiver has to be between 100 MHz up until 320 MHz.

Table 1.1: Authorized bandwidth and frequency for Synthetic Aperture Radar.

Band	Ku band	X band	C band	S band	L band
Center frequency	13.5 GHz	9.65 GHz	5.41 GHz	3.2 GHz	1.26 GHz
RF Bandwidth	500 MHz	300-320 MHz	320 MHz	200 MHz	85-100 MHz

Generally in a radar receiver, the band of operation is bandpass filtered in the radiator panel. The bandpass filter is assumed to suppress any unwanted out-of-band interfering signals to an adequate low level before the integrated receiver. However, a very selective RF bandpass filtering would be required before the sampling of the signal in receiver architectures that performs A/D conversion close to the receiver input. This is due to the increased effects of the aliasing of noise and unwanted out-of band interferers in the signal sampling operation. Furthermore, it is die area consuming to implement selective integrated RF filter. With regards to off-chip implementation, the more selective the RF filter, the more discrete components have to be used, thus increasing the price.

In this SAR receiver, the RF bandpass filter is implemented off-chip before the integrated receiver. When employing radar receiver architectures such as superheterodyne and direct conversion topology, some filtering is needed in addition to the bandpass filter of the radiator panel to have clean signal path.

1.3 Problem Statement

Although the RF bandpass filter has been implemented off-chip in this SAR receiver, it is important to have filtering again in the baseband to keep the signal path clean from interfering signals and to limit the noise bandwidth. This continuous-time baseband filter needs to be on-chip to have an integrated SAR receiver. The specification of the cutoff frequency for the integrated baseband low-pass filter in this SAR receiver is