DESIGN AND IMPLEMENTATION OF EMBEDDED TRUE PARALLELISM JAMMER SYSTEM USING FPGA-SoC FOR LOW DESIGN COMPLEXITY

By

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LIST OF ABBREVIATIONS

AADL	Architecture Analysis and Design Language
ASIC	Application-Specific Integrated Circuit
BCD	Binary Coded Decimal
CAD	Computer Aided Design
CB	Connection Block
CFAR	Constant-False-Alarm-Rate
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CREW	Current Read Exclusive Write
DDL	Double Dabble Algorithm
DGAS	Distributed Global Address Space
DLL	Delay-Locked Loop
DLP	Data-Level Parallelism
DSK	Digital Signal Processing Kit
DSM	Distributed Shared Memory
DSP	Digital Signal Processing
FIFO	First-In-First-Out

FMCW	Frequency Modulated-Continuous Waveform
FPGA	Field Programmable Gate Array
FSK	Frequency-Shift Keying
GPIO	General Purpose Input / Output
GSB	General Switch Box
HDL	Hardware Description Language
IEEE	Institute Of Electrical And Electronic Engineering
ILP	Instruction-Level Parallelism
IP	Intellectual Property
LCD	Liquid Crystal Display
LF	Loop Filter
LIFO	Last-In-First-Out
LUT	Look-Up Table
MIMD	Multiple Instruction Multiple Data
MISD	Multiple Instruction Single Data
MMP	Massively Multi-processing
MPSoC	Multiprocessor System-on-Chip
NCD	Native Circuit Description

NUMA	Non-Uniform Memory Access
PD	Phase Detector
PE	Processing Element
PLD	Programmable Logic Devices
PLL	Phase-Locked Loop
PRAM	Parallel Random Access Memory
PWM	Pulse Width Modulation
ROM	Read-Only Memory
RTL	Register Transfer Level
SAR	Synthetic-Aperture Radar
SARH	Semi-Active Radar Homing
SIMD	Single Instruction Multiple Data
SISD	Single Instruction Single Data
SMP	Symmetric Multi-processing
SoC	System on Chip
SRAM	Static Random-Access Memory
TLP	Thread-Level Parallelism
UMA	Uniform Memory Access

UML	Unified Modeling Language
VCO	Voltage-Controlled Oscillator
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

REKABENTUK DAN IMPLIMENTASI SISTEM KESELARIAN ASLI BERASAKAN JAMMER FPGA-SoC BAGI REKABENTUK KOMPLEKS RENDAH

ABSTRAK

Keadaan yang mendorong sistem untuk melengkapkan pemprosesan beberapa fungsi dalam jumlah masa yang tertentu dipanggil sistem masa nyata. Platform pemprosesan sistem peluru berpandu menghadapi dua isu utama: kos yang tinggi dan struktur yang kompleks. Kerumitan sistem struktur ini adalah hasil daripada pelbagai sebab-sebab yang termasuk mekanisme yang digunakan dalam sistem tersebut untuk melaksanakan fungsi sistem. Mekanisme ini boleh mengakibatkan kelewatan dalam pemprosesan data disebabkan oleh pelbagai faktor, seperti penyegerakan isyarat modul sistem, seni bina unit pemprosesan, dan kuasa pengiraan unit tersebut. Dalam usaha untuk mengurangkan sistem kompleks dan kos sistem, ia telah dicadangkan bahawa mekanisme keselarian yang benar hendaklah digunakan ke atas sistem, bersama-sama dengan struktur serentak. Platform FPGA (DE1-SoC) telah digunakan sebagai persekitaran bagi pelaksanaan sistem ini. Ini mengakibatkan sistem yang dicadangkan berkualiti mempunyai kos yang rendah. Tambahan pula, kerumitan system telah berkurang kerana sistem tersebut menggunakan struktur serentak. Antara modul yang berkait rapat dengan sistem yang dicadangkan termasuk unit pengurus input isyarat yang menyegerak empat isyarat input, modul emulator isyarat yang menghasilkan ujian isyarat untuk memeriksa fungsi sistem apabila tiada isyarat yang berfungsi, data output modul penampan akan menyimpan isyarat yang telah dirakam dan diproses, dan unit generasi alamat yang menjana alamat supaya data yang diproses boleh disimpan dalam output penimbal data. Dalam sistem ini, isyarat yang diliputi adalah dalam empat arah. Fasa Dikunci Loop telah dimanipulasi untuk membolehkan sistem merangkumi spektrum isyarat yang luas. Tambahan pula, sistem unjuran frekuensi jamming laser mampu memproses pelbagai frekuensi pada satu masa. Pelaksanaan itu mampu mendapatkan tahap yang boleh menerima kendalian dan juga menurunkan kerumitan. Tambahan pula, kaedah struktur reka bentuk tersebut juga membolehkan seni bina pengkomputeran serentak menjadi berskala, manakala penumbuhan keseluruhan sistem tersebut menaik.

DESIGN AND IMPLEMENTATION OF EMBEDDED TRUE PARALLELISM JAMMER SYSTEM USING FPGA-SOC FOR LOW DESIGN COMPLEXITY

ABSTRACT

The condition that drives a system to complete the processing of a number of functions within a given amount of time is called the real-time system. A projective missile system's processing platforms face two major issues: high cost and structureal complexity. The system structure's complexity is a result of various reasons that include the mechanism utilised in the system in order to perform the system functionality. This mechanism can lead to delays in data processing because various factors, such as the synchronisation of the system modules' signals, the processing unit's architecture, and the unit's computational power. In order to lessen system complexity and system cost, true parallelism mechanism is applied over the embedded system, along with a concurrent structure. The FPGA platform (DE1-SoC) was used as the implementation environment for this system. This led to an enriched implemented system that had low costs. Furthermore, the system complexity is lessened since the system uses a concurrent structure. Some of the modules that are closely related to the system are implemented to support main processing module. In this system, the signals covered were in four directions. The total logic element was (5032) and total registers was (5180). The Phase Locked Loop up to (1.6) GHz was manipulated in order to allow the system cover a wide spectrum of signals with high accuracy of computing process. Furthermore, the laser projective frequency jamming system is capable of processing multiple frequencies at a time. The implementation was able to obtain acceptable levels of throughput and it also lowered the complexity. Furthermore, the structural design methodology also makes it possible for the embedded concurrent computing architecture to be scalable while the entire system grows.

CHAPTER ONE

INTRODUCTION

Embedded systems are also considered as reactive systems, which means that they continuously react to the environment and mostly have the real-time respond characteristic. Recent trends in the development of embedded systems have moved away from being restricted to a specific function. Instead, alternative trends have more flexibility that will allow one to modify, add, and even delete some of the embedded system's sub-functionality units. In fact, changes are already taking place in the field of embedded systems even while this research is being conducted. As such, the goal is to make these embedded systems as fast and small as possible. One of the areas of application that the embedded systems encompass is the mission critical area which includes avionic, frequency jammer, and spacecraft(Chawan, Patle, Cholake, & Pardeshi, 2012).

The need for big companies to meet customer requirements has made them consider certain key features during the design and implementation of their systems. The most important features that need to be considered are the re-configurability, power consumption, cost, and time to market. The FPGA possesses all these features and even some more characteristics like reliability and the capacity to process data in a parallel manner (Dorta, Jiménez, Martín, Bidarte, & Astarloa, 2009). Although the focus of this thesis was on enhancing system performance and improving the throughput through the application of true parallelism, the relative complexity was also considered. Thus, the mapping tasks of the high-level designing stages could be transformed into lower-level sub-tasks to lessen the complexity of the functionality units. The design that was proposed aimed to simplify the complicated tasks in order to come up with a system that had as much real-time responses as possible.

Currently, FPGA-based systems have the capacity to merge the advantages of both ASIC and DSPs. This leads to systems that are capable of rapid development cycles, high reliability, easy upgrading, high flexibility, and moderate costs (Griessl et al., 2014). This project utilised the FPGA in the design and implementation of its functional units in order to take advantage of these features. Harnessing the FPGA resources within this project led to better performance and higher throughput since true parallelism was utilised in its implementation.

This project aims to achieve the ability to process multiple signals at a time instead of just processing a single signal. Other aspects like the power consumption, cost, reconfigurability, and portability were improved with the use of the FPGA platform as the proposed system's implementation environment. It has been proposed that less than four aircraft fighters must utilise their laser missiles during the attack of a single target because a laser beam interference situation might take place if more than four laser missiles are launched to destroy a single target. As such, a laser missile frequency jamming system that can process four frequency signals at a time and control four defused plates was proposed. This will allow the system to direct the frequencies that have been captured towards attacking aircraft fighters.

Additionally, supported modules are designed and implemented such as the input signal unit manager that can synchronise four input signals, the signal emulator module that produce test signals to check the functionality of the system when there are no available signals, the output data buffer module that is responsible for storing the captured and processed signals for later studies, and the address generation unit which generates addresses for the processed data so that they can be stored within the output data buffer.

Since the code is divided into discrete portions, every part is considered an independent process concurrently executed using various modules. In this case, true

parallelism was used. This means that the calculation of an interpolated value for every grid cell in the lattice is independently treated from all the other cells' computation of values. First, the jammer analyses the spectrum of the signal that was received from the frequency hopped transmitter. Then, the signal's features are extracted. The features are then taken to the frequency synthesiser so that the synthesiser produce the same hopping frequency. Lastly, the narrow-band interference signals are sent to the display units on board like the Seven Segment and LCD.

1.1 Problem Statement

Rapid improvements in systems development have allowed for the development of systems that are more specifically related to human lives. As a consequence, it is now vital to give such systems the capacity to process real-time data and take accurate decisions in order to solve specific problems. The frequency jamming system considered a part of this category, where such a system's computational platform has to be efficient, accurate, and robust. In addition, systems with such functionalities, like the jamming system, should be scalable and portable.

Despite its long clinical success, processing platforms of the frequency jamming system have a number of problems in use which is represented in their complexity and the time required to process signals. Such expositions are unsatisfactory because the delay of processing is examined as a nature result for the system design and the delay occurring in the processing modules. because these main factors, the platforms used to implement the frequency jamming functionality are not capable of providing the requirements for effective and fast processing systems for multiple missiles attack from different directions. The delay time required for processing data, the complexity of the system and the limitation in the frequency range are the core factors of this complication.

Additionally, design and implementation of embedded true parallelism jammer system using FPGA-SoC for low design complexity, is required to overcome delay of processing for multiple missiles threat.

1.2 Project Objectives

The aim of this project is to design and implement a frequency jamming which exploit the principle of the true parallelism and obtain the full advantage of the FPGA to guide the missiles to a specific target, the objectives of this research are:

1. Decreased system overall complexity level jamming system, improved operating frequency, consumed chip resources, and improved throughput.
2. Speed up the processing time, increase the processing cores utilities, and reduce the delay occurring in the processing modules.

1.3 Project Scopes

This project concentrated on qualities that need to be enhanced for increasing the performance as well as throughput of the frequency jamming systems by employing the characteristics embedded within the FPGA. It also gives a brief explanation of the implemented designed system on the board of FPGA. Those qualities that have been improved are integrated in the processing of multiple data each time by applying the true parallelism principle. The attained results in this research has been presented and scrutinised not just for the final system response but also for every stage involved in the system modules so that other researchers and readers can easily understand the same.

1.4 Project Contribution

The following presents the research contribution of this system:

I- For the embedded systems and in any design, a key factor would be the reconfigurability feature. Based on this, the design and implementation of the system is done keeping in mind a reconfigurable embedded frequency jamming system.

II- The second contribution of the system would be the capacity to quickly handle multi-targets all at the same time by applying the true parallelism principle as well as the light temporal approach.

1.5 Project Organization

This thesis is organized with five chapters including

Chapter 1 briefly introduces research approach on FPGA and some research background. Motivations of research and problem statement are also defined. Goal, objectives and scopes of research are stated clearly. Finally, research contributions are discussed.

Chapter 2 is introduces the true parallelism. This chapter presented the related work done in the field of concurrent computing architectures and also presents the benefit of using the true parallelism computing systems as well as introducing brief information about the aspects related to the FPGA.

Chapter 3 describes about the construction of the proposed frequency jamming and the way to achieve this goal. This chapter also presented a highlighted overview about the system design as well as its modules and the functionality of each module.

Chapter 4 presents the obtained result, discussion and detailed explanation of verification phase and implementation phase.

Chapter 5 presents the conclusions derived out of the entire implementation of the system. The future work is also discussed in this chapter.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

A simple overview will result in defining the system on programmable chip (SoPC) as an integrated circuit that has the capacity to incorporate multiple components of computer or a system on a single chip. These days, SoC has caught major interest of developers in the embedded systems domain as it allows them to integrate numerous processor cores alongside other embedded components such as interconnect infrastructure, memories and application-specific circuits, which all result in uniting the entire system on just a single chip. In fact, the embedded system can be optimised efficiently to execute a specific function or a set of related functions. Therefore, the embedded system is deemed as the key-field in employing the SoC as it can even harness large Field Programmable Gate Array (FPGA) that includes both logic elements and memory as well as the intellectual property (IP) processor core to perform a specific application. The true parallelism principle, despite its known association with difficulties in comparison with the non-parallel functional systems, has managed to gain preference due to its overall performance, as duplicate components can be pooled together like processors for enhancing the performance. Some of the major challenges associated with such systems include how these various components can be synchronised better, efficiently leverage the available resources and provide suitable communication techniques.