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High-*k* Gate Dielectric Selection for Germanium based CMOS Devices

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ABSTRACT

This paper presents a systematic approach of material selection for gate oxide material in Germanium (Ge) based CMOS Devices. Various possible high-k gate dielectrics that can be stacked with Ge substrates are Al_2O_3, HfO_2, La_2O_3, Y_2O_3, ZrO_2 and Lu_2O_3. However, each of the dielectric material has its own advantages and limitations therefore it is important to select the best possible candidate. For this purpose, Technique for Order Preference by Similarity to Ideal Solution (TOPSIS) as a Multiple Attribute Decision Making (MADM) technique is used. Based on the ranking derived from TOPSIS, it is found that La_2O_3 is the most suitable material, followed by Y_2O_3 for being used as a gate dielectric in Ge-based CMOS devices. The proposed result is in good agreement with experimental findings thus justifying the validity of the proposed study.

Keywords: Material Selection, Germanium, TOPSIS, High-*k* Gate Dielectrics, CMOS Devices.

1. INTRODUCTION

For the past few decades, the down-scaling trend of CMOS technology is continuing because it reduces cost, decreases power consumption, and increases performance [1]. To further enhance the performance and with recent materials innovation, the semiconductor industry is exploring the alternatives of silicon. A report published in the International Electron Devices Meeting 2016 (IEDM) says that, to push the boundaries of Moore's law, Ge-based devices are a key focus area of research by semiconductor industries [2]. The need of this study lies in the fact that silicon is approaching its limit, with gate oxide thickness going below the 2nm mark which is lower than the threshold of tunneling. A further decrease would lead to an increase in unwanted characteristics such as high leakage current and low drain current. To address this issue, the semiconductor industry is showing interest in high-mobility substrates such as Ge, III-V compound semiconductors, and co-integrated GeSi and III-V structures on large-scale Si-wafers that use wafer bonding techniques for CMOS devices [3-4]. Ge has a high hole mobility while III-V compound semiconductors have a high bulk electron mobility. Various other challenges in implementing III-V channels include ineffective gate stack solution, deposition problem, brittle nature of substrate, and difficulty in making the large substrate sizes [1,3]. Though the wafer bonding technique is the most cost-efficient in terms of the number of processing steps, it is largely constrained by the incompatibility of thermal budgets, wet chemistries, and integration density [4]. Moreover, reliability issues exist for the MOS stacks on InGaAs as it currently appears to be one of the main limitations for CMOS applications [4].

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The use of high-*k* gate dielectric would support, as the same functionality can be derived from a thicker oxide and scaling would further increase the performance of CMOS devices. Recently, Heng Wu. *et al*. [5] realized the Ge CMOS technology and proposed a novel hybrid CMOS structure with inversion-mode Ge pFET and accumulation-mode Ge nFET. High maximum drain current of 714mA/mm and trans-conductance of 590mS/mm and high I_{on}/I_{off} ratio of 1×10^5 were archived at a channel length of 60nm on the nFETs. Moreover, benefiting from the Fermi-Level pining of Ge near the valence band, recently high performance Ge pFETs have been demonstrated [6-7]. So, Ge with proper gate dielectric seems to be the promising alternative of Si CMOS technology.

Some of the high-*k* gate dielectric materials that are being investigated for Ge CMOS devices are Al_2O_3, HfO_2, La_2O_3, Y_2O_3, ZrO_2, and Lu_2O_3 [8-15]. Because of some practical limitations such as reliability, interface quality, and mobility degradation, proper optimization of the device performance is required through a suitable selection of high-*k* gate dielectrics that are compatible with the Ge CMOS technology.

A well-established method of material selection based on the multiple attribute decision making (MADM) approach is used in this paper for selecting high-*k* gate dielectric materials with Ge substrate. The key performance indices include low leakage current and high drain current in device. These indices further depend upon various material indices such as band gap, permittivity, interface trap density, and conduction band offset of high-*k* gate dielectric material/Ge stack.

This paper is organized as follows: section 2 describes the challenges associated with various gate oxides, section 3 explains the desirable criteria for selection, section 4 describes the TOPSIS approach and its implementation in this study, section 5 explains the results and discussion, and finally section 6 gives the conclusion of the proposed study.

2. CHALLENGES WITH GE AND COMMON OXIDES

Ge differs from that of Si mainly because of the fact that in Ge, unlike Si, the Si/SiO_2 stack is not present. Oxides of Ge thermally decompose and desorb at low temperatures and result in defects on the surface. These defects can further act as recombination sites due to the smaller band gap of Ge. The need for a good passivation material and the lack of knowledge on dopant incorporation also hamper the development of Ge devices [16]. Another major concern in the adoption of Ge devices is the lattice mismatch, with respect to Si. [1] Moreover, the thermal expansion coefficients mismatch aggravates the problem. The large dielectric constant of the Ge substrate also makes the devices vulnerable to short channel effects. High-k materials have more number of defects as compared to SiO_2 due to their larger coordination number. These defects have an adverse effect on the mobility in the channel. The role of the passivation layer becomes more important because of the aforementioned reason. A high-quality passivation layer is of critical importance, but then the interfacial layers have low values of the dielectric constant thus increasing the overall effective oxide thickness (EOT). Reducing the EOT below a certain level results in a decrease of the mobility irrespective of high-k gate structures.

Another crucial consideration is the band offsets, namely the conduction band offset (CBO) and the valence band offset (VBO). These must be, at minimum, 1 eV to suppress the Schottky emissions of electrons and holes into the oxide bands [17].

The possibility of using GeO_2 as gate oxide in Ge based CMOS devices is not possible because of the poor electrical properties of GeO_2, and also because the Ge/GeO_2 gate stack is highly undesirable. When GeO_2 and Ge are allowed to react at a processing temperature of 673K, the following reaction takes place:

$$GeO_2 + Ge \rightarrow 2GeO(g) \text{ at } 673K$$

It is clear from the above equation that GeO_2 on the surface eats away Ge and then desorbs as a gas phase. GeO(g) being a reducing agent [18] degrades the electrical properties of the stack. Hence, one should choose other oxides as gate dielectrics in Ge based CMOS devices. High-k gate dielectrics provides the possibility to be used in such cases. For this, the desirable characteristics of a high-*k*/Ge stack are; low EOT and leakage current, large k value and CBO, and small interface trap density. Apart from these, other properties include thermodynamic stability and compatibility with the current process technology.

The next section provides the properties that have been taken into account and the list of materials that are suitable for this purpose.

3. MATERIAL INDICES

The major concern with scaling down the gate dielectric's thickness is leakage current, which in turn affects the driving current of a CMOS device. So these two parameters are taken as performance indices. These performance indices are further dependent on the material properties of the gate dielectrics, which are considered as material indices.

For a MOSFET, in saturation as well as in linear region, the drain current is directly proportional to the capacitance of gate oxide per unit area (C_{ox}). Hence, C_{ox} is an important parameter that can be increased to enhance the drain current of the device. This indicates that a higher value of dielectric constant can boost the drain current of the CMOS device. However, due to the Poole Frenkel effects for a low leakage current, the value of the dielectric constant *k* should be low. Hence, the first material index considered is the dielectric constant.

$$MI_1 = k \tag{1}$$

In order to reduce the possibility of tunneling of electrons, the barrier between the valence band and the conduction band should be large enough. This would mean that the larger the band gap, the better the protection from leakage current. The energy band of a material with high-*k* is given as [19-21]

$$E_g = 20\left(\frac{3}{2+k}\right)^2 \text{ eV} \tag{2}$$

Therefore, the second material index is the band gap E_g.

$$MI_2 = E_g \tag{3}$$

At the interface between the gate oxide and the active Ge layer, discontinuities in the energy bands are formed which lead to the difference in the conduction band as well as in the valence band. These differences between energy levels are known as conduction band offset $\left(\Delta E_c\right)$ and valence band offset $\left(\Delta E_V\right)$. The conduction band offset (CBO) is generally calculated from the electron affinities of the materials and is then used to calculate the valence band offset (VBO). Out of these two, the value of the VBO is generally higher than that of the CBO. The CBO defines the energy barrier height between the gate dielectric and the substrate when the electrons travel from the latter to the gate. Ideally, the value of the CBO should be large enough to prevent leakage current from the device when a high gate source voltage is applied, but since the band

gap depends inversely on the high-*k*, it becomes a challenge to satisfy both aspects. Thus, the third material index is the CBO.

$$MI_3 = \Delta E_c \tag{4}$$

While manufacturing, it is necessary to use extremely clean chemicals, water, gases, and processing environment to prevent impurities from creeping. However, certain defects still persist primarily due to the sudden termination of semiconductor crystal lattice at oxide interface. These causes charge at the boundary of the semiconductor and the oxide. As biasing is done to the device, the interface trap density (D_{it}) increases from accumulation to deep depletion region or vice versa. The interface trap density is given as [22]

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox}-C_{LF}} - \frac{C_{HF}}{C_{ox}-C_{HF}}\right) \tag{5}$$

where C_{LF} and C_{HF} are the capacitance at the onset of strong inversion at low and high frequencies respectively. To improve the device performance, it is imperative that the interface trap density should be low. A lower value results in a lower leakage current. Thus our fourth material index is interface trap density.

$$MI_4 = D_{it} \tag{6}$$

Apart from these material indices, another important criterion is the crystal structure of the gate dielectric. Since this property cannot be quantified, it is used as a supporting measure once the results from the analysis are ranked. Amorphous dielectrics are preferred since they prevent the diffusion of Ge atoms into the high-k film and show minimal intermixing with Ge oxide to stabilize the interface [23]. The material properties of the materials used are provided in Table 1 [1, 8-15]

Table 1 Material properties of the various materials considered

Material	Band gap (eV)	k-value	Interface Trap Density ($eV^{-1}cm^{-2}$)	ΔE_c (eV)	Crystal Structure
Al_2O_3	8.7	9.5	6×10^{11}	2.1	Amorphous
La_2O_3	4.3	27	3×10^{11}	2.6	Amorphous
HfO_2	5.7	35	7×10^{12}	2.0	Crystal, T > 973 K
ZrO_2	5.8	25	8×10^{12}	1.79	Crystal, T > 673-1073 K
Y_2O_3	5.6	16	10^{11}	2.56	Crystal
Lu_2O_3	5.8	11-12	10^{13}	2.1	-

4. TOPSIS APPROACH

Technique for Order of Preference by Similarity to Ideal Solution (TOPSIS) is a multicriteria decision making method, developed by Hwang and Yoon in 1981 [19]. Figure 1 shows the flowchart of steps involved in TOPSIS. TOPSIS works on the principle that the chosen alternative should have the least geometric/Euclidean distance (S*) from the Positive Ideal solution (A*) and the maximum distance(S^{--}) from the Negative Ideal solution (A^{--}). It assigns

weights to each criterion, normalizes scores for each of them, and then calculates the geometric distance between each alternative and the best and worst solution. An important assumption that the TOPSIS approach follows is that the criteria are monotonic in nature and that they are independent.

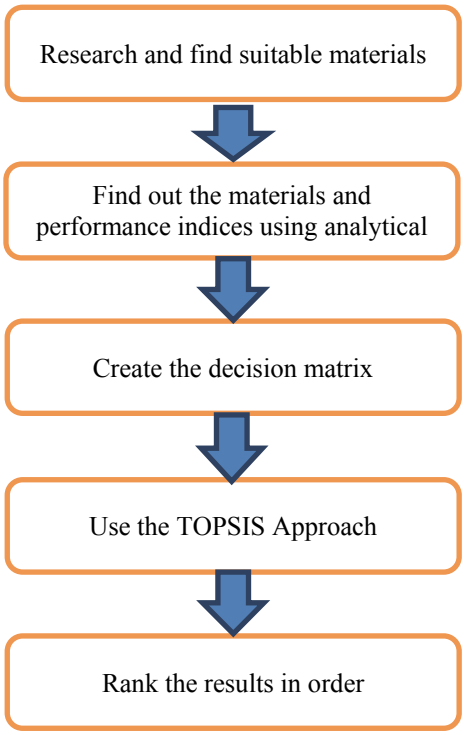

Figure 1. Material selection methodology.

The TOPSIS method is as follows:

Step 1

Create an evaluation matrix consisting of m alternatives and n criteria: $(x_{ij})_{m\,x\,n}$.

Step 2

Normalized the matrix:

$$n_{ij} = \frac{x_{ij}}{\sqrt{\sum_{i=1}^{m} x_{ij}^2}}$$

In the above equation, i represents the set of alternative = 1,2,...,m and j represents the set of criteria = 1,2,...,n.

Step 3

Calculate the weighted normalized decision matrix $(v_{ij})_{m\,x\,n.}$ Here weights are assigned to the different criteria by the virtue of their importance, keeping in mind that the value assigned must be positive and less than 1 and the summation of all weights is equal 1.

$$\sum_{j=1}^{n} w_j = 1$$

$$v_{ij} = n_{ij} * w_j$$

Step 4

Determining the worst solution and the best solution. The maximum value is selected from benefit criteria and the minimum value from cost criteria for the positive ideal solution, and vice versa for the negative ideal solution.

$A^* = \{(\max v_{ij} \mid j \in J_1), (\min v_{ij} \mid j \in J_2)\} = \{v_1^*, v_2^*, \dots, v_n^*\}$
$A^- = \{(\min v_{ij} \mid j \in J_1), (\max v_{ij} \mid j \in J_2)\} = \{v_1^-, v_2^-, \dots, v_n^-\}$

where $J_1 = \{j = 1,2, \dots, n\}$ and *j* is associated with the beneficial criteria and
$J_2 = \{j = 1,2, \dots, n\}$ and *j* is associated with the cost criteria.

Step 5

Calculate the separation between the various alternatives and the best and worst case solution using a simple Euclidean distance equation.

$S_i^* = \sqrt{\sum_{j=1}^{n}(v_{ij} - v_j^*)^2}$, from the ideal solution for *i* = 1,2, …,*m*.

$S_i^- = \sqrt{\sum_{j=1}^{n}(v_{ij} - v_j^-)^2}$, from the worst possible solution for *i* = 1,2, …,*m*.

Step 6

Measure the relative closeness to the ideal solution.

$$C_i = \frac{S_i^-}{(S_i^+ + S_i^-)}$$

where $0 < C_i < 1$, i = 1,2, …,*m*

Step 7

Rank the alternates depending on the value of C_i, where a larger value will imply a better alternate (i.e. the closer the value to 1, the better is the solution). The closer the value to 0, the closer is the solution to the negative ideal solution.

To execute the TOPSIS approach steps, MATLAB code was generated to get the final ranking of the materials.

5. RESULTS AND DISCUSSIONS

For the TOPSIS approach, a well justified weighted matrix is needed with proper weights assigned to the various indices. For high-*k* dielectrics, the highest weight is assigned to the dielectric constant *k*, followed by the interface trap density that has a negative impact on the performance of the device as lower value results in a lower leakage current. The conduction band offset comes next followed by the band gap. This is due to the fact that the same performance as that with Si/SiO_2 can be achieved with a high-*k* dielectric with a much larger thickness than that of SiO_2, and the band gap and the conduction band offset become comparatively less important as the physical width is increased, offering a much higher resistance to the tunneling carriers. Therefore, the weights assigned are: k = 0.4, D_{it} = 0.3, CBO = 0.2 and E_g = 0.1

Hence, the weighted matrix W is given as

$$W = [0.1 \quad 0.4 \quad 0.3 \quad 0.2]$$

Using the parameter values mentioned in Table 1, the normalized decision matrix obtained is:

$$N = \begin{bmatrix} .5796 & .1715 & .0411 & .3877 \\ .2865 & .4874 & .0205 & .4800 \\ .3797 & .6318 & .4791 & .3692 \\ .3864 & .4513 & .5476 & .3305 \\ .3731 & .2888 & .0068 & .4726 \\ .3864 & .2166 & .6845 & .3877 \end{bmatrix}$$

The weighted normalized matrix is given as

$$V = \begin{bmatrix} \mathbf{.0580} & .0688 & .0123 & .0775 \\ .0286 & .1957 & .0062 & \mathbf{.0960} \\ .0380 & \mathbf{.2537} & .1437 & .0738 \\ .0386 & .1812 & .1643 & .0661 \\ .0373 & .1160 & \mathbf{.0021} & .0945 \\ .0386 & .0797 & .2053 & .0775 \end{bmatrix}$$

From V, the ideal and negative ideal solutions are calculated. The positive ideal solution is given as A^* = { 0.0580 0.2537 0.0021 0.0960} and the negative ideal solution is given as A^- = { 0.0286 0.0688 0.2053 0.0661}.

Table 2 gives the geometric distance of the alternates from $A^*$and A^- and the value of the relative closeness C_i. The ranks are then specified in the last column. From Table 2, it is observed that La2O3 is the best high-k material to be used as the gate dielectric in the Ge based CMOS devices. Moreover, La2O3 is amorphous which prevents the diffusion of Ge into the high-k film. Rossel [13] also proposed that the La2O3/Ge stack would be much better than the other possible materials. Song [14] had also extensively supported claims for La2O3 in his thesis. The second alternate material is Y2O3, which had been extensively studied by Mitrovic [12].

Table 2 TOPSIS Results with Ranks

Dielectric	$\mathbf{S^-}$	$\mathbf{S^+}$	**C**	**Rank**
Al_2O_3	0.1956	0.1860	0.5152	4
La_2O_3	0.2380	0.0651	0.7852	1
HfO_2	0.1952	0.1448	0.5741	3
ZrO_2	0.1200	0.1812	0.3984	5
Y_2O_3	0.2108	0.1392	0.6022	2
Lu_2O_3	0.0187	0.2689	0.0650	6

6. CONCLUSIONS

This paper presents the material selection for the gate oxide layer in germanium-based CMOS devices using the Technique for Order Preference by Similarity to Ideal Solution (TOPSIS) approach. Various material indices such as dielectric constant, interface trap density, conduction band offset, and band gap have been considered. The effect of these material indices on the performance parameters of the device have been studied. It has been observed that La_2O_3 is the best material, followed by Y_2O_3. This finding is also in agreement with the experimental results that support the use of Y_2O_3 material for the gate oxide layer in CMOS devices in order to get a high-performance device.

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