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An Optimized Low-Noise Low-Power Preamplifier for Cardiac Implants

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ABSTRACT

Among various analog circuits, the preamplifier has a prominent role in the analog front end (AFE) circuit of biomedical implantable microsystems for a reliable acquiring of weak biophysiological signals. The AFE acts as an interface between the acquired analog biosignals and the digital part in these implants. As the industry of the biomedical implantable devices develops, lowering the power consumption as much as possible without sacrificing the performance is essential in improving the service time of the battery, which cannot be replaced frequently. Hence, there is an increasing demand for a low noise, low power bio-acquisition system so as to avoid bulky connectivity and reduce patient mobility and discomfort. This paper thus presents an operational transconductance based preamplifier for the application in cardiac implants. The performance of the proposed design was evaluated based on various parameters such as gain, common mode rejection ratio (CMRR), noise spectral density, and power consumption. Besides, optimization by supply voltage scaling of the proposed design was done with the focus is on lowering the power consumption. The trade-offs between various parameters like gain, speed, and power consumption were observed in the optimized design. The preamplifier, designed using a 180nm CMOS technology, provides a high gain of 50dB at a supply voltage of 1.5V and a low power dissipation of 61.10µW. Based on the performance evaluation, it was observed that the proposed preamplifier is suitable for low power cardiac applications.

Keywords: Cardiac Implants, Preamplifier, Low Power Electronics, Operational Transconductance Amplifier.

1. INTRODUCTION

The term implant represents a medical device that acts as a part of the whole biological system or can be used to provide support to a damaged biological structure [1,2]. Currently biomedical implants are used for various applications including cardiac pacemakers, defibrillators, and cardiovascular stents. The monitoring of biomedical signals provides us information about the vital health of the body and thus the data can be of prime importance to medical practitioners [3]. With the rapid development in microelectronics towards medical therapies and diagnostic aids, there is a need for lowering the power consumption in active implantable devices that are battery powered so that the device lifetime increases. One such example of active implantable device is the Cardiac Pacemaker in terms of its widespread application [4]. A Cardiac Pacemaker is a device that uses electrical pulses to recover the normal heartbeat of a diseased heart. The major building blocks of the pacemaker, as shown in Figure 1, are an analog front end (AFE) circuit, a microcontroller with ultra low power

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consumption, a battery, and an output circuit that stimulates the heart. The AFE comprises of a preamplifier, a low-pass filter, a level shifter, and a synchronizing circuit. The cardiac signal is given to a low noise preamplifier for amplification purposes and is then filtered. This filtered signal is then given to the comparator that produces a pulse which depends upon the threshold voltage level. The output stage of a pacemaker is called a charge pump that uses a pulse generator to stimulate the activity of the heart. Thus, a preamplifier is a critical block that is used for the detection of small level signals especially for biomedical applications [3].

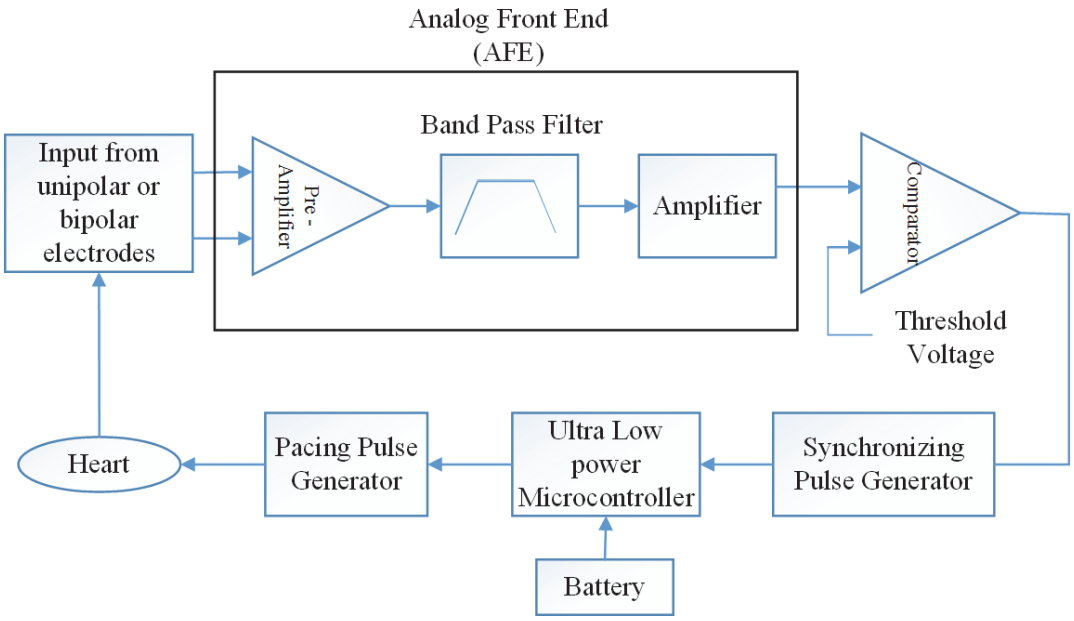


Figure 1. General Block Diagram of an Implantable Cardiac Pacemaker System.

Biosignals like EEG, ECG, EMG, EOG are weak signals with an input amplitude typically ranging from 0.5μV to 5mV [5,6] and are highly susceptible to noise and power line interference at 50Hz to 60Hz. Nowadays there is a demand for a low noise, low power bio acquisition system so as to avoid bulky connectivity and reduce patients' mobility and discomfort [7]. A Preamplifier is one of the important components of the analog front end as it determines the SNR of the entire biomedical signal acquisition system and is required for reliable monitoring of the physiological signal [8]. These weak biosignals need to be amplified before being compatible for processing by the other components of the implant for measurement and testing purposes [9].

2. DESIGN SPECIFICATIONS

Neural implantable devices, EEG, and cochlear implants are the major application areas for the preamplifier design in the survey [10-15] while less explored applications being the cardiac pacemaker, EOG, PCG, and retinal prostheses. Some of the key design parameters of an amplifier are its Gain, stability, power consumption, CMRR, PSRR, Noise, THD, and Dynamic range. Different applications demand different parameters that are critical to that particular application. Some applications like Neural Implantable devices require a low noise, low power analog front end while others like cochlear require a high PSRR, and good SNR. Based on the literature study [16-18], the required design specifications for the preamplifier for Cardiac Implants are formulated and summarized in Table 1. A high gain of >50dB, a high CMRR of around 70dB, and a high PSRR of 60dB are required for this particular application.

Table 1 Design Specifications for Preamplifiers in Cardiac Implants

Parameters	Target Specifications
Gain	> 50dB
Slew Rate	>10V/μs
Load Capacitance	10pF
Min and Max Output voltages	±2V
Unity Gain Bandwidth	7MEG
ICMR	-1.5V to 2.5V
CMRR	> 70dB
PSRR	> 60dB
Technology	180nm

3. PROPOSED LOW POWER PREAMPLIFIER

The folded cascode Operational Transconductance Amplifier (OTA) was chosen for the design of the preamplifier for cardiac applications. An OTA is actually an op-amp without the output buffer and is capable of driving only capacitive loads. One of the important features of the OTA is that its transconductance can be adjusted by a bias current. A folded cascode is actually a compromise between a two stage and a telescopic cascode. The name "folded" comes from the fact that because of the folding of P-channel cascode active loads of a differential pair and then converting the MOSFETs to N channel. A folded cascode overcomes the drawbacks of a telescopic structure, i.e. limited output swings and difficulty in shorting input and output, thus provides a wide swing. A Wide Swing means that an input Common mode range is very close to the supply voltage [19]. The Output voltage swing is limited by supply voltages. In a folded cascode OTA a perfect balance of currents in the differential amplifier stage is not required because of the fact that excess dc currents can flow in or out of the current mirror. The practical version of an OTA and its small signal Model are shown in Figure 2 and Figure 3 respectively. The bias currents I_3, I_4, and I_5 of the topology should be designed such that the DC current in the cascode mirror never goes to zero, e.g. if the input voltage Vin is made large enough such that M1 is turned on and M2 is turned off. Then, all the current I_3 will flow through M1 that results in $I_1 = I_3$ and I_2 will be zero. If the currents I_4 and I_5 are not greater than current I_3, then I_6 will be zero. To avoid this problem, the values of currents I_4 and I_5 were kept between values of currents I_3 and $2I_3$ [20]. The resistances R_A and R_B as seen looking into the source of M6 and M7 and are given as:

$$R_A = \frac{rds_6 + R_2 + \dfrac{1}{gm_{10}}}{1 + gm_6 \cdot rds_6} \approx \frac{1}{gm_6} \tag{1}$$

$$R_B = \frac{rds_7 + R_9}{1 + gm_7 \cdot rds_7} \approx \frac{R_9}{gm_7 \cdot rds_7} \tag{2}$$

Here, $R_9 = gm_9 \cdot rds_9 \cdot rds_{11}$

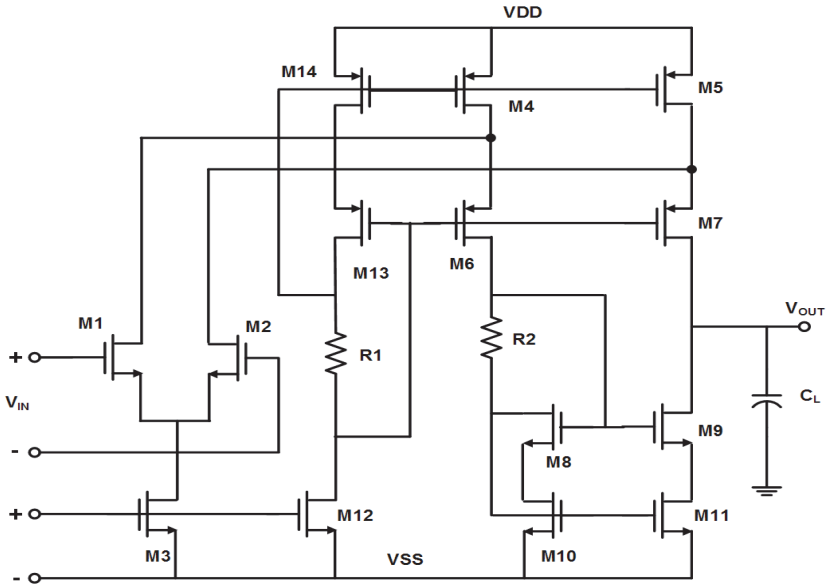


Figure 2. Folded Cascode OTA schematic.

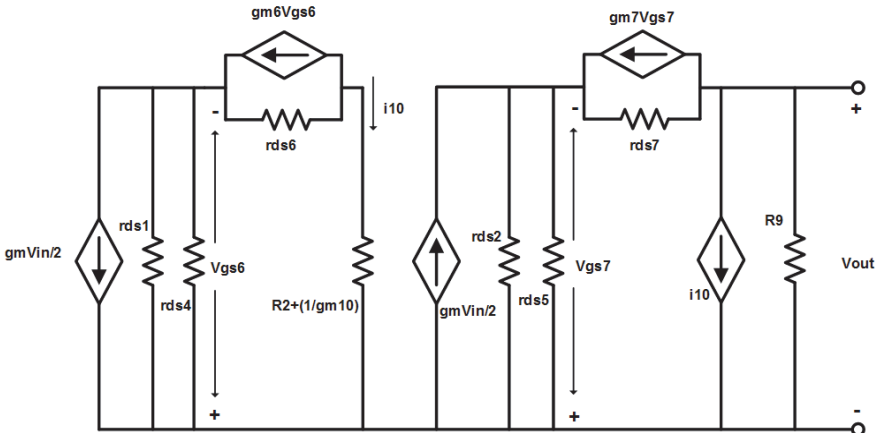


Figure 3. Small signal model of the OTA.

Current i_{10} is given as:

$$i_{10} = \frac{-gm_1\left(rds_1 \parallel rds_4\right)V_{in}}{2\left(R_A + \left(rds_1 \parallel rds_4\right)\right)} = \frac{-gm_1 \cdot V_{in}}{2} \tag{3}$$

Current i_7 can be written as:

$$i_7 = \frac{gm_2 \cdot V_{in}}{2\left(1 + \dfrac{R_9\left(gds_2 + gds_5\right)}{gm_7 \cdot rds_7}\right)} = \frac{gm_2 \cdot V_{in}}{2\left(1+K\right)} \tag{4}$$

Typically K > 1

$$K = \frac{R_9\left(gds_2 + gds_5\right)}{gm_7 \cdot rds_7} \tag{5}$$

The Output Voltage can be expressed as the sum of i_7 and i_{10} flowing through R_{11}

$$\frac{V_{out}}{V_{in}} = \left(\frac{gm_1}{2} + \frac{gm_2}{2(1+K)} \right) = \left(\frac{2+K}{2+2K} \right) gm_1 \cdot R_{11} \tag{6}$$

where R_{11}, the output resistance is given as $R_{11} \approx gm_9 \cdot rds_9 \cdot rds_{11} \,||\, \left(gm_7 \cdot rds_7 \left(rds_2 \,||\, rds_5 \right) \right)$

3. 1 Analytical Modeling

The design of the Proposed Folded Cascode OTA was done using level 49 BSIM3v3 MOSFET and TSMC 0.18μm. T-Spice parameters were used, which are summarized in Table 2. The design consists of determining the specifications, selecting device sizes and biasing conditions, and simulating and characterizing various performance parameters such as the open loop gain, CMRR, slew rate, and output swing.

Table 2 Parameters from Tspice Model File (TSMC 180nm)

Parameter	Value
k_n'	172.1μA/V^2
k_p'	-36.4 μA/V^2
Low Field Mobility μ_n	398.72 (cm^2)/V*s
Low Field Mobility μ_p	84.33 (cm^2)/V*s
V_{thn}	0.37965 V
T_{ox} for NMOS	4.1e-9 m
V_{thp}	-0.4215 V
T_{ox} for PMOS	4.1e-9 m

The main goal is to design a preamplifier based on the above design specifications and to choose proper W/L sizes for the amplifier design. The design steps to compute the transistor sizes are as follows :

i. Smallest device length is chosen such that the channel length modulation parameter λ is kept constant, and also there is good matching for current mirrors. (Here $L=1\mu m$)
ii. From the Slew rate expression, the tail current I_3 is obtained
iii.

$$I_3 = SR \cdot C_L \tag{7}$$

Where SR is the slew rate and C_L is the load capacitance.

iv. Bias currents in the output cascode while avoiding zero currents in the cascode are given as:

$$1.2I_3 \le I_4 = I_5 \le 1.5I_3 \tag{8}$$

v. Design for S_5 and S_7 is obtained from the maximum output Voltage. Let S_4=S_{14}=S_5=S_{13} and S_6=S_7

$$S_5 = \left(\frac{W}{L}\right)_5 = \frac{2I_5}{k_p^{'} \cdot \left(Vds_5\right)^2} \tag{9}$$

$$S_7 = \left(\frac{W}{L}\right)_7 = \frac{2I_7}{k_p^{'} \cdot \left(Vds_7\right)^2} \tag{10}$$

Here $Vds_5(\text{sat}) = Vds_7(\text{sat}) = \dfrac{V_{DD} - V_{out}(\max)}{2}$

vi. Design for $S_{11}$and S_9 is obtained using minimum output voltage. Let S_{10}=S_{11} and S_8=S_9

$$S_{11} = \left(\frac{W}{L}\right)_{11} = \frac{2I_{11}}{k_n^{'} \cdot \left(Vds_{11}\right)^2} \tag{11}$$

$$S_9 = \left(\frac{W}{L}\right)_9 = \frac{2I_9}{k_n^{'} \cdot \left(Vds_9\right)^2} \tag{12}$$

Here $Vds_9(\text{sat}) = Vds_{11}(\text{sat}) = \dfrac{V_{out}(\min) - \left|V_{SS}\right|}{2}$

vii. Calculation of resistance values.

$$R_1 = \frac{Vds_{13}(\text{sat})}{I_{12}}, R_2 = \frac{Vds_8(\text{sat})}{I_6} \tag{13}$$

viii. Design of S_1 and S_2 is obtained from the value of Unity gain bandwidth and load capacitance C_L.

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^{\,2}}{k_n^{'} \cdot I_3} I_3 \tag{14}$$

Where $GB = \dfrac{gm_l}{C_L}$

ix. S_3 design is obtained from the minimum Input common mode voltage

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{2I_3}{k_n^{'}\left[V_{in}(\min) - V_{SS} - V_{t1} - \sqrt{\dfrac{I_3}{k_n^{'} \cdot S_1}}\right]} \tag{15}$$

x. S_4 and S_5 design is obtained from the maximum Input common mode voltage.

$$S_4 = S_5 = \frac{2I_4}{k_p^{'}\left[V_D - V_{in}(\max) + V_{t1}\right]^2} \tag{16}$$

Also S_4 and S_5 values should be large enough to satisfy the maximum Input common mode voltage.

xi. The differential Voltage gain is given as

$$A_v = \left(\frac{2+K}{2+2K}\right) gm_1 \cdot R_{11} \cdot I_3 \tag{17}$$

xii. Power dissipation given as

$$P_{diss} = \left(V_{DD} - V_{SS}\right) \cdot \left(I_3 + I_{12} + I_{10} + I_{11}\right) \cdot I_3 \tag{18}$$

xiii. Positive CMR given as:

$$V_{in}(\max) = V_{DD} - \left[\frac{I_5}{\beta_3}\right] \cdot \left|V_{TO3}\right|_{\max} + V_{T1}(\min) \tag{19}$$

xiv. Negative CMR

xv.

$$V_{in}(\min) = V_{SS} + Vds_5(\text{sat}) + \left[\frac{I_5}{\beta_1}\right]^{0.5} + V_{T1}(\max) \tag{20}$$

14. The second stage resistance is

$$R_1 = R_9 \parallel gm_7 \cdot \frac{1}{gds_7} \cdot \left(\frac{1}{gds_2} \parallel \frac{1}{gds_5}\right) \cdot I_3 \tag{21}$$

Where $R_9 \approx gm_9 \cdot rds_9 \cdot rds_{11} \cdot I_3$

15. The parameters can be evaluated from the following equations

$$gm = I_3 \cdot \sqrt{2 \cdot k_{n,p}{}' \cdot S_{n,p} \cdot I_D} \tag{22}$$

$$gds = \lambda I_D \tag{23}$$

$$rds = \frac{1}{gds} = \frac{1}{\lambda I_D} \tag{24}$$

$$Vds(\text{sat}) = I_3 \cdot \sqrt{\frac{2I_{DS}}{\beta}} \tag{25}$$

From the above mathematical equations, the bias currents and the transistor sizes ($\frac{W}{L}$) for the amplifier were calculated and summarized in Table 3 and 4 respectively.

Table 3 Parameter Values

Parameter	Value
I_3	100μA
I_4=I_5	125μA
C_L	10pF
R_1=R_2	2KΩ

Table 4 Calculated $\frac{W}{L}$ of transistors (Assuming L=1μm)

W/L ratios of transistors	Transistor Widths (μm)
$S_5 = S_4 = S_{14} = S_{13}$=109.80	$W_5 = W_4 = W_{14} = W_{13}$=109.80
$S_6 = S_7$ = 65.93	$W_6 = W_7$=65.93
$S_8 = S_9 = S_{10} = S_{11}$=47.44	$W_8 = W_9 = W_{10} = W_{11}$=47.44
S_1=S_2=11.24	W_1=W_2=11.24
S_3=8.421	W_3=8.421
S_{12}=10.5	W_{12}=10.5

3.2 Circuit Schematic

The proposed preamplifier schematic is shown in figure 4. The topology uses cascode current mirrors as active biasing elements. Current mirrors are more economical than passive resistors in terms of the die area required to provide bias current of a certain value.

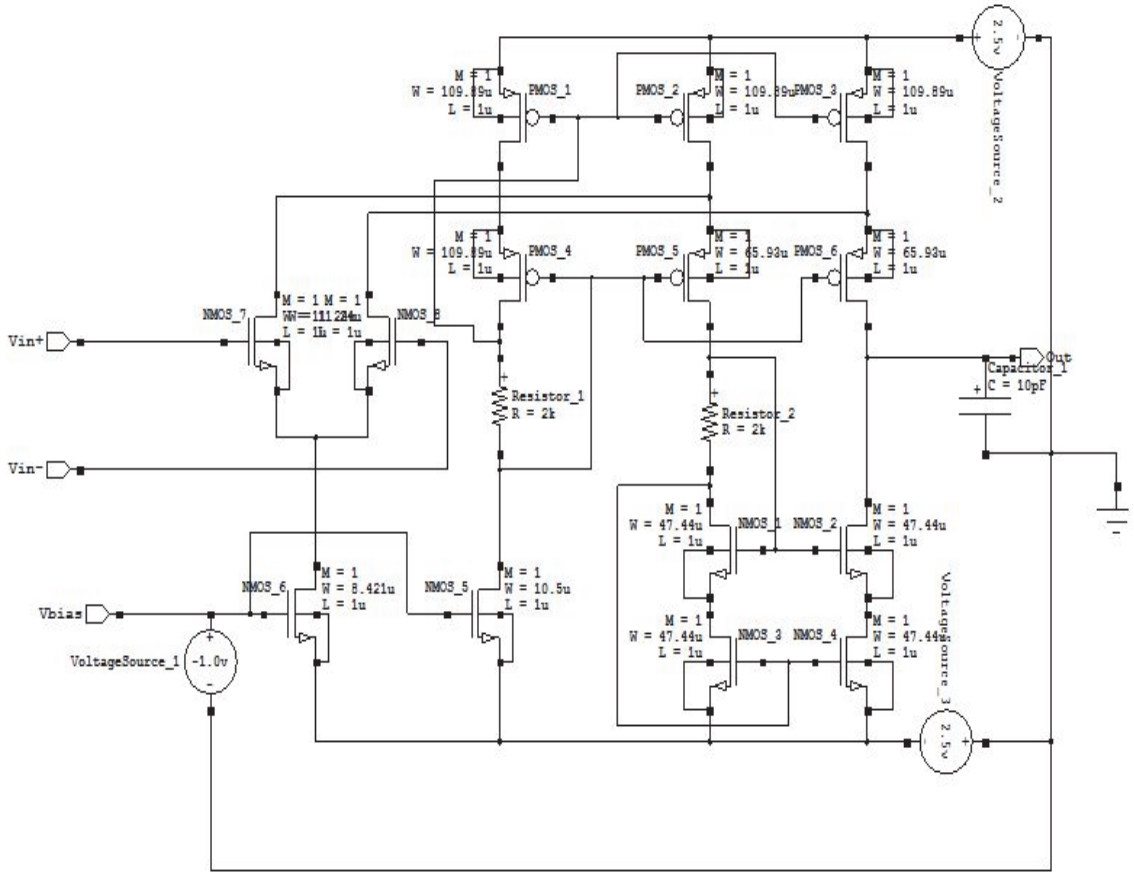


Figure 4. Schematic of the proposed folded cascode OTA based preamplifier.

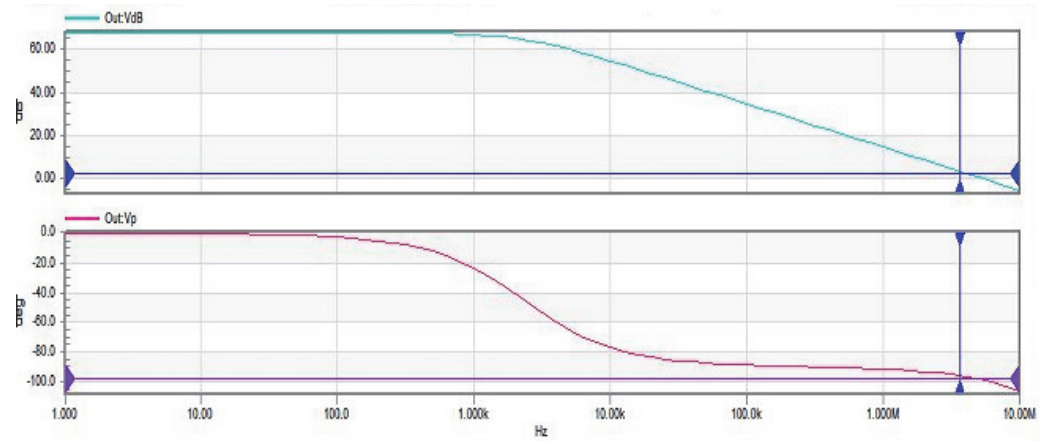
A cascode current mirror provides a wider swing compared to a Wilson current mirror. Because of this current mirror, folded cascode op-amp has a wider output swing. The 3 main

stages of the OTA include the differential input stage, the folded cascode load stage, and the output stage. The Cascode topology increases the gain of the input differential stage. The folded cascode was used to improve the ICMR and also to reduce the required supply voltage. The Current mirror sink used in this folded cascode topology has the following advantages:

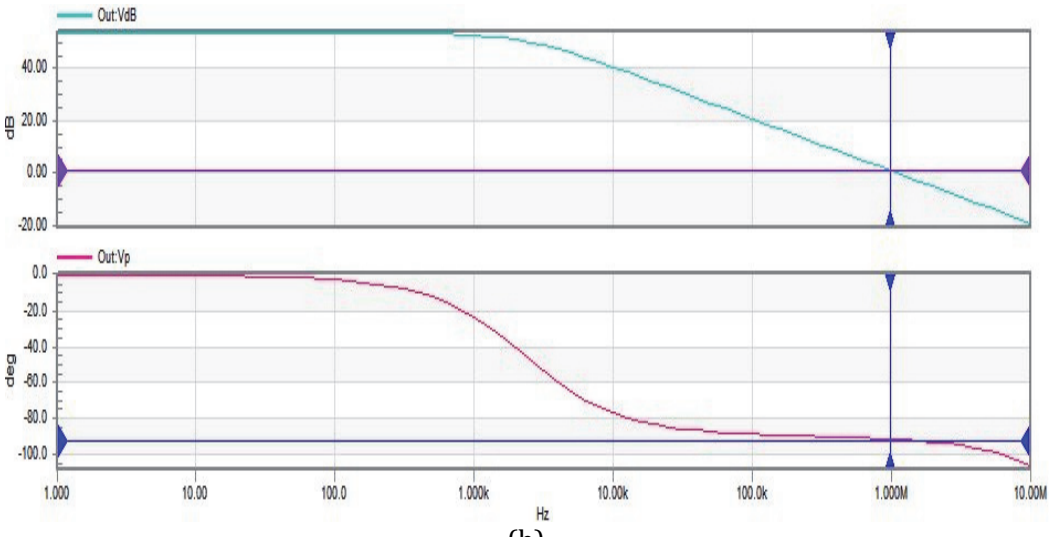
i. High Output resistance
ii. Low Power dissipation
iii. Self-biasing
iv. High swing
v. Small saturation Voltage

4. RESULTS AND DISCUSSIONS

Low Voltage and low power are important attributes for cardiac implants to achieve a longer battery life time. The proposed preamplifier was first designed at a supply of 2.5 V and then optimized by scaling it down to 1.5 V to achieve a lower average power consumption. To find the AC response of the OTA, a 100mV input was given to the differential amplifier along with DC voltages; the ac analysis was done from 1Hz to 10MHz. Figure 5 shows the frequency response of the proposed designs.



(a)



(b)

Figure 5. Frequency response of the proposed preamplifier at (a) 2.5V and (b) 1.5V supply voltage.

To find the Common Mode gain, both Vin+ and Vin- inputs were shorted and then AC and DC voltages were applied. The simulated results in Figure 6 show the common mode gain.

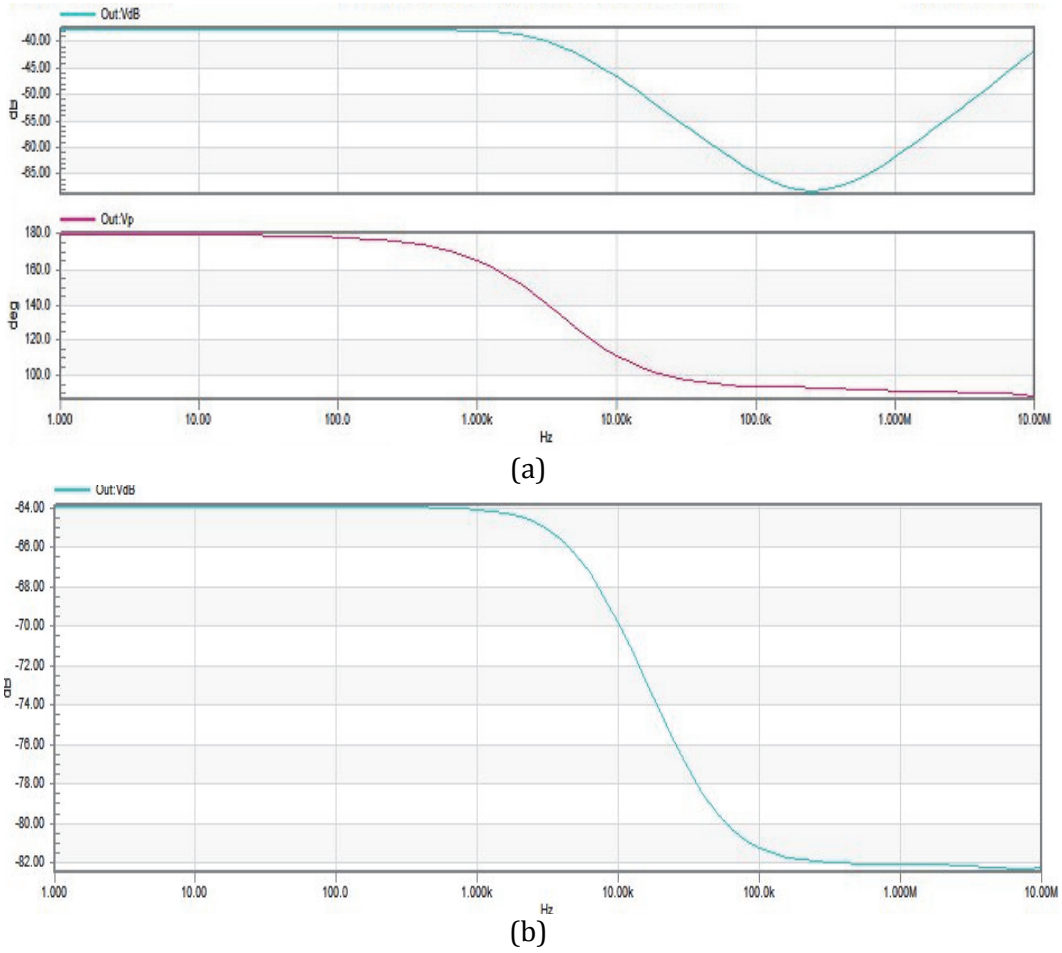


Figure 6. Common mode gain at (a) 2.5V and (b) 1.5V supply voltage.

A square wave was given to the inputs of the differential stage, and the transient analysis gave the simulation results. The Slew rate actually represents the current available to drive the load capacitance. The slew rate for the proposed designs can be evaluated from Figure 7.

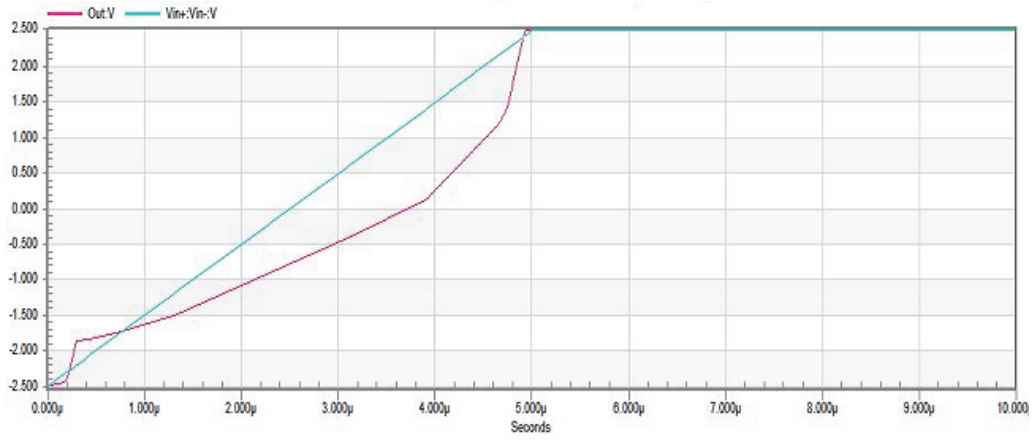
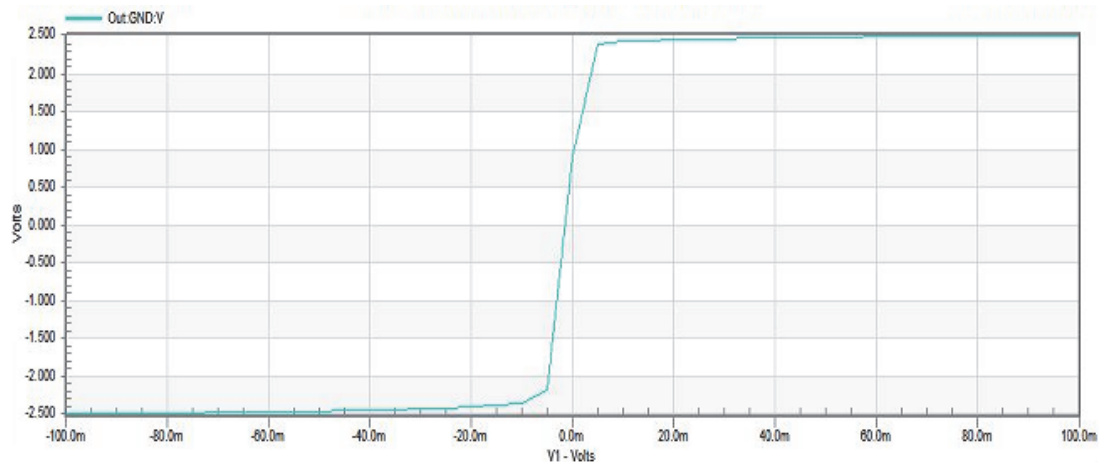
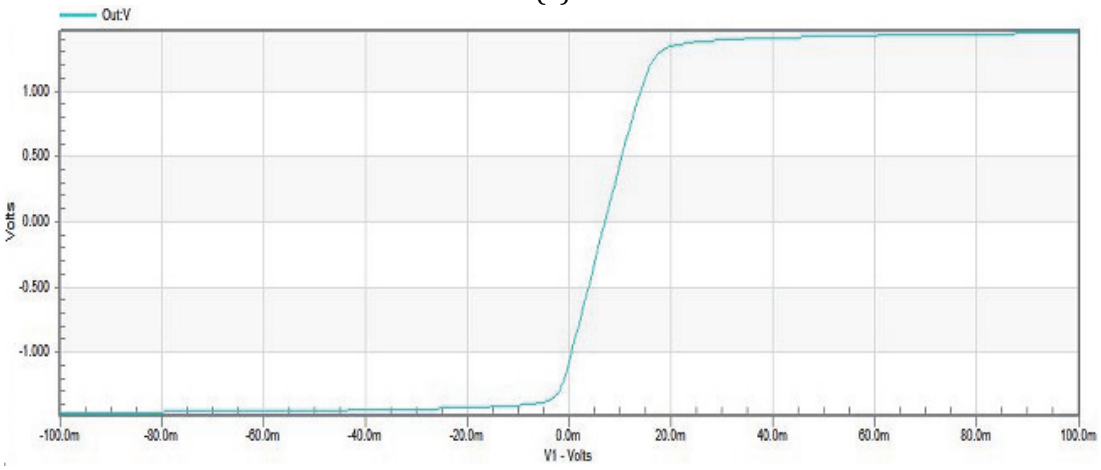


Figure 7. Slew rate at 2.5V.



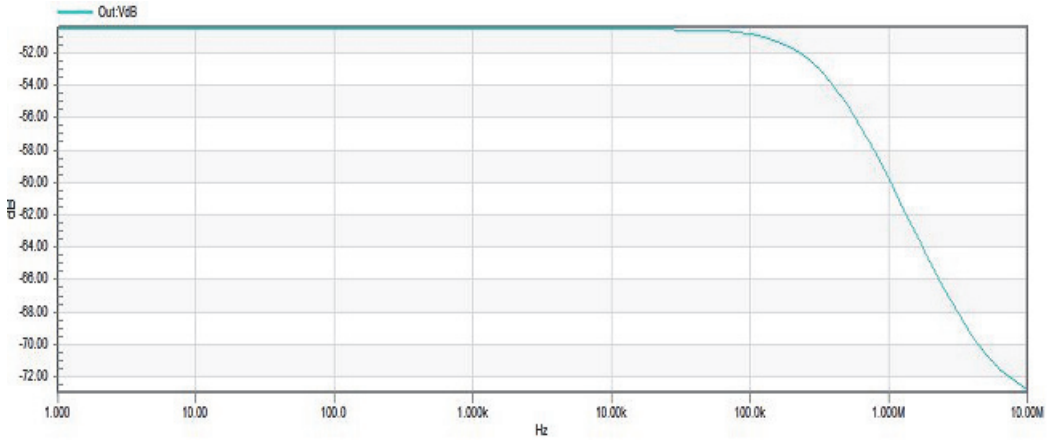
(a)



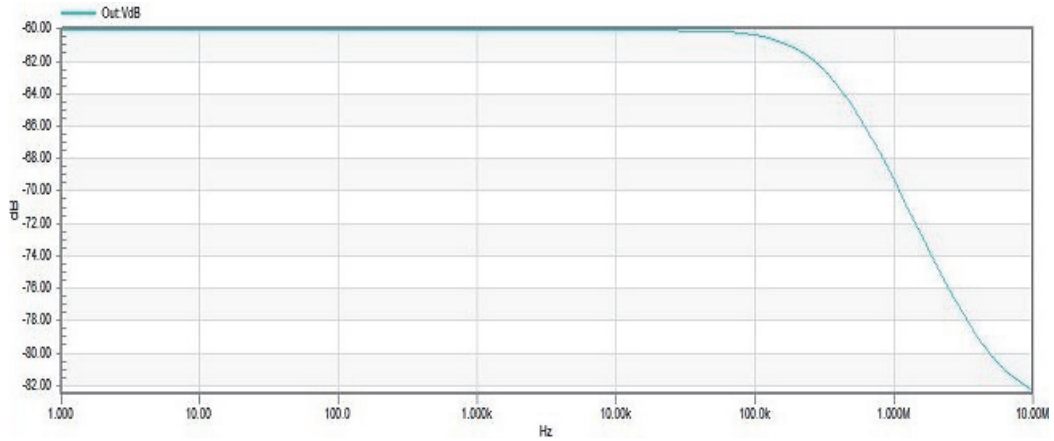
(b)

Figure 8. Output swing at (a) 2.5V and (b) 1.5V supply voltage.

The output swing represents the values of the maximum positive and negative voltages above which transistor will remain out of saturation and thus specifies the range over which output voltage can vary without excessive distortion. The graphs in Figure 8 shows the voltage swing from -2.5V to +2.5V. The OTA provides a wide swing, meaning the input CMR is close to the supply voltages. The output swing is limited by the supply voltages as is evident from Figure 8.



(a)



(b)

Figure 9. PSRR at (a) 2.5V and (b) 1.5V supply voltage.

If there is a change X in the supply voltage that produces an output voltage change of Y volts, then the PSRR is expressed as a ratio of X/Y. This quantity is expressed in dB. The PSRR can be a positive or negative quantity. To determine the PSRR, DC bias was applied to the inputs of the differential stage and an AC Voltage was applied to the positive V_{DD} terminal to determine the PSRR +. For the proposed designs, the PSRR can be calculated from the graph shown in Figure 9.

This paper first presents the design of a preamplifier for cardiac implants designed at a supply voltage of 2.5 V, where a high gain of around 60dB was obtained but the power consumption is slightly high. Therefore, further optimization was done where a supply voltage of 1.5 V was obtained. The average power consumption reduced to 61.10μW at the expense of a reduced gain of 50dB. Also, there is an improvement in the noise spectral density at 1.5V. The performance parameters of the proposed and optimized designs are summarized in Table 5.

Table 5 Comparsion of Proposed and Optimized Preamplifier Designs

Specification	Proposed Design	Optimized Design
Supply Voltage	**2.5 V**	**1.5V**
Open Loop Gain	62dB	50dB
Phase Margin	-95.83º	-92.02º
CMRR	102dB	114dB
PSRR+	-50dB	-60dB
Power Consumption	0.131mW	61.10µW
Output Swing	-2.5V to 2.5V	-1.4V to 1.4V
Noise Spectral Density	250µV/$\sqrt{Hz}$ at 100mV input	3.5µV/$\sqrt{Hz}$ at 100mV input

The state of the art comparison of the proposed low power preamplifier with some other related work is given in Table 6. A gain of 50dB, a low power consumption of 61.10μW, and a high CMRR of 94dB were achieved, which are suitable for the cardiac applications. Also, an improvement in the noise spectral density is quite evident from the table.

Table 6 Performance Comparison of Proposed Preamplifier

Parameter	[21]	[22]	[23]	[24]	This Work
Technology (μm)	0.6	0.35	0.18	0.18	**0.18**
Gain (dB)	39.4	20.4	40	63.06	**50**
Power Consumption (W)	2.4μ	23.1μ	-	0.0154m	**61.10μ**
CMRR (dB)	66	-	82	-	**114**
PSRR (dB)	80	-	-	-	**60**
Supply Voltage (V)	2.8	3.3	1.8	1.8	**1.5**

5. CONCLUSION

Parameters such as size, weight, and battery are of prime importance in cardiac implants. As the industry of the medical implantable devices develops, lowering the power consumption as much as possible is essential in improving the service time of the battery, which cannot be replaced frequently. Hence, a low voltage operation becomes critical to achieve a low power consumption. This paper presents the design and optimization of an OTA based preamplifier for cardiac application. The preamplifier provides a gain of 50dB at a supply voltage of 1.5V and a low power dissipation of 61.10μW, thereby making it suitable for this particular application. The trade-offs between various parameters such as gain and power consumption are also evident in the optimized design. In the future, further optimization to an ultra-low power level can be done. Also, different applications such as retinal prostheses, EOG, and PCG can be considered since much of the work is done on neural implantable devices.

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