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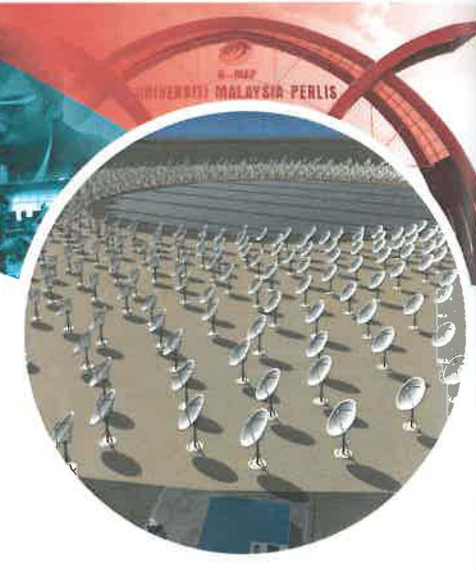

HIGH ACCURACY LINEAR AND NONLINEAR MODELS FOR pHEMT DEVICES

INVENTORS

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PRODUCT DESCRIPTIONS

- An accurate linear and nonlinear models of a transistor or also known as transistor model is an essential requirement for any circuit design. Therefore, there is a continuous effort from circuit designers to produce efficient transistor model. The high accuracy of transistor model will enable the designer to predict the real output of the circuit before the design is fabricated into the actual chip.
- These days, the models for CMOS transistor using silicon technology are well established. These CMOS transistor models are ready to most of Computer Aided Design (CAD) software such as CADENCE and Mentor Graphics. However, for advanced devices from other high frequency materials like InP pseudomorphic High Electron Mobility Transistor (pHEMT), the transistor models still an issue. Therefore, there are many effort carried out to publish the best method for higher accuracy of the pHEMT transistor models.
- Consequently, this work presents the high accuracy linear and nonlinear models of InP pHEMT devices for circuit designs especially in high speed, high frequency, low noise applications such as Low Noise Amplifier (LNA).

NOVELTIES

- Device modeling technique for highly strained, high speed pHEMT mainly for satellite communication.
- First time a simplistic modeling step has been developed to assess circuit performance of InP pHEMT devices.
- Accurate simulation of circuit's DC and RF characteristics. It has been validated against measured data and found to be in very close agreement.

COMMERCIALIZATION POTENTIAL

- Developed datasheet or transistors library of InP pHEMT devices for CAD tools: CADENCE, ADS, Mentor Graphics

APPLICATIONS

- **Astronomy:**
  LNA in radio astronomy satellite dish
- **Military:**
  Secure frequency for UAV, military communication
- **Communication:**
  Mobil communication - high speed application
- **Medical:**
  High frequency skin care machine, Wireless communication between machines

COLLABORATIONS

ELVIRA Systems Sdn Bhd

ARM

MANCHESTER 1824 The University of Manchester

pHEMT TRANSISTORS

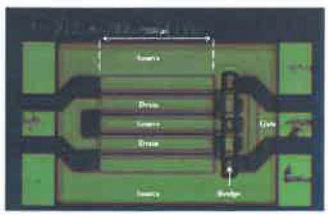

Fig. 1 Fabricated transistor (4 x 200 µm gate width device with LG = 1 µm)

Epitaxial layer	Device width	Gate length	Note
XMBE144	2 x 50 µm (W_T = 100) 2 x 100 µm (W_T = 200) 4 x 200 µm (W_T = 800)	1.00 µm	Low gate leakage epitaxial layer
VMBE2100	4 x 200 µm (W_T = 800)	1.00 µm	Extremely low gate leakage epitaxial layer
XMBE131	2 x 50 µm (W_T = 100) 2 x 200 µm (W_T = 400)	0.35 µm	Submicron epitaxial layer

Table 1 Summary of the fabricated and modelled devices. W_T = Devices' total width and S-D = 5 µm

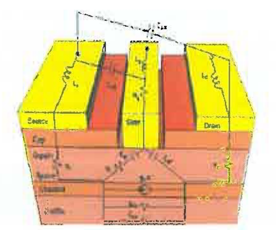

Fig. 2 Physical origin of the pHEMT/HEMT linear equivalent circuit model

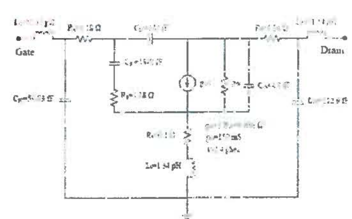

Fig. 3 The optimised Linear Model (with extrinsic and intrinsic values) for the XMBE144 4 x 200 µm device

DC & RF PARAMETER MODELS

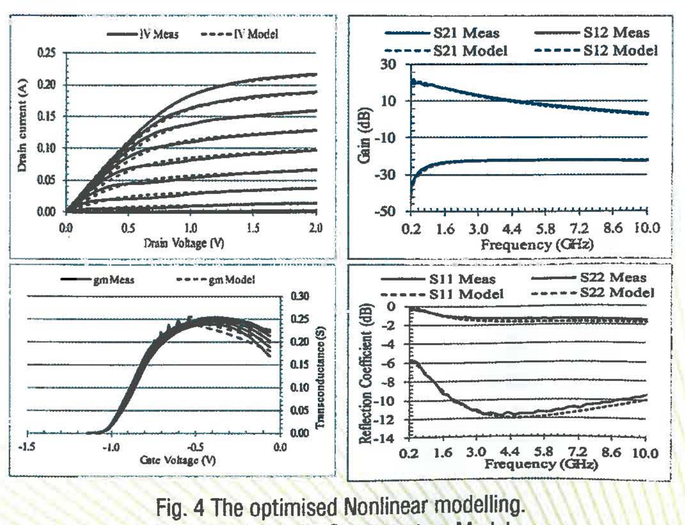

Fig. 4 The optimised Nonlinear modelling. (a) RF Model; (b) S-parameters Model

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