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# UTBB SOI MOSFETs analog figures of merit: Effects of ground plane and asymmetric double-gate regime

## Abstract

In this work we investigate the effect of ground plane (GP) on analog figures of merit (FoM) of ultra-thin body and thin buried oxide (UTBB) SOI MOSFETs. Based on experimental devices, both n- and p-type GP configurations are considered and compared with standard no-GP substrates. In a standard single-gate (SG) regime, the effect of GP implementation on analog FoM (related to slightly higher body factor and improved gate-to-channel coupling) is negligible. Moreover, p-GP implementation allows higher intrinsic gain at high frequency compared with no-GP and n-GP substrates. Furthermore, we demonstrate that application of an asymmetric double-gate (ADG) (i.e. front-gate to back-gate/substrate connection) regime allows better control of short-channel effects in terms of drain induced barrier lowering, subthreshold slope and threshold voltage control, due to improved gate(s)-to-channel coupling. Application of an ADG mode is shown to enhance analog FoM such as transconductance, drive current and intrinsic gain of UTBB SOIMOSFETs. Finally, simulations predict that improvements of analog FoM provided by ADG mode can be obtained in the whole dynamic operation range. Moreover, ADG mode provides elimination of the high-frequency substrate coupling effects.

### Keywords

Analog figures of merit; Asymmetrical double gate; Ground plane (GP) implementation; Ultra-thin body and thin buried oxide FD SOI MOSFETs