CHAPTER FOUR

RESULTS AND DISCUSSION

4.1 Introduction

In this chapter, we describe the implementation of the encoder and decoder modules to the new OCDMA systems based on Fiber Bragg Gratings (FBGs). The results which are obtained mainly from the simulation works are presented. In this simulation analysis, the study will focus on the encoder and decoder modules to encode and decode a newly developed Spectral Amplitude Spectral (SAC) code known as Modified Double Weight (MDW) code. Details about MDW code will be explain in the subtopic of results. The results are taken from studies on the effect of input power and bit rate.

The results from this simulation will show the differences between parallel and serial configurations. From these results, we will know which configuration give better performance from the graphs show in this section.

4.2 Simulation Setup for Encoder and Decoder Modules

The setup model for encoder and decoder modules in this design are shown in figures and will be explain details in this section. In the transmitter part, each of transmitters consists of six components; a dc bias generator, a LED, Uniform Fiber Bragg Gratings (FBGs), a pseudo random bit sequence (PRBS) generator, a Non-Return to Zero (NRZ) pulse generator and a Mach Zehnder Modulator. The Single Mode Fiber cable (10km) acted as the interface to connect from transmitter side to receiver side. The receiver side consists of Uniform Fiber Bragg Gratings (FBGs), PIN Photodetector, Low Pass Bessel Filter, Electrical Subtractor and Eye Diagram.

4.2.1 MDW Code

The encoder and decoder modules developed in this project are mainly designed for the DW code family. In this work, we investigating the serial and parallel configurations of encoder and decoder modules to encode and decode a newly developed Spectral Amplitude Coding (SAC) known as Modified Double Weight (MDW) code. MDW code is developed in a family of the Double Weight (DW) code [1]. This coding scheme is designed in a way to decrease the number of FBGs used in the encoder and decoder modules to maintain the cross-correlation, λ_c parameter to 1. Basically, MDW allows the code weight to be in any even number which is greater than two. The basic of this code is donated by (n, w, 1) for the code length n, code weight w while the in-phase cross-correlation λ_c is always maintained at 1, respectively.

Furthermore, MDW code can eliminate Multiple Access Interference (MAI) and suppress Phase Induced Intensity Noise (PIIN) completely by employing the detection technique called AND-subtraction technique [2-3]. In MDW code, the chips which represent the high bits of a code sequence are always allocated in pair. Thus, the number of FBG used for encoder or decoder can be reduced by half since a pair of chips can be covered by a single FBG with a broader linewidth.

Table 4.1: Wavelength assignment for MDW codes

λ_1	λ_2	λ_3	λ_4	λ_5	λ_6	λ_7	λ_8	λ_9
1549 .95	1550 .35	1550 .75	1551 .15	1551 .55	1551 .95	1552 .35	1552 .75	1553 .15
0	0	0	0	1	1	0	1	1
				1551.75			1552.95	
0	1	1	0	0	0	1	1	0
	1550.55					1552.55		

4.2.2 Parallel Configurations

The design setup consists of a single LED broadband source and two channels of point-to-point transmission using MDW of 4 codes weight. The AND-subtraction scheme is used as the detection scheme at the receiver part.

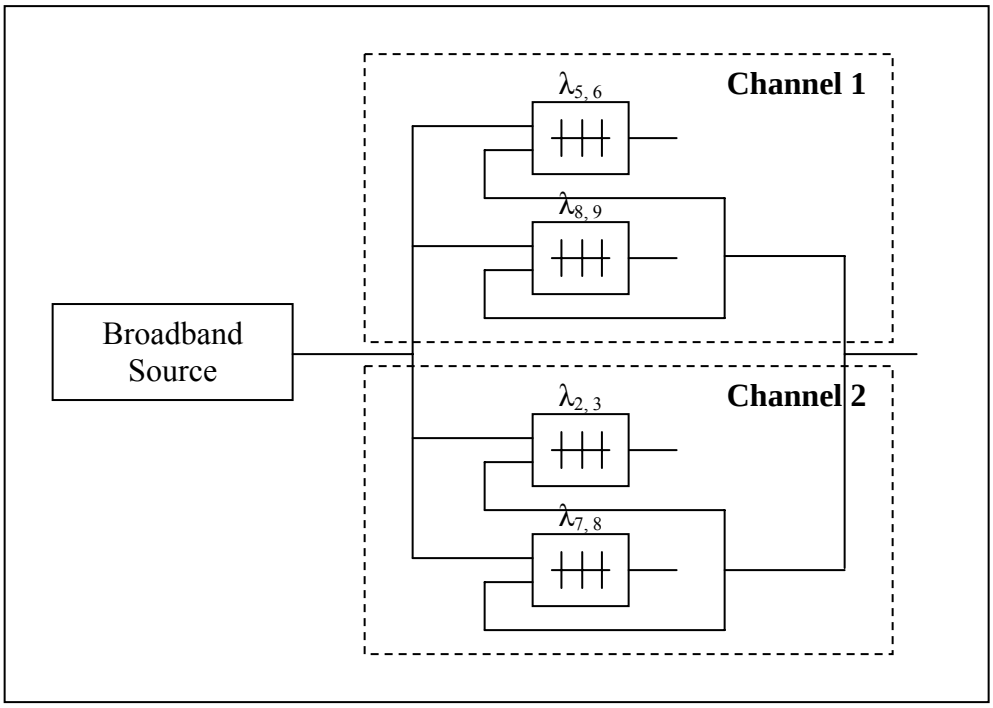

Figure 4.1: Parallel Configuration Encoder Module

Figure 4.1 above shows the encoder module for parallel configuration where a single FBG will encode two wavelengths (or two chips) which are represented by the wavelength values of 1551.75nm ($\lambda_{5,\ 6}$) and 1552.55nm ($\lambda_{8,\ 9}$) for the first code, and 1550.55nm ($\lambda_{2,\ 3}$) and 1552.55nm ($\lambda_{7,\ 8}$) for the second code as shown in Table 4.1. It shows that the correlated chip is at the same wavelength which is at 1552.75nm. Every FBG would encode 2 combined chips which represented in the shading areas of Table 4.1. This is because of every chip in MDW code is designed in pair. This would reduce the number of FBG used in encoder and decoder modules.

At the receiver part, the same FBG configuration at the decoded branch is used to decode the data shown in Figure 4.2.

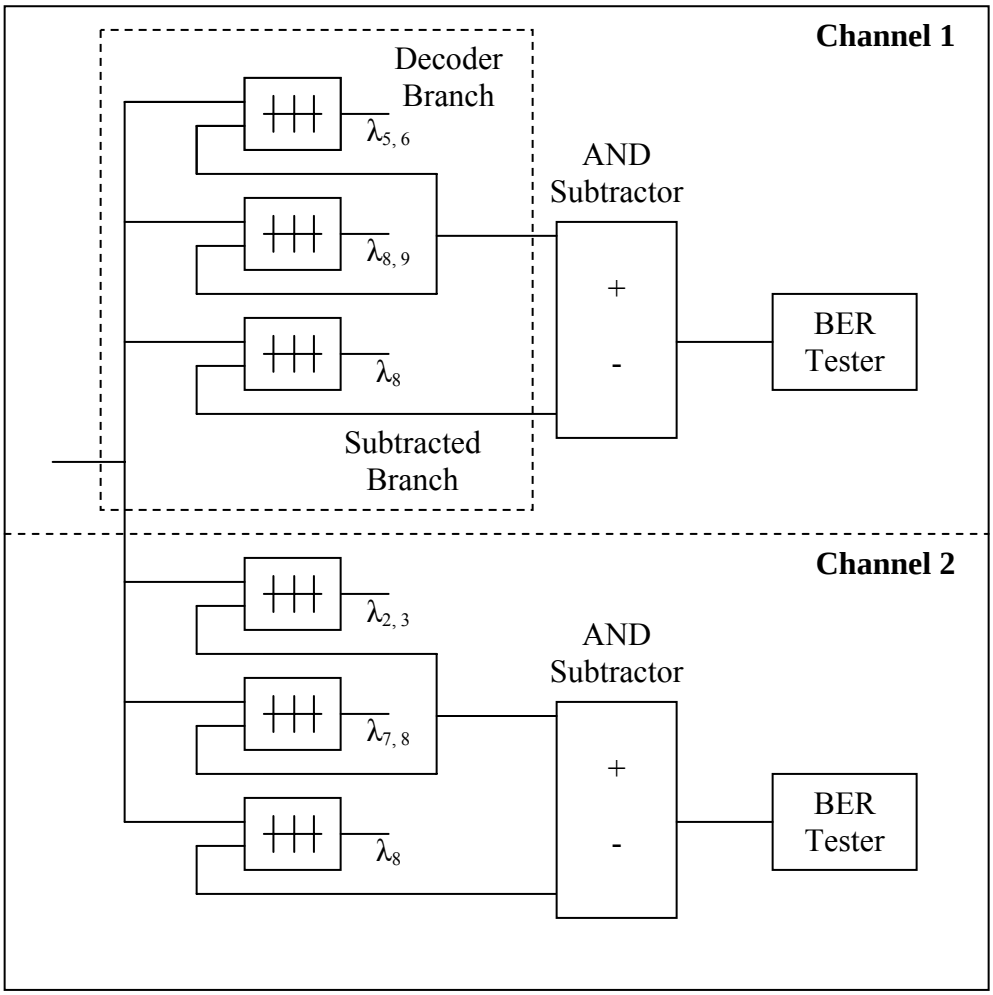

Figure 4.2: Parallel Configuration Decoder Module

An AND-subtraction technique is used to deal with the correlated signal. The signal obtained at the decoded branch is subtracted with the correlated or overlapping chip between the two code sequences at the subtracted branch. This will eliminate the unwanted signal introduced by the identical wavelength which is used at the other code sequence [1].

Three FBGs were used to decode the code sequence with 4 chip width. The AND-subtraction scheme will subtract the correlated chip denoted by λ_8 to obtain the original data of the respective channel.

4.2.2.1 Simulation Design of Parallel Configuration

Figure 4.3 below shows a design of encoder and decoder modules which in parallel configuration. The design is done with using the OptiSystem Software.

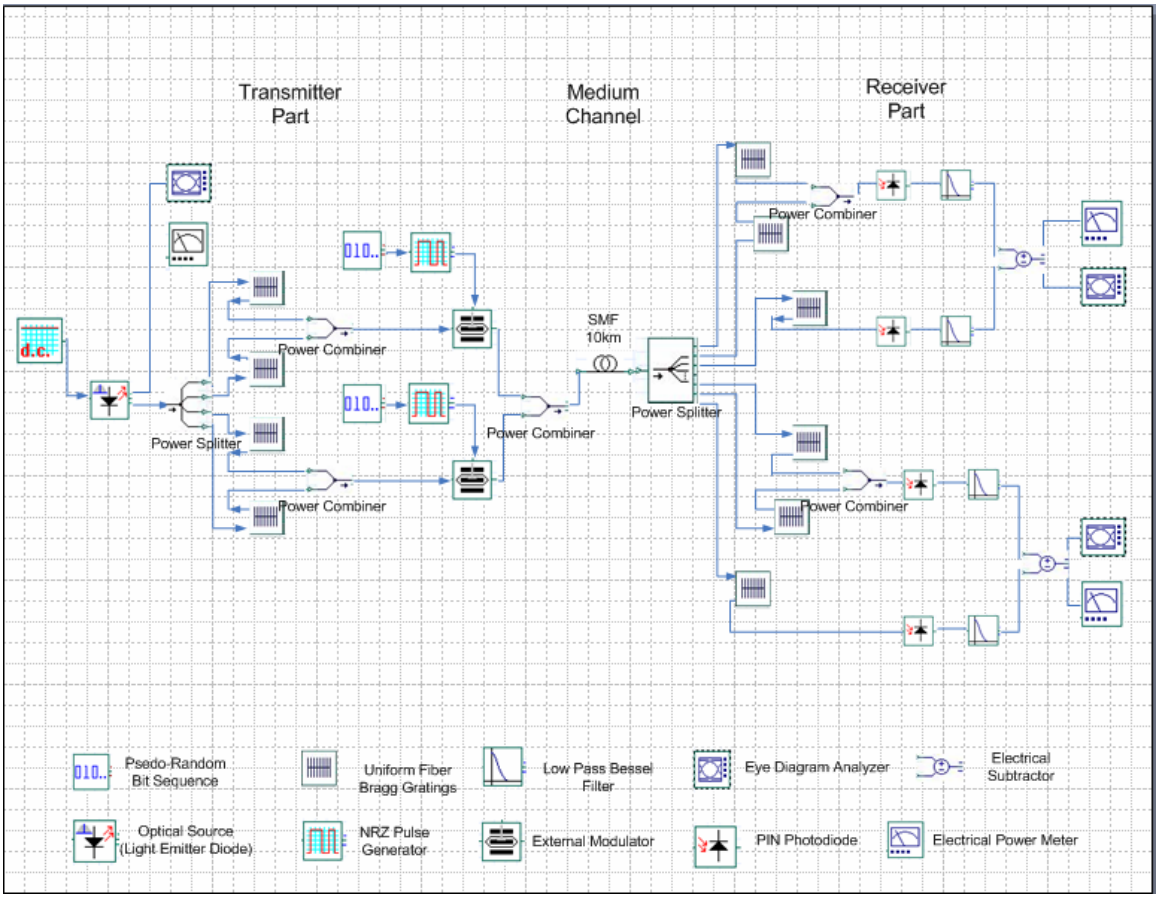

Figure 4.3: The design of Parallel Configuration in simulation software

4.2.3 Serial Configuration

Figure 4.4 shows the encoder modules of the serial configuration. A serial arrangement of FBGs is used to encode the wavelengths. The reflected branches are combined to construct the code. In Channel 1 for example, the transmitted branch of the first FBG ($\lambda_{5,\ 6}$) connected to the second FBG ($\lambda_{8,\ 9}$) is compared to the parallel configuration where all FBGs are linked directly to the broadband source. As shown in Figure 4.4 a serial configuration only need a 1-to-2 power splitter from LED broadband source for 2 channels of users, whereas in Figure 4.1 for parallel configuration, a 1-to-4 power splitter is required to accommodate 2 channels of users. This may introduce a higher power loss for the parallel configuration.

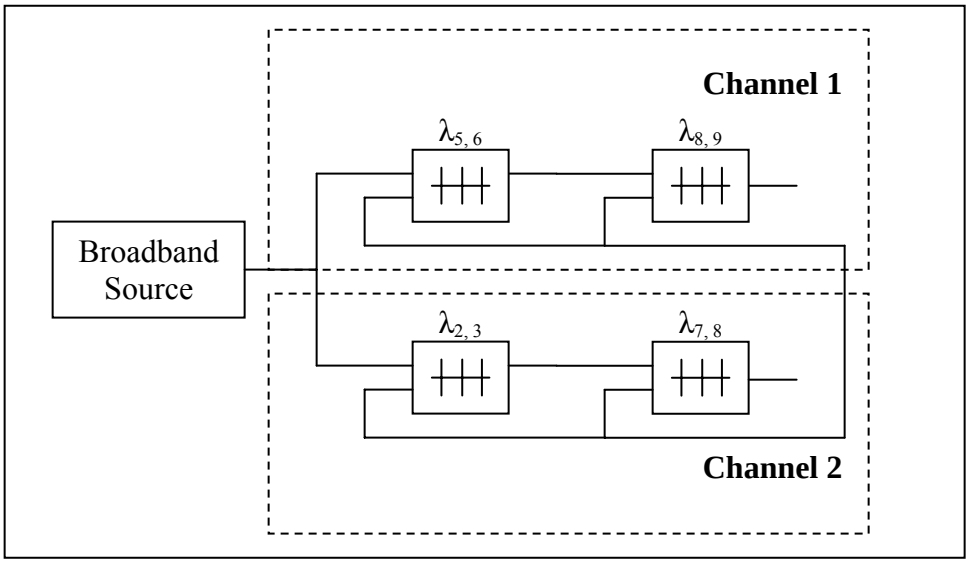

Figure 4.4: Serial Configuration Encoder Module

The decoder module for the serial configuration is shown in Figure 4.5. The reversed order of FBGs from the serial configuration is used to decode the code sequence which can be found in many serial configuration encoder designs [4-5].

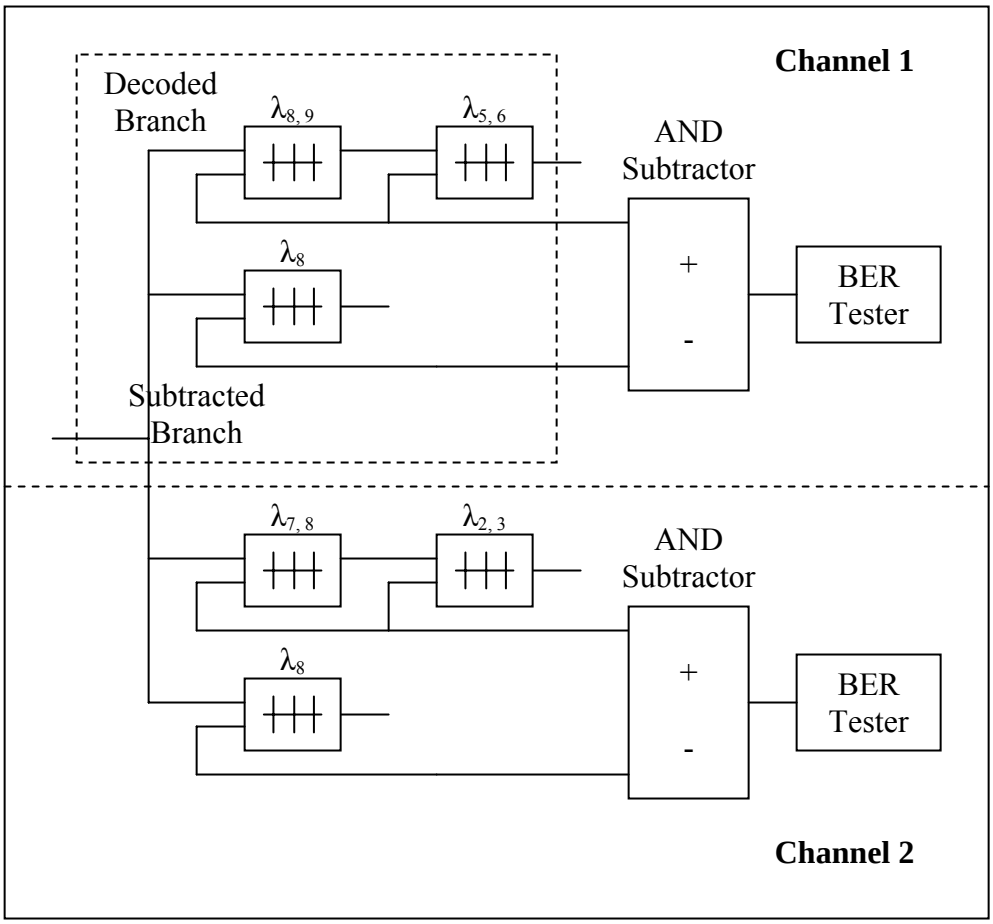

Figure 4.5: Serial Configuration Decoder Module

For example, $\lambda_{8,9}$ in Channel 1 will reach the encoder first and followed by $\lambda_{5,6}$ according to the arrangement of the FBGs at the encoder part.

4.2.3.1 Simulation Design of Serial Configuration

Figure 4.6 below shows a design of encoder and decoder modules which in serial configuration. The design is done with using the OptiSystem Software.

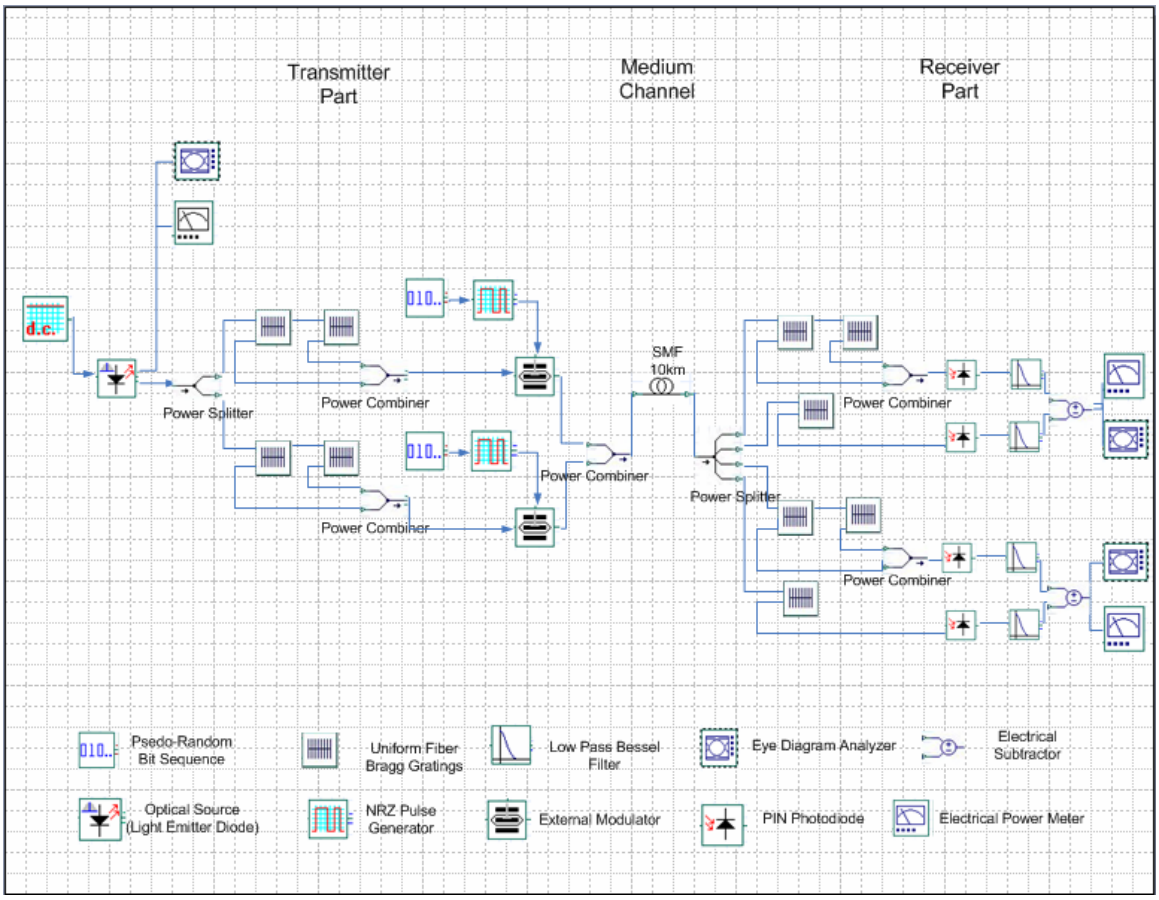

Figure 4.6: The design of Serial Configuration in simulation software

4.3 Simulation Results for Parallel and Serial Configuration

The system setup consists of a single LED source and 2 channels point-to-point transmission with 4 codes weight. The system is modulated with a 622 Mbps bit rate with a transmit power of 8 dBm of the LED source. A high input power is required since the system setup only used a single broadband source to support multiple users in the system. In reality, high input power can be achieved using standard optical amplifier.

Figure 4.7 (a) and (b) shows the encoded spectra for parallel configuration respectively. The spectra are encoded at 1551.75 nm and 1552.95 nm for Channel 1 and 1550.55 nm and 1552.55 nm for Channel 2.

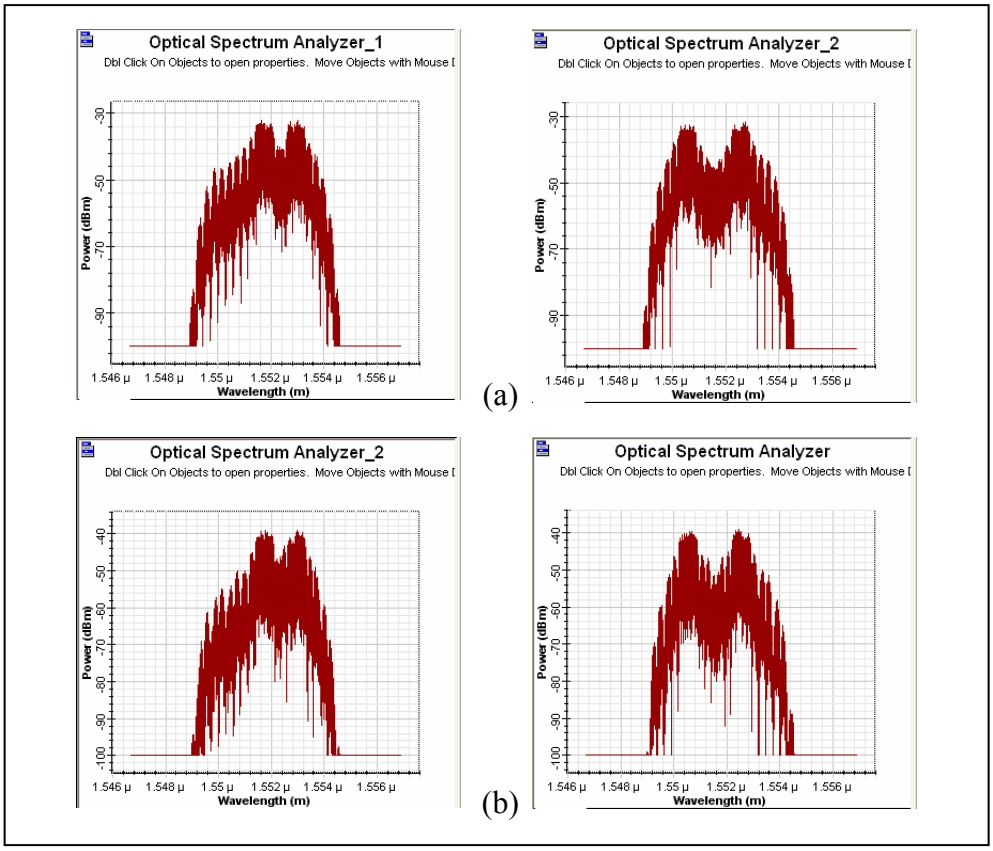

Figure 4.7: Encoded spectra at 1551.75nm and 1552.95nm, 1550.55nm and 1552.55nm for Channel 1 and Channel 2 respectively (a) Spectra of Parallel configuration encoder (b) Spectra of Serial configuration encoder

The decoded spectra of every channel represented at the decoded and subtracted branch are shown in Figure 4.8 (a) and (b) for the serial and parallel configuration respectively.

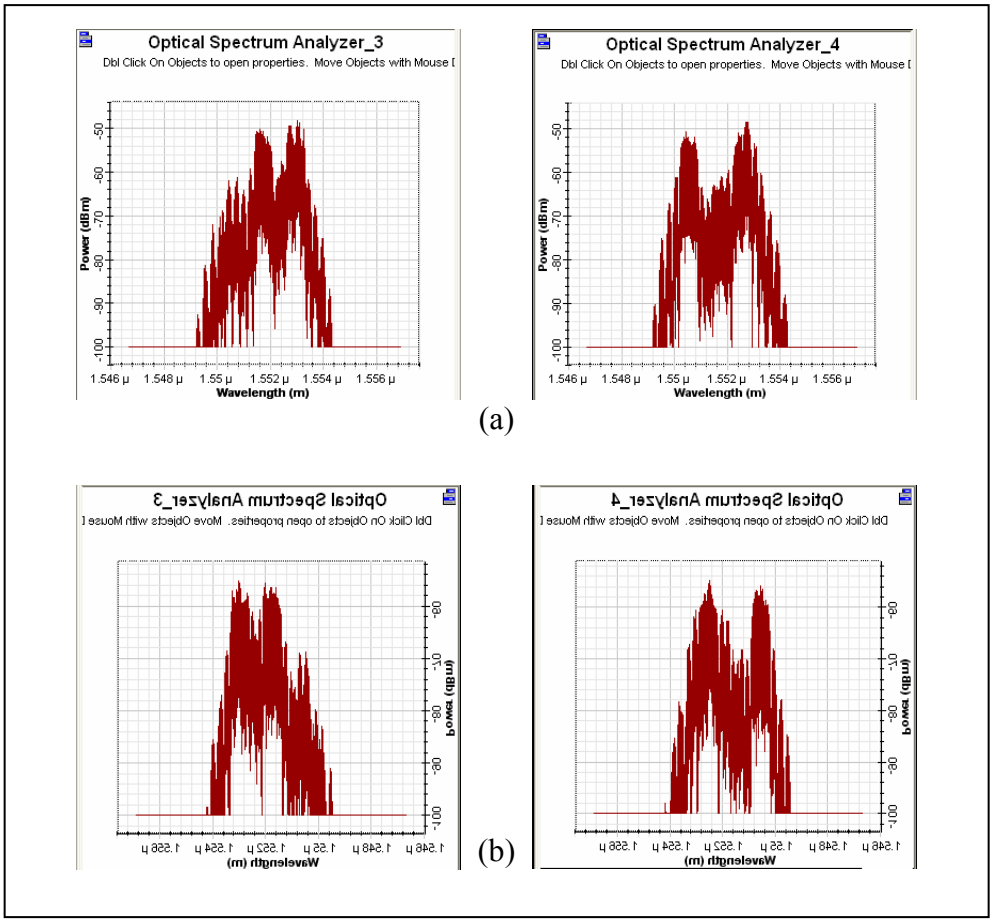

Figure 4.8: (a) Channel 1 decoded spectra of parallel configuration at the decoded branch of 1551.75nm and 1552.95nm and the spectrum of the subtracted branch at 1552.75nm.
(b) Channel 2 decoded spectra for serial configuration at the decoded branch of 1550.55nm and 1552.55nm and the spectrum of the subtracted branch at 1552.75nm.

4.3.1 Effect of Input Power in Point-to-Point Transmission Network

If the signal is too weak when it reaches the far end of the system the data will be difficult to separate from the noise. This will cause the number of errors in the received data bits to increase. The problem can be solved by keeping the input power or the transmitted power to a higher value.

4.3.1.1 Effects of Input Power on System Performance at Bit Rate 622Mbps for Parallel Configurations

Figure 4.9 shows the performance of the OCDMA system at bit rate of 622Mbps for 10km multiple access point-to-point transmission which using parallel configuration connection.

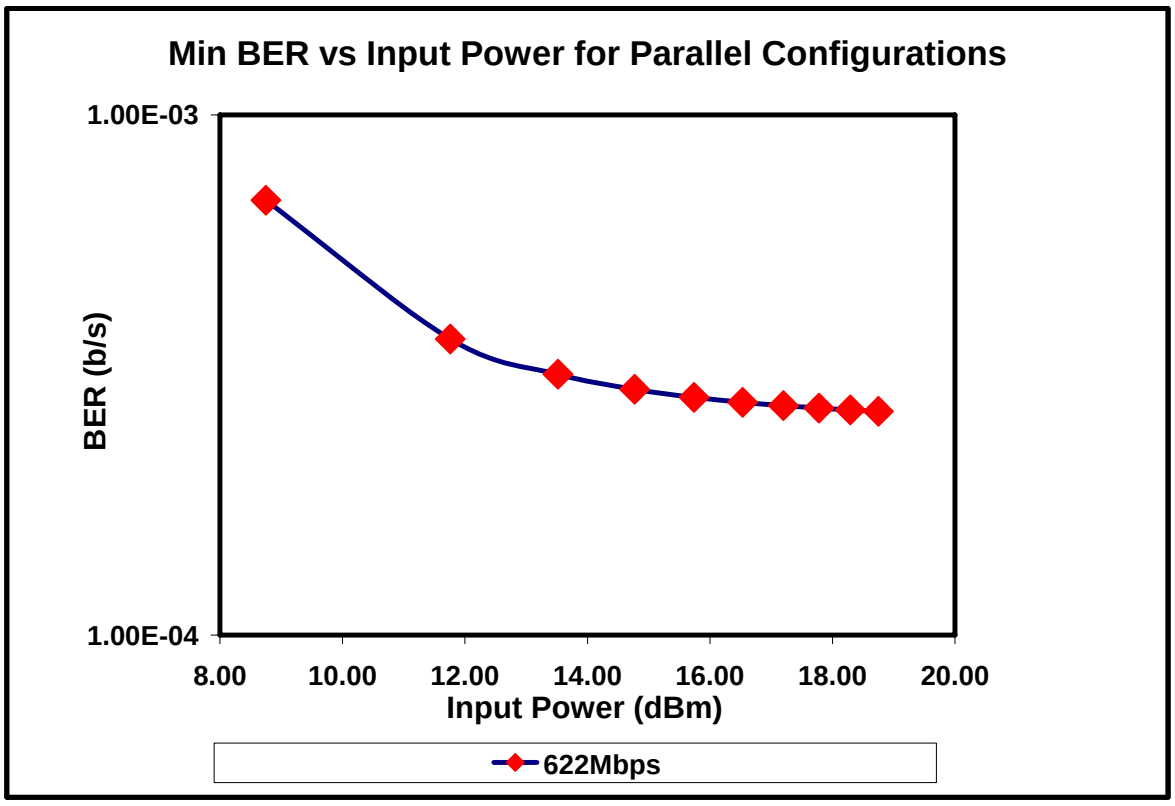

Figure 4.9: BER versus Input Power for OCDMA System at Bit Rate of 622Mbps

From the performance graph shows in Figure 4.9, the BER reduced exponentially when the input power increased. The parallel configuration for this design can support a transmission distance of 10km for input power increased from 8.75dBm to 18.75dBm. For input power of 18.75dBm can support the BER to 2.69×10^{-4} taking the average of Channel 1 and Channel 2 for 622Mbps of bit rate performance.

4.3.1.2 Effects of Input Power on System Performance at Bit Rate 622Mbps for Serial Configurations

Figure 4.10 shows the performance of the OCDMA system at bit rate of 622Mbps for 10km multiple access point-to-point transmission which using serial configuration connection.

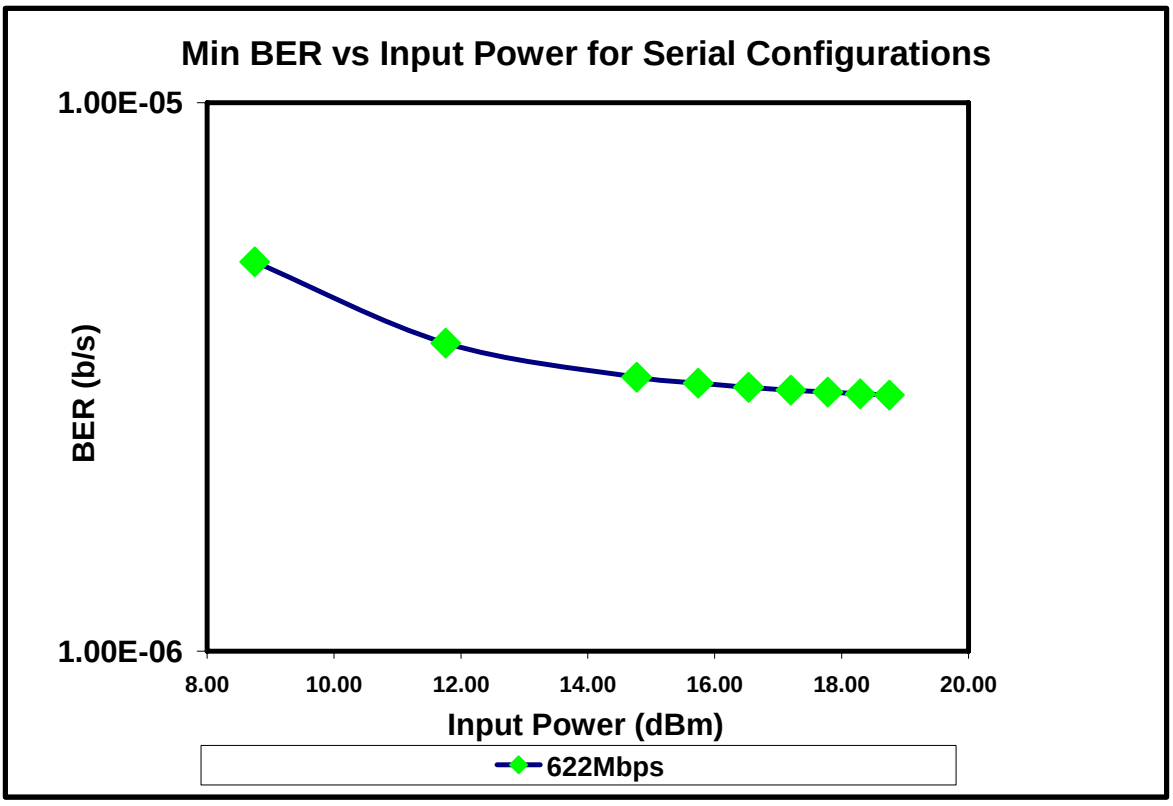

Figure 4.10: BER versus Input Power for OCDMA System at Bit Rate of 622Mbps

Approximately with the parallel configuration, the BER also reduced exponentially when the input power increased. The serial configuration for this design can support a transmission distance of 10km for input power increased from 8.75dBm to 18.75dBm. For input power of 18.75dBm can support the BER to 2.93×10^{-6} taking the average of Channel 1 and Channel 2 for 622Mbps of bit rate performance.

4.3.1.3 Comparison of Parallel and Serial Configurations on effects of Input Power on BER

Figure 4.11 shows the comparison between parallel and serial configuration for performance of the OCDMA system at bit rate of 622Mbps for 10km multiple access point-to-point transmission which using serial configuration connection.

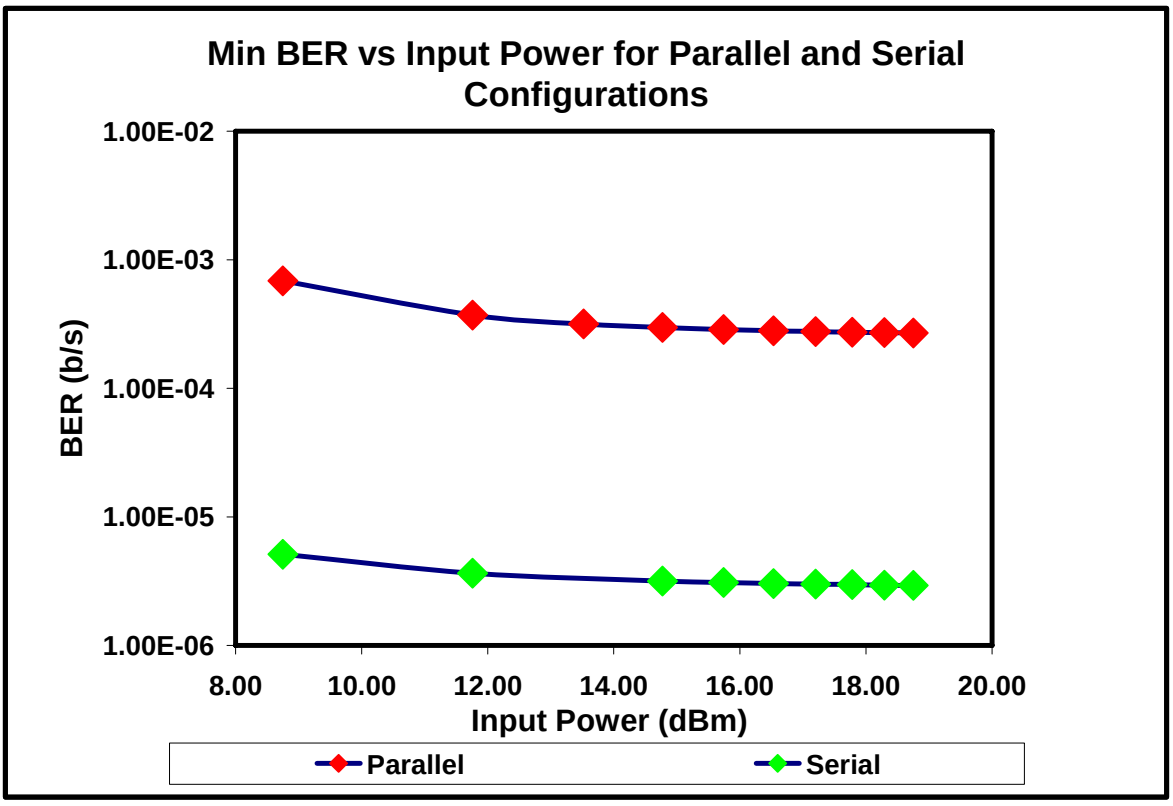

Figure 4.11: Comparison between parallel and serial configuration of BER versus Input Power for OCDMA System at Bit Rate of 622Mbps

4.3.2 Effect of Bit Rate in Point to Point Transmission Network

In the simulation, the transmission bit rate was varied by changing the numerical values in the dialog box at the transmitter section. A range of bit rate from 100Mbps to 1.5Gbps was chosen for the simulation. The different between parallel and serial configuration results are obtained from the performance graph shows in this section. The fiber length was fixed to 10km, while the input power of LED is 8dBm, and all other parameters were made constant.

4.3.2.1 Effect of Bit Rate on System Performance for Parallel Configurations

The effect of bit rate for parallel configuration in this design is shown in Figure 4.12. In the figure, the bit error rate increases with the bit rate. This can be explained that the increasing of bit rate will be decrease the pulse width, thus making the bits more sensitive to dispersion effect. The results shows that, at the fixed distance of 10km on a SMF, the OCDMA system are running on MDW codes could support bit rates of up to 1Gbps with BER of 2.18×10^{-3}. But unfortunately, this parallel configuration's result not given a better performance if compared to the serial configuration which will explain based on Figure 4.11. At 1Gbps though, the bit rate became too fast for the system and was not supported well.

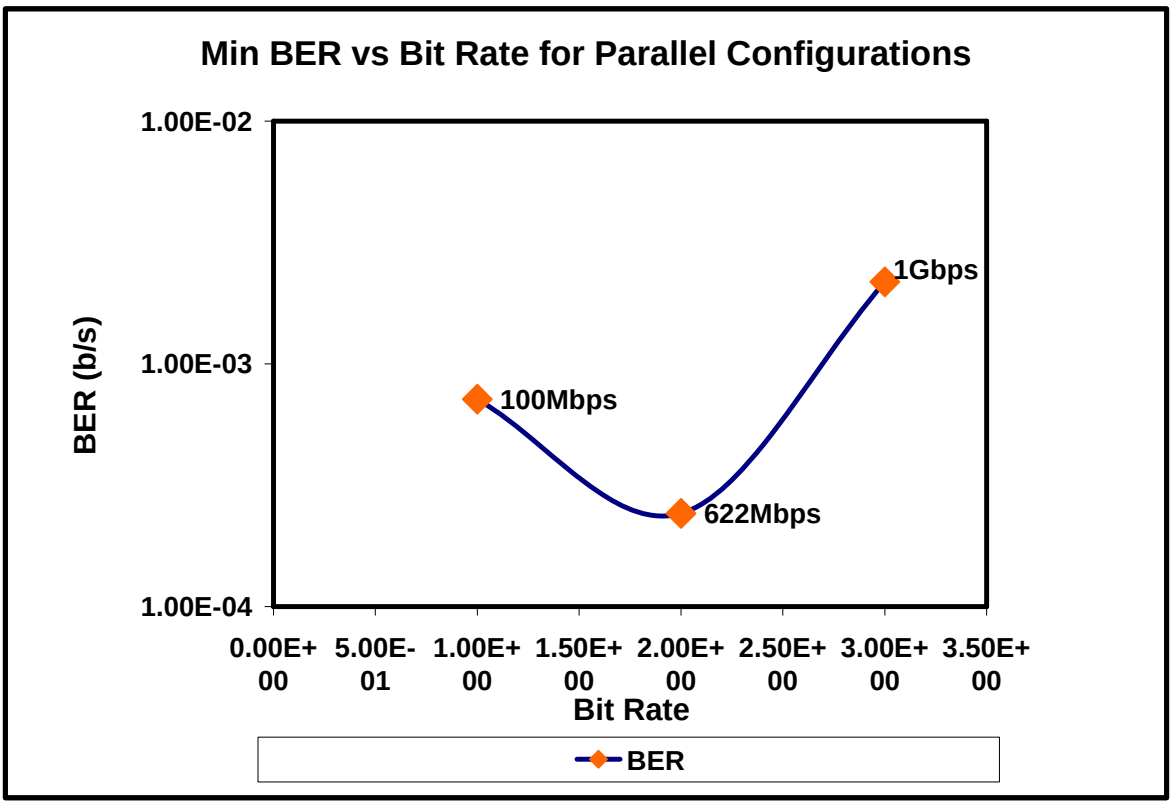

Figure 4.12: BER versus Bit Rate

4.3.2.2 Effect of Bit Rate on System Performance for Serial Configurations

The effect of bit rate for serial configuration in this design is shown in Figure 4.13. Such in the figure for parallel configuration, the error rate increases with the bit rate. This can be explained that the increasing of bit rate will be decrease the pulse width, thus making the bits more sensitive to dispersion effect. The results shows at the fixed distance of 10km on SMF and the OCDMA system running on MDW codes could support bit rates of up to 1.5Gbps with BER of 7.73 x 10^{-4}. Compared with parallel configuration's performance graph, the serial configurations gave a better performance on effect of the bit rate. The system still supports for bit rate 1.5Gbps. These results are taking the average of Channel 1 and Channel 2.

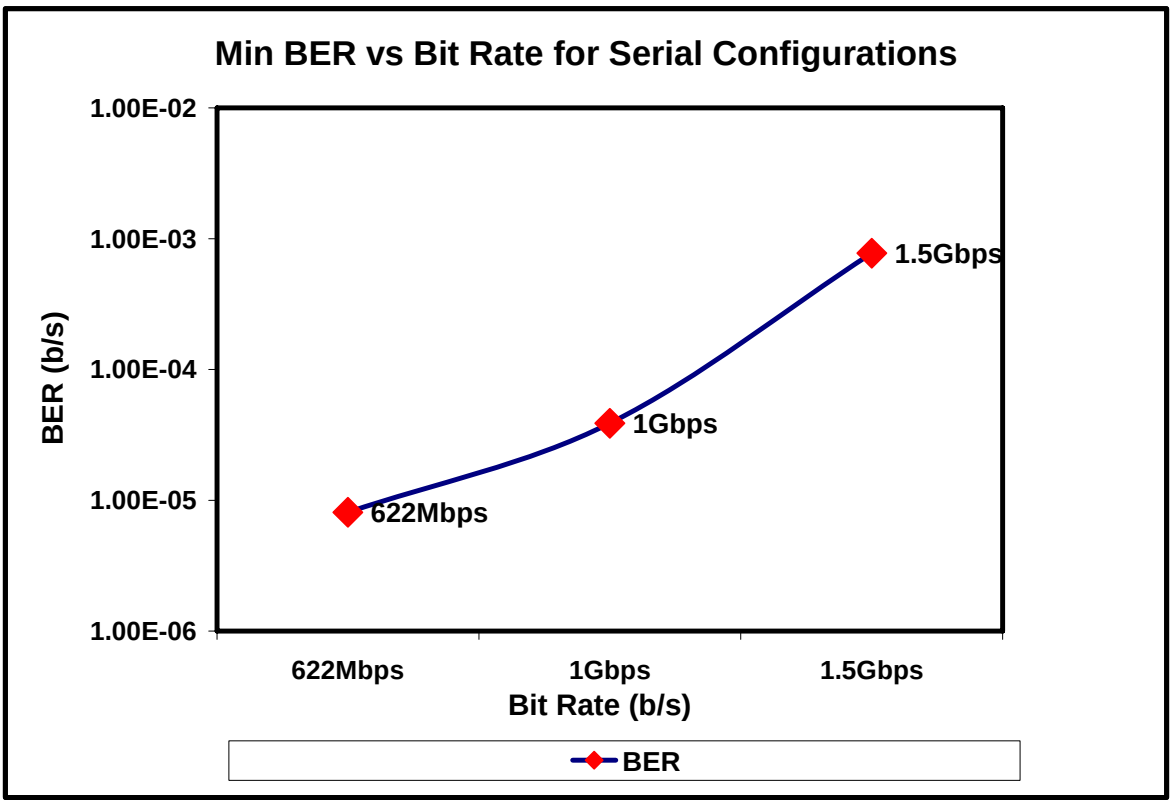

Figure 4.13: BER versus Bit Rate

4.3.2.3 Comparison of Parallel and Serial Configurations on effects of Bit Rate on BER

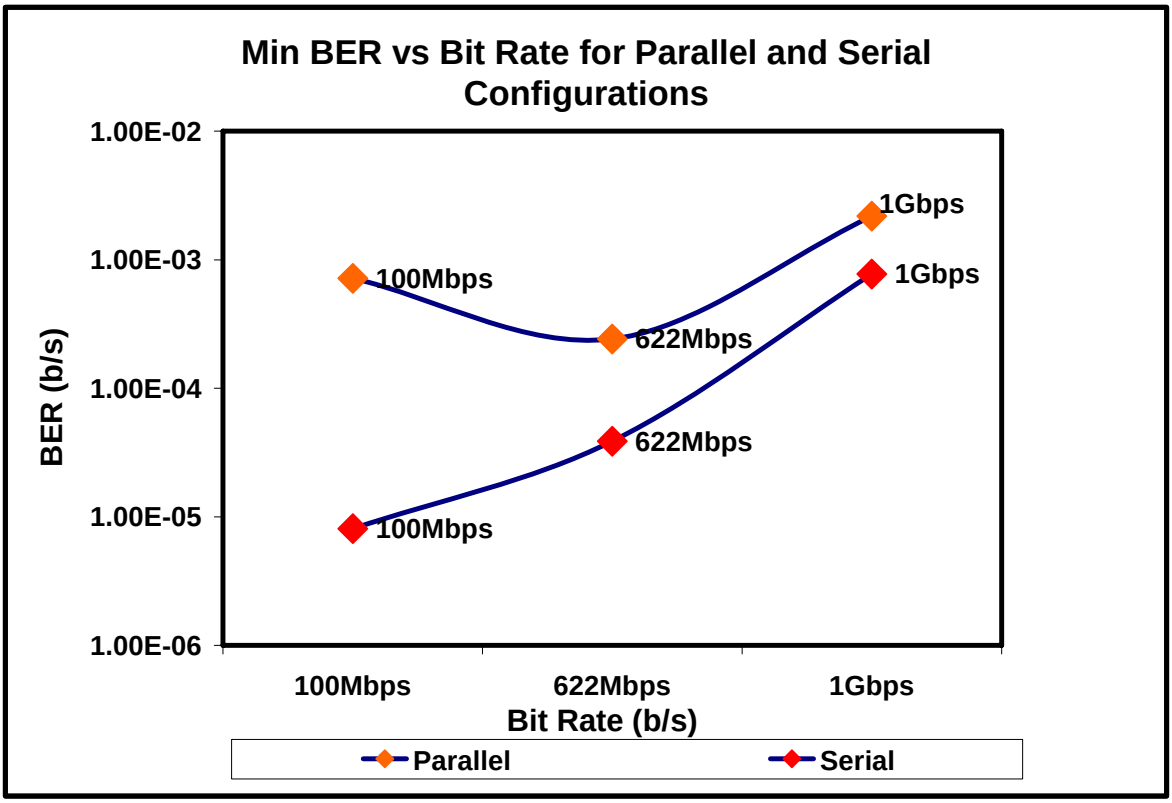

Figure 4.14: Comparison between parallel and serial configuration of BER versus Bit Rate for OCDMA System

4.3.3 Eye Diagram

The eye diagram is a useful tool for the qualitative analysis of signal used in digital transmission. It provides at-a-glance evaluation of system performance and can offer insight into the nature of channel imperfections. Careful analysis of this visual display can give the user a first-order approximation of signal-to-noise, clock timing jitter and skew. The eye diagram is an oscilloscope display of a digital signal, repetitively sampled to get a good representation of its behavior. In a radio system, the point of measurement may be prior to the modulator in a transmitter, or following the demodulator in a receiver, depending on which portion of the system requires examination. The eye diagram can also be used to examine signal integrity in a purely digital system such as fiber optic transmission, network cables or on a circuit board. Figures below show the eye diagram for the simulation design consists of parallel and serial configuration that is undistorted, and another that includes noise and timing errors.

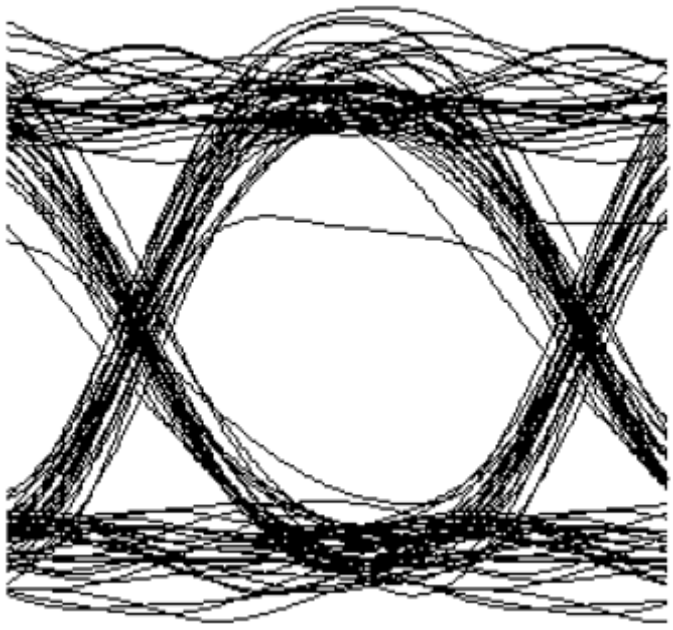

Figure 4.15: Example of Eye Diagram