CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This section discussed the result from the I-V curve and analyses the effect of MOS transistor scaling on threshold voltage, V_T, subthreshold swing, St, saturation drain current, I_{Dsat} and off current, I_{off}. These device parameters give the high impact to the device performance as it has been scaling for the requirement of speed and density in integrated circuit technology.

4.2 Threshold voltage, V_T

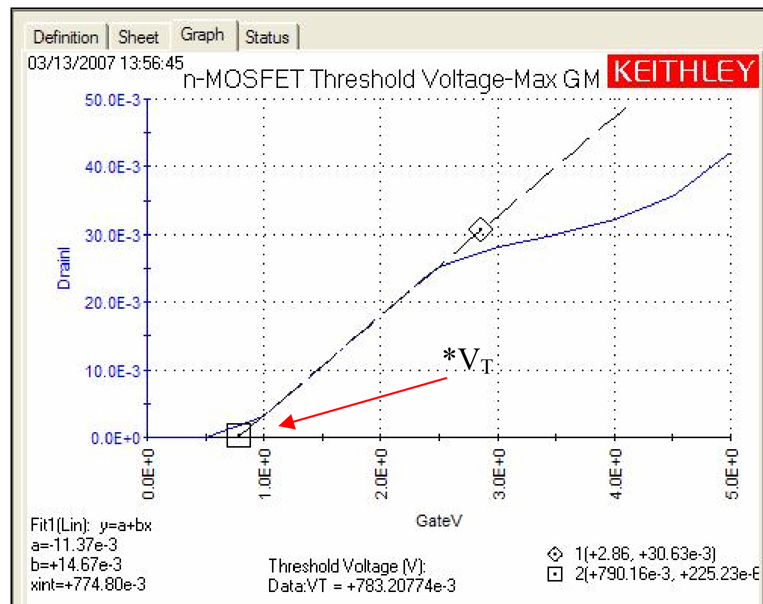

Figure 4.0: I_D versus V_{GS} for NMOS W20/L0.35µm

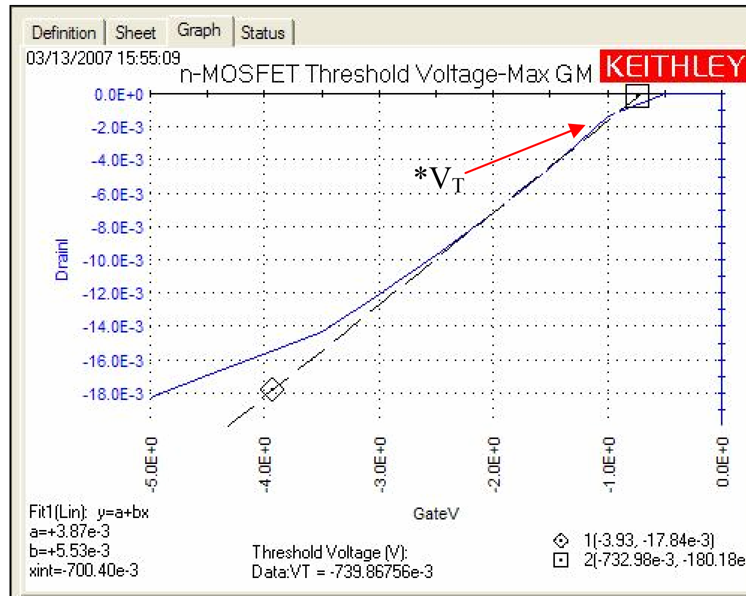

Figure 4.1: I_D versus V_{GS} for PMOS W20/L0.35µm

* The threshold voltage is indicated by the intercept of the straight line with the voltage axis as indicated in **Figure 4.0** for NMOS and **Figure 4.1** for PMOS transistor.

4.2.1 Result and data of V_T

Table 4.0: Data of V_T for NMOS and PMOS transistor

Gate length (Lg)	NMOS (V)	PMOS (V)
0.3µm	0.701	0.689
0.35µm	0.751	0.713
0.4µm	0.761	0.716
0.45µm	0.764	0.717
0.5µm	0.771	0.718
10µm	0.775	0.718

4.2.2 Graph plot of V_T for NMOS & PMOS

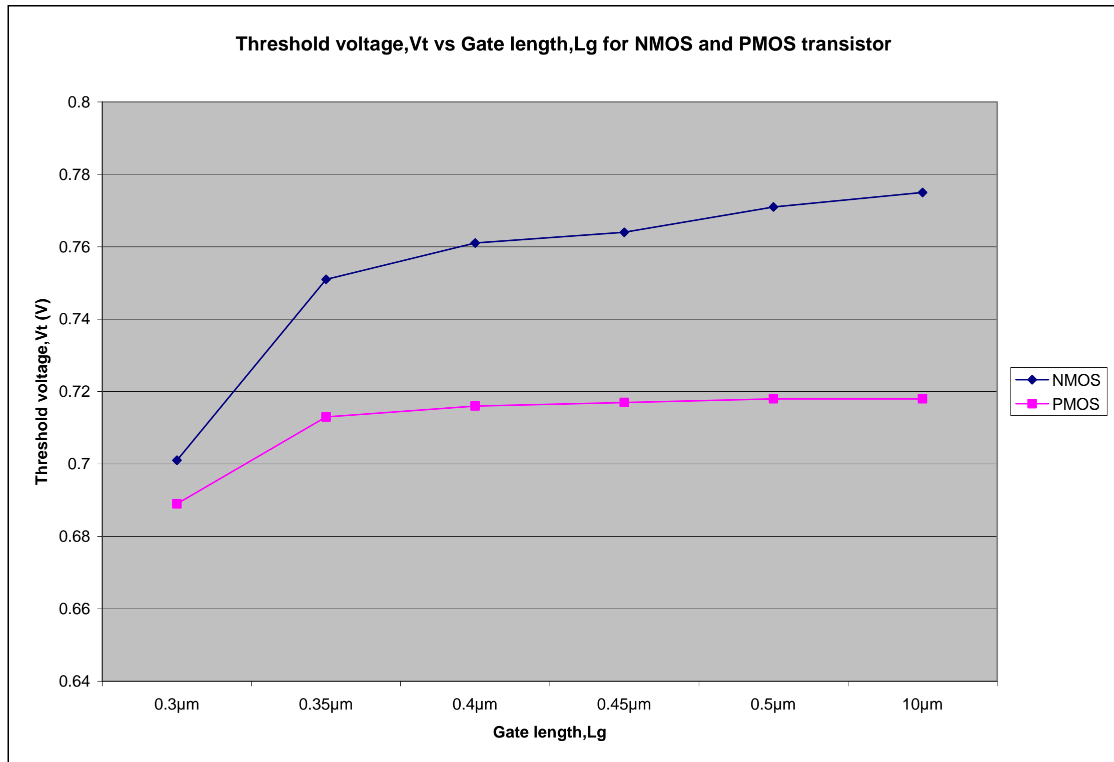

Figure 4.2: Graph shows the V_T vs. Lg for NMOS and PMOS transistor

One of the most important parameters of a MOSFET is the gate voltage at the onset of strong inversion. This parameter is known as the threshold voltage, V_T. Based on the **Table 4.0**, it shows that the value of the V_T for every dimension of gate length is comprises of the theoretical V_T value which is 0.7 ± 1 V. So, the transistor can be assumed that it was functions properly when the V_{GS} was applied to the gate. Experimentally, it is observed that as the dimensions of the gate are reduced, the threshold voltage of MOSFETs become less well predicted by the long channel V_T. It is because one of the long channels MOSFET behavior is the threshold voltage V_T is independent of gate length, Lg. The error becomes significant as the gate length dimension, Lg is reduced to less than 0.50µm.In short channel MOSFET, V_T decreases as Lg is reduced and it was shown as in **Figure 4.2** above. Obviously we can see that the V_T started to roll-down when it

approach to the Lg = 0.35μm.So, we can assume that when Lg=0.35μm, the short channel MOSFET behavior had been occurred.

The decrease of V_T with Lg in short channel devices is crucial because enhancement mode FETs are generally designed to operate with V_T magnitudes of 0.6-0.8V. If the magnitude of V_T drops even slightly below its designed value, the device may exhibit excessive drain leakage current when V_{GS} = 0V. Thus, as the device length is reduced, the measured value of V_T of n-channel enhancement mode devices becomes less positive while for p-channel devices, V_T becomes less negative. It is assumed that the space charge under the gate is a function of only the vertical electric field, ε_x. If the channel length is long, this is a reasonable assumption, as the influence of the drain and source junctions on the quantity of charge in the channel can be neglected. However, as the channel length approaches the dimensions of the widths of the depletion regions of the source and drain junctions, these depletion regions become a greater part of the channel depletion region. Thus, some of the channel depletion region charge is actually linked to the charge in the depletion region within the source and drain structures, rather than being linked to the gate charge. Hence, some of the channel region is partially depleted without any influence of the gate voltage. Since, some of the channel is depleted without the need to apply a gate bias, and less gate charge is required to invert the channel in short channel devices than in a long channel device with comparable doping. The V_T values of 0.6-0.8V in long channel MOSFET devices with lightly doped substrates can only achieved by increasing the doping concentration at the surface of the channel, with V_T adjust implant. If short channel effects reduce V_T below the long channel values, higher channel doping concentration must be increased even more to re-establish the desired V_T. Conventional bulk MOSFETs require channel doping approaching or exceeding 10^{18} cm^{-3} in order to limit short-channel effects (SCEs).Such high doping concentrations are likely to cause severe performance degradations due to impurity scattering, off current and reduced carrier mobility in the high transverse field [20].

An increase of the threshold voltage as the channel or gate length narrows, in contrast with a decrease of the threshold voltage when the channel shortens [21].The short channel effect becomes important when the channel length is comparable or smaller than the thickness of the depletion layer and the gate oxide. Channel width will denote the width of the inversion layer or conduction channel and it will vary with applied dc gate voltage. Gate oxide thickness must be approximately linearly scaled with channel length to maintain the same amount of gate control over the channel to ensure good short channel behavior.

The device with the thinner oxide has a smaller channel depletion layer and hence improved short channel characteristics. The improved short channel effects can be taken advantage of by targeting a smaller channel length. Channel depletion layer is engineered to become as smaller as the gate oxide thickness as decreased. In addition, short channel behavior is governed by the ratio of channel depletion layer thickness to channel length. The channel depletion layer is inversely proportional to the square root of the channel doping concentration. During device optimization, channel doping is increased as the oxide is scaled to maintain approximately the same device threshold voltage. Thus, for continued MOS channel length scaling, the gate dielectric thickness must continue to be scaled.

4.3 Saturation drain current, I_{Dsat}

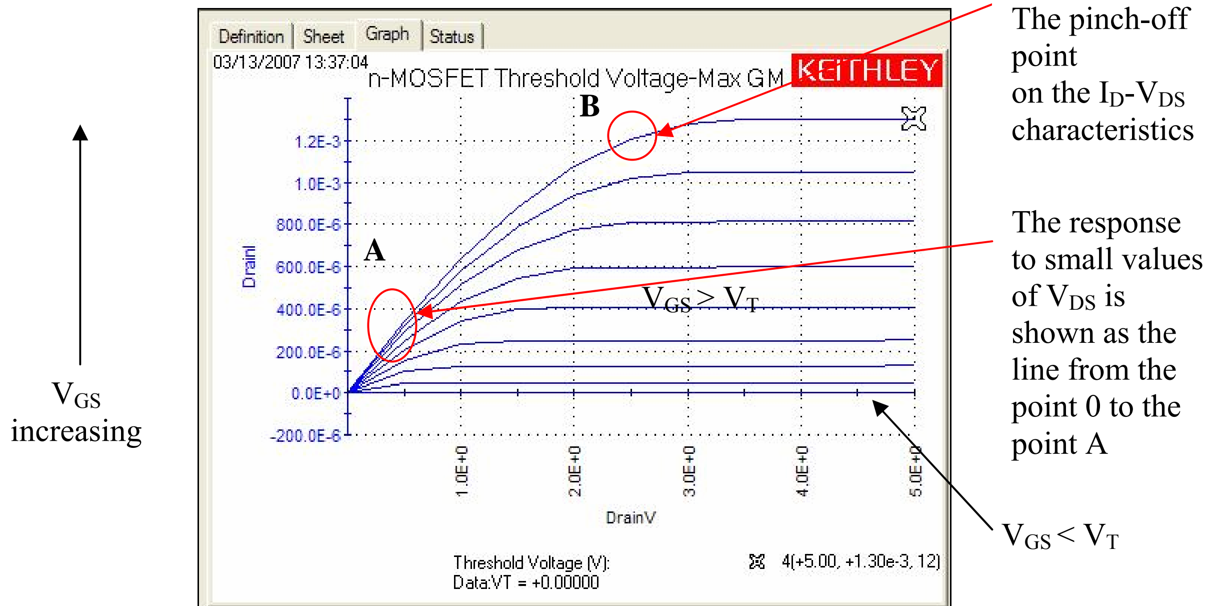

Figure 4.3: I_D versus V_{DS} for NMOS W20/L10µm

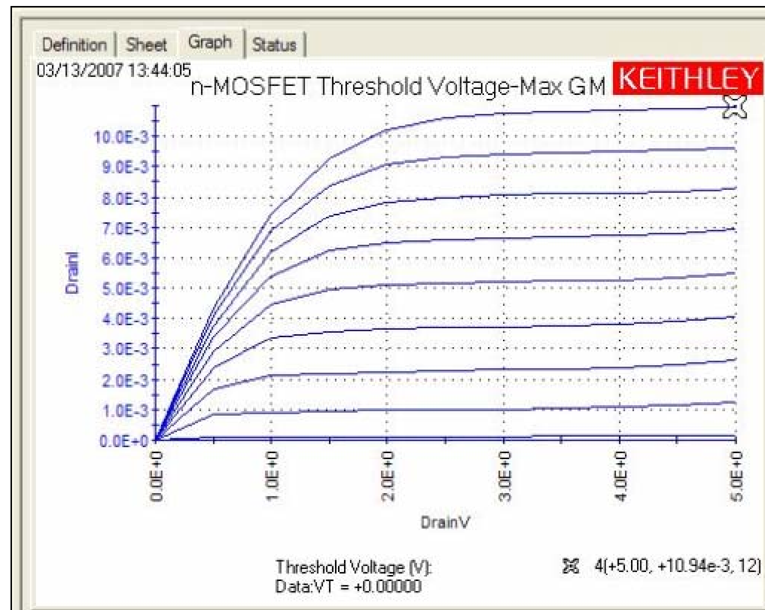

Figure 4.4: I_D versus V_{DS} for NMOS W20/L0.50µm

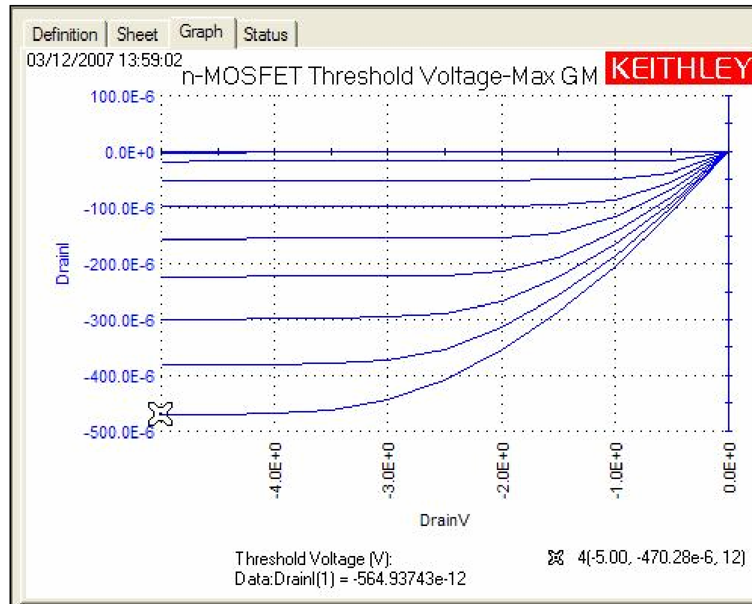

Figure 4.5: I_D versus V_{DS} for PMOS W20/L10µm

Now, we consider the operation of I_D versus V_{DS} as shown in **Figure 4.3** for NMOS W20/L10µm and **Figure 4.4** for NMOS W20/L0.50µm.Both of this figure was differentiate by the different gate length. At first, we assume that V_{GS} kept fixed at single value while V_{DS} is varied, and V_{BS} = 0V.Sufficient gate bias is applied to ensure that the MOSFET is being operated in inversion ($V_{GS} > V_T$).When V_{DS} is increased slightly, I_D starts to flow. When V_{DS} is small, a few tenths of a volt or less, the surface channel behaves like a simple resistor. That is, an I_D proportional to V_{DS} flows into the drain. The V_{DS} is increased beyond a few tenths of a volt, the MOSFET exhibits a new phase of behavior. That is, current flowing in the channel gives rise to a significant voltage drop in the channel. Specifically, the channel voltage is drain-bulk voltage, V_{DB} at the drain end and source-bulk voltage V_{SB} at the source end. If V_{SB} = 0V, the channel voltage at the drain end will not be zero, since we assume V_{DS} > 0V.

A non-zero V_{DB} causes the depletion region under the gate to widen toward the drain end of the channel. This implies that the mobile charge concentration in the inversion layer simultaneously decreases. The smaller number of carriers causes the channel conductance to decrease, which in turn is manifested as a smaller slope

in the I_D-V_{DS} characteristics as V_{DS} is increased. As the drain voltage is further increased, the depletion region continues to widen and the slope of the I-V characteristics continues to decrease. Since the gate voltage is constant across the entire gated region, less voltage is available near the drain to establish the inversion layer charge. Hence, inversion is less strong in the channel near the drain.

Eventually, if V_{DS} is sufficiently increased such that $V_{DS} > (V_{GS}-V_T)$, the inversion layer ceases to exist near the vicinity of the drain. The disappearance of the inversion layer due to an increase in V_{DS} is termed pinch-off as shown in point B at **Figure 4.3**.We see that the slope of the I_D curves here has become approximately zero. However, that pinch off does not mean that I_D vanishes as V_{DS} exceeds the pinch off voltage. In fact, it is the gradual channel approximation that is no longer valid in the region of the device in which pinch off exists. That is, mobile charges still move through the depleted region near the drain and drain current continues to flow. For voltages greater than V_{DSsat} the current stream of the carriers moving into the pinched off region is no longer confined to the inversion layer region near the surface, but begins to move away from the surface and into the bulk. Once V_{DS} becomes larger than $(V_{GS}-V_T)$ the polarity of the vertical electric field in the pinched off region is reversed. This tends to push any mobile carriers flowing in the channel away from the surface. Thus, in the region of the channel where $V_{DS} > (V_{GS}-V_T)$, the mobile carriers flow toward the drain beneath the surface.

For each value of $V_{GS} > V_T$, a characteristics of the form shown in **Figure 4.3** and **Figure 4.4** had been observed. Since the conductance of the channel will increase as V_{GS} is made larger, the initial slope of I_D will also become stepper with increasing V_{GS}. Furthermore, since the inversion layer contains more electrons, a larger value of V_{DS} is needed to produce pinch-off in which V_{DSsa}t increase for increasing V_{GS} .For $V_{GS} < V_T$, no channel exists and $I_D = 0$ for all drain biases below junction breakdown.

4.3.1 Result and Data of I_{Dsat}

Table 4.1: Data of I_{Dsat} for NMOS and PMOS transistor

Gate length, Lg	NMOS (mA)	PMOS (mA)
0.3µm	1.41E-02	1.29E-02
0.35µm	1.43E-02	1.28E-02
0.4µm	1.30E-02	1.06E-02
0.45µm	1.20E-02	9.32E-03
0.5µm	1.09E-02	8.44E-03
10µm	1.30E-03	4.70E-04

4.3.2 Graph plot of I_{Dsat} for NMOS & PMOS

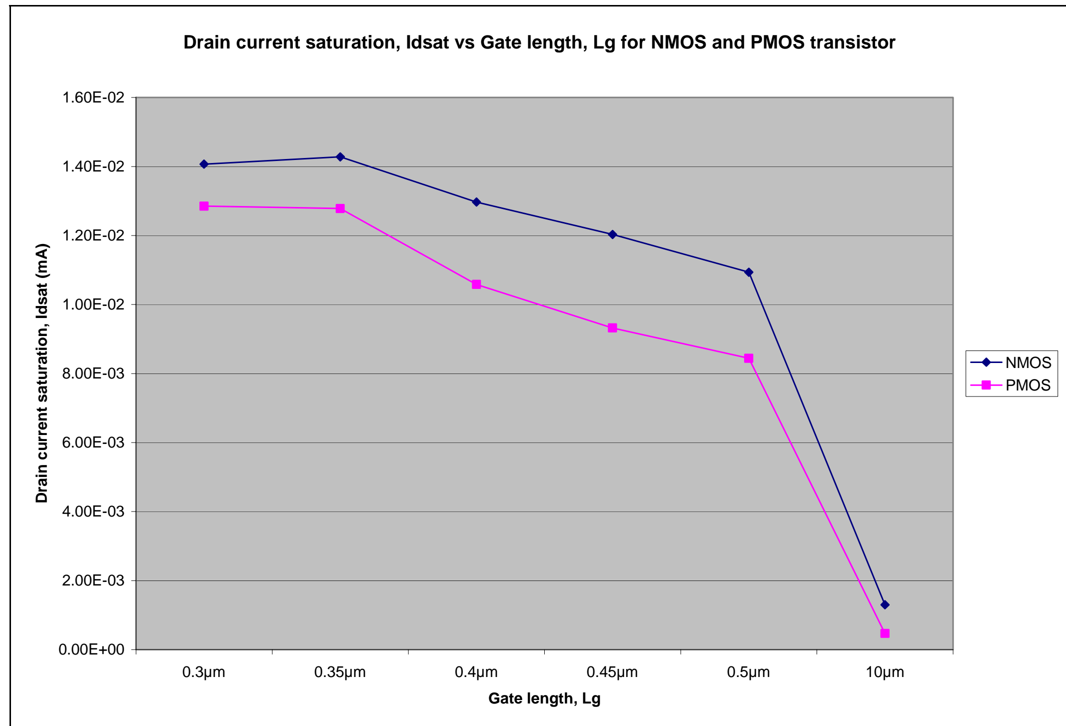

Figure 4.6: Graph shows the I_{Dsat} vs Lg for NMOS and PMOS transistor

To increase the speed of digital ICs, the MOSFET saturation drain current I_{Dsat} must be increased which is to allow faster charging and discharging of parasitic capacitance. From the long channel MOSFET, a decrease in either the channel length Lg or gate oxide thickness t_{ox} will lead to an increase in $I_{Dsat.}$ From the

perspective of the MOSFET as a circuit component, the characteristics of long channel MOSFET for the drain current in saturation I_{Dsat} is independent of V_{DS}. This characteristic has been shown for the Lg = 0.10µm to Lg = 0.50µm in **Figure 4.6.** However as process technology improved to the point where devices could be fabricated with gate lengths smaller than ~2µm, it turned out that MOSFET began to exhibit phenomena not predicted by the long channel MOSFET. As shown in **Figure 4.6**, Lg =0.5µm and below is more prone to approach the short channel MOSFET behavior which is I_{Dsat} increases as V_{DS} increases. One of the more surprising of such short-channel effects which becomes especially pronounced as Lg decreases below 0.50µm is that the drain current in saturation I_{Dsat}, shows far less increase as Lg is decreased than is predicted by the long channel model [22].I_{Dsat} start to increase as it reached 0.10µm.Then it continuously slightly increases as the Lg decrease from 0.50µm until 0.35µm.I_{Dsat} is roll-up as it reached Lg = 0.35µm to 0.30µm, thus it is shows the occurrence of the short channel MOSFET behavior at this portion of gate length.

I_{Dsat} is predicted to become independent of Lg in extremely small MOSFETs. I_{Dsat} will increase more rapidly as Lg is decreased if the MOSFET has a thinner gate oxide. This benefit provides even a greater impetus for making t_{ox} as thin as possible as gate lengths are decreased further in the drive for higher density. Since the quest for higher density still requires Lg to be further reduced, it will nevertheless be necessary to confront the short channel effects.

The drain current decrease more when gate length is 10µm.It is because, the source and drain terminals of the MOSFET allow bias V_{DS} to be applied across the ends of the channel region, giving rise to a drain current, $I_{D.}$ For drain voltages in excess of the pinch off voltage (V_{DSsat}) the gate to drain voltage drops below the voltage value needed to establish an inversion layer, it becomes smaller than the threshold voltage. Hence, long channel MOSFET theory implies that the inversion layer no longer exists in this case, and that there are no longer any mobile carriers present in the channel at such locations.

The values of I_{Dst} can be well predicted in long channel MOSFETs by modifying the basic MOS model to take into account the fact that the minority carrier concentration at the Si surface is greater than the value at equilibrium, but still less than the bulk doping concentration. The results is indicate that the magnitude of I_{Dst} is essentially independent of V_{DS} but is exponentially proportional to V_{GS}. Typically, to ensure that I_{Dst} will be negligible small, the bias applied to the gate should be 0.5V below V_T.

4.4 Subthreshold swing, St

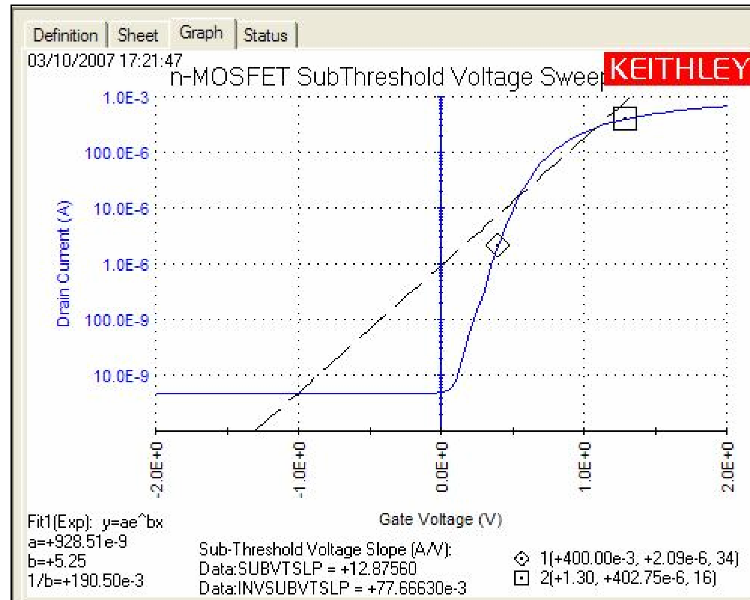

Figure 4.7: I_D versus V_{GS} for NMOS W20/L0.45μm

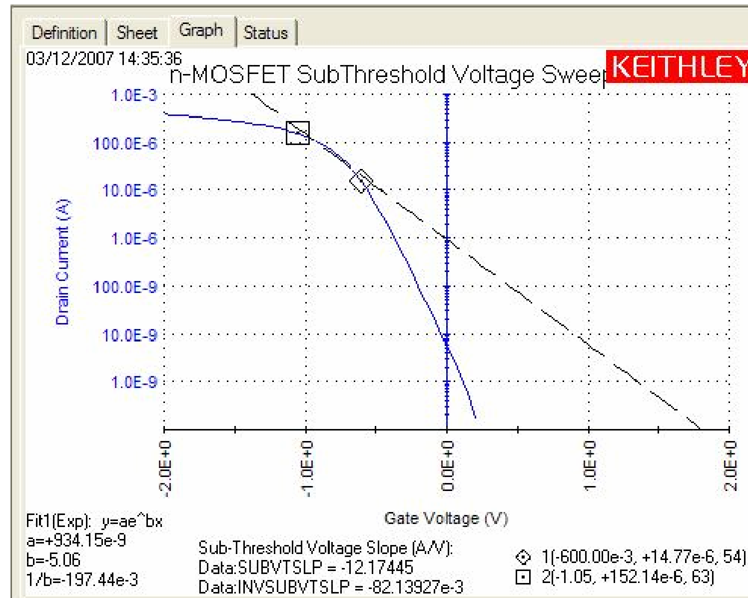

Figure 4.8: I_D versus V_{GS} for PMOS W20/L0.35µm

In a field-effect transistor, the minimum voltage swing needed to turn a transistor from on to off is an important figure of merit which ultimately determines how low in power the device technology can be. This characteristic is usually quantified by measuring how many milivolts it takes to change the drain current by one order of magnitude, i.e. one decade of current on a logarithmic scale. The measure of this characteristic is called the subthreshold slope and is given in units of mV/decade of current change.In the MOSFET, the subthreshold swing is limited by thermal voltage, kT/q, which is 60mV/decade at room temperature

The **Figure 4.7** and **Figure 4.8** above show the variation of I_D with V_{DS} for NMOS and PMOS transistor. At first, we assume that V_{GS} kept fixed at single value while V_{DS} is varied, and V_{BS} = 0V.Sufficient drain bias, V_{DS} = 0.1V is applied to ensure that the MOSFET is being operated. The St value of typical submicron nMOSFETs operating at 300K is ~100mV/decade, and in such devices I_D will drop from 1µA to 1pA for a 0.6V decrease in V_{GS}. Thus, if a MOSFET exhibits a constant-current V_T of 0.6V (i.e., I_D=1µA/µm when V_{GS} = V_T= 0.6V), when V_{GS} = 0V, I_D will be reduced to 1pA/µm. Ideally, an abrupt change in I_D should occur as V_{GS} passes through V_T. If a MOSFET exhibits a steep decline in I_D as V_{GS} below V_T, its St value be small.

4.4.1 Result and Data of St

Table 4.2: Data of St for NMOS and PMOS transistor

Gate length,Lg	NMOS (mV/dec)	PMOS (mV/dec)
0.3µm	98.712	82.139
0.35µm	83.235	79.911
0.4µm	78.218	78.822
0.45µm	77.666	78.533
0.5µm	77.589	78.351
10µm	77.488	78.212

4.4.2 Graph plot of St for NMOS & PMOS

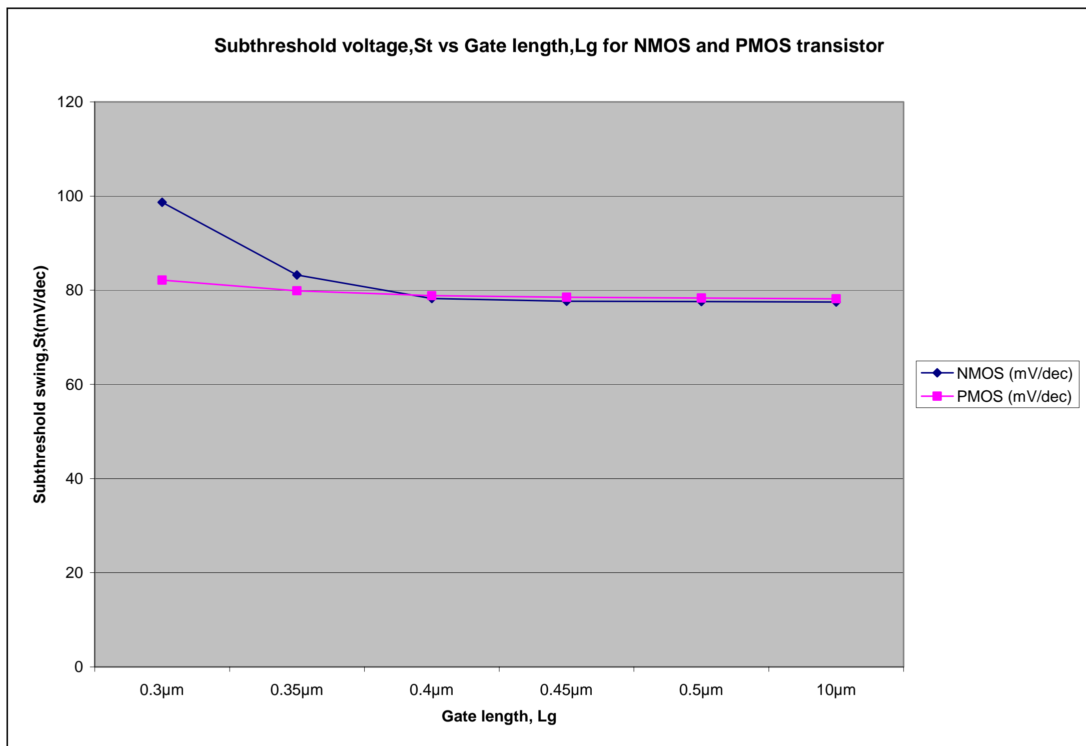

Figure 4.9: Graph shows the St vs. Lg between NMOS and PMOS transistor

According to the **Figure 4.9**, the St value for NMOS is more prone to roll-up compared to the PMOS transistor. This is because at off mode, electron which is the majority carrier in NMOS has two times mobility acceleration compared to holes, which is the majority carrier in PMOS transistor. The St was roll-up as it reached the Lg = 0.4µm. Note that when the channel length gets small, the values of I_{Dst} are

larger. This is due to so-called short channel effects, as a result of the gate inability to control the electrostatic potential and free carrier distribution within the device channel. As a consequence, degradation is seen in the subthreshold characteristics, and a related dependence of threshold voltage on channel length arises due to drain-induced barrier lowering and punch-through between the source and drain junctions. As a result, measurements of St versus channel length are used to detect the onset of these short channel effects which are punchthrough and surface drain-induced barrier lowering.

Devices with gate lengths of ~2μm are at the transition between long-channel and short channel devices behavior. In long channel MOSFETs, I_{Dst} will exponentially increase with V_{GS} but will remain substantially independent of V_{DS}. That is, when V_{DS} is sufficiently increased in MOSFETs with $L \leq 2\mu m$, the source and drain depletion regions merge, and that point I_{Dst} starts to become dependent on V_{DS}.In short channels MOSFETs, however, if V_{GS} is fixed while V_{DS} is increased, larger value of I_{Dst} values than are predicted by the long channel are observed. This larger subthreshold current is due in part to increased I_{Dst} flowing at the surface as a result of surface-drain-induced barrier lowering (DIBL).If only surface DIBL is occurring in a MOSFET, St values are observed to remain unchanged as shown when the Lg is decrease from 10μm to 0.4μm.However, another short-channel effect known as subsurface punchthrough can also give rise to an increase in I_{Dst}. One manifestation of this effect is an increase in the measured value of St as Lg is decrease from 0.4μm to 0.30μm.That is, the gate has less control of the subsurface punchthrough current than it has over the surface subthreshold current. Thus, once a MOSFET enters subsurface punchthrough and such current starts to flow, the St value of the MOSFET becomes larger than if only normal subthreshold current is flowing. We can minimize the depletion depth of retrograde channel doping MOSFETs by judicious selection of the channel and the substrate doping densities and the thickness of the lightly doped layer for a given threshold voltage.

A small value of St is desirable, since it indicates maximum control over the gate over the channel current. Typical values of subthreshold swing in long channel MOSFET are around 90mV/decade. Such values can be achieved by building devices that have a low value of substrate doping concentration, which gives a larger depletion width and a thin gate oxide.

The key factor that leads to reduced short channel effects in St is the amount of gate control on the channel charge [23].Therefore to ensure the minimum short channel effects; the devices must be design to maximize gate control. This can be achieved by minimizing the channel depletion depth, gate oxide thickness, junction depth and reducing the supply and the substrate voltages [24].Although reduced depletion width leads to increased subthreshold swing of the device, it will be shown that this is an acceptable increase given the performance advantages of smaller channel length devices. At the maximum operating V_{DS} value the punchthrough current should be kept smaller than the long channel I_{Dst} value. One simple rule of thumb to accomplish this in a MOSFET that employs a V_T adjust implant is to set the substrate doping concentration. It should also be noted that the V_T adjust implant generally increases the subthreshold swing, St and this is one reason that St in real devices is larger (~100mV/dec).

4.5 Off current, I_{off}

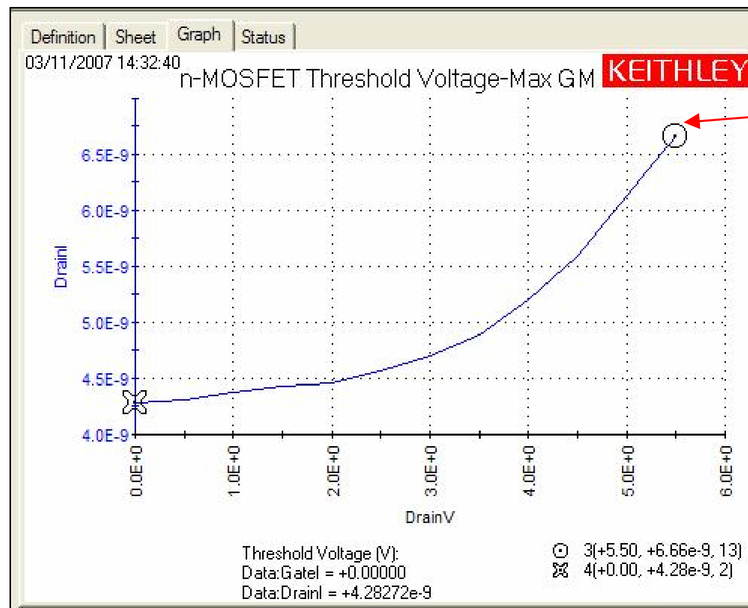

Figure 4.10: I_D versus V_{DS} for NMOS W20/L10µm

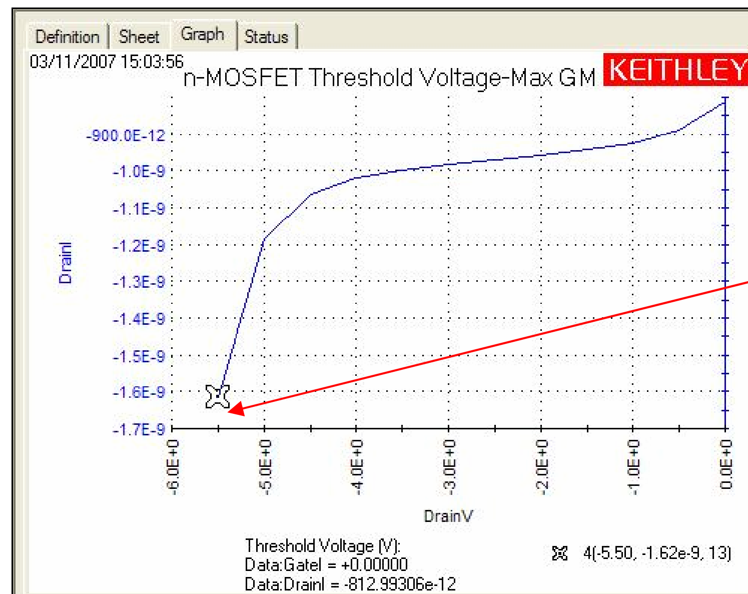

Figure 4.11: I_D versus V_{DS} for PMOS W20/L10µm

4.5.1 Result and Data of I_{off}

Table 4.3: Data of I_{off} for NMOS and PMOS transistor

Gate length,Lg	NMOS (pA/µm)	PMOS (pA/µm)
0.3µm	7.40E-07	8.99E-03
0.35µm	8.51E-08	9.22E-04
0.4µm	6.57E-09	2.60E-05
0.45µm	6.92E-09	1.67E-07
0.5µm	6.77E-09	6.43E-09
10µm	6.66E-09	1.62E-09

4.5.2 Graph plot of I_{off} for NMOS & PMOS

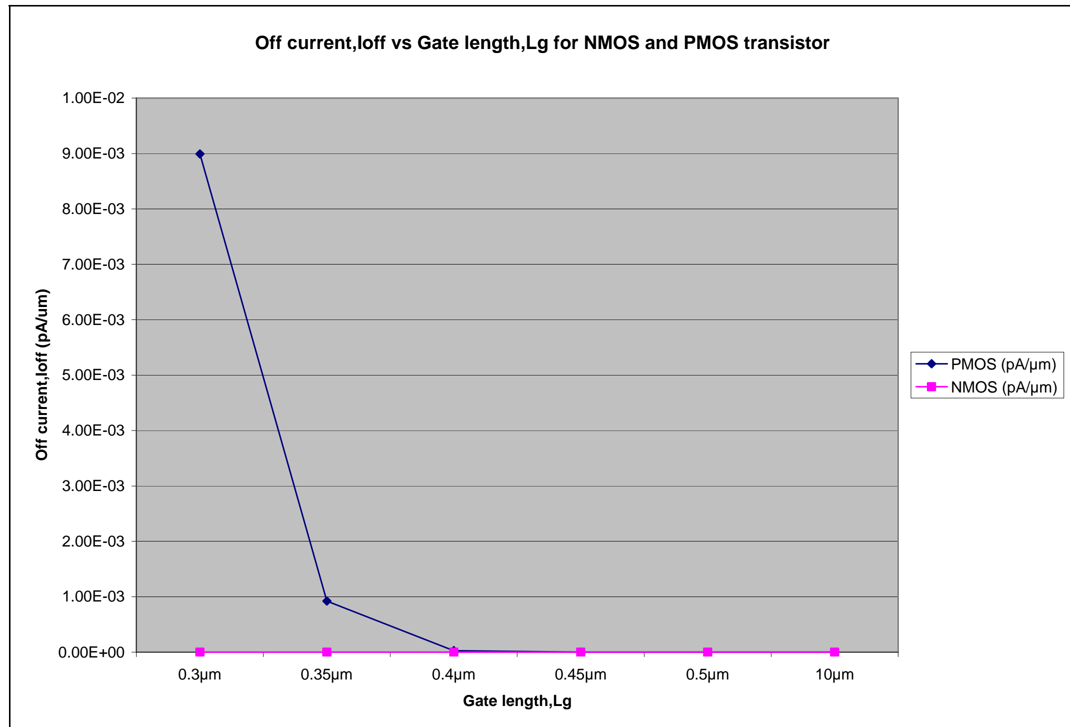

Figure 4.12: Graph shows the I_{off} vs. Lg for NMOS and PMOS transistor

Based on the **Figure 4.12**, it shows that the I_{off} value for NMOS is nearly zero while for the PMOS the I_{off} roll-up when Lg = 0.35µm. I_{off} (I_{DS} at V_{GS} = 0 and V_{DS} = V_{DD}) is one of the most important device characteristics directly related to short channel effect. The standby power of a chip is determined by the combined I_{off} of all the transistors and as such it must be minimized to integrate millions of

transistors together. I_{off} should be optimized and it is mainly due to diffusion current, increases with decreasing feature sizes. I_{off} is one of the critical parameters that determine the scalability of the technology.

Scaling approach employing a more flexible criterion for acceptable "off"state behavior has been recently proposed. The crux of the procedure involves finding a channel doping profile which yields an acceptable combination of off-current, I_{off} in a device with as small an Lg as possible. Conventional lithography typically introduces a 10-20% variation in Lg. Device design should be optimized by using halo doping so that I_{off} do not vary significantly with this undesirable fluctuation in the gate length. The fluctuation of transistor characteristics on the same chip forces the circuit design to become conservative to allow enough margin such that the circuit can operate even with the worst case I_{off} (shortest Lg) and the worst case (longest Lg).The profile is initially determined assuming that the device exhibits long channel behavior. No significant punchthrough should be observed in the subthreshold operating region. However, the acceptable value of "off " current in the long channel device is deliberately picked to be smaller than I_{off} in the short channel device being designed, in anticipation of the increase in I_{off} due to surface-DIBL in the shrunken device.

Gate oxide thickness and junction scaling has enabled channel length scaling by improving short channel characteristics for I_{off}. The technique to improve short channel characteristics is well engineering. By changing the doping profile in the channel region, the distribution of the electric field and potential contours can be changed. The goal is to optimize the channel profile to minimize the off-state leakage while maximizing the linear and saturated drive currents. Super Steep Retrograde Wells (SSRW) and halo implants have been used as a means to scale the channel length and increase the transistor drive current without causing an increase in the off-state leakage current [25].

The barrier lowering analysis examines the effect of shrinking Lg to the minimum value that can be fabricated with the best lithographic process at hand. If I_{off} is less than or equal to the target value, the device with that value of Lg will succeed in meeting the circuit requirements and is deemed nominally manufacturability. If I_{off} is too high, either the channel length will need to be increased, or a larger value of Ioff will need to be accommodated by changing the circuit design.

The term nominally manufacturability is used, because as the channel length is reduced, the sensitivity of V_T to channel length variations increases. As already noted, the impact of channel length variation is to require a more conservatives setting if nominal I_{off} so that the devices with smaller than nominal V_T values will still have acceptable off currents. As the channel length is reduced, at some points this lowered I_{off} estimate will encounter the same punchthrough limit already discussed. If channel length is under very tight control, then V_T variations from length variation remains small and only variation due to changes in V_{DS} will matter.