

CHAPTER 5

CONCLUSION

5.1 Summary

As previously stated, the main objective of this project is to investigate the effect of MOS transistor scaling on the critical device parameters. The parameter under studies are threshold voltage, on and off state leakage current and short channel effect on sub-threshold characteristics.

The results showed that the gate length gives the most influential effect on those parameters. It is also clearly demonstrated that, MOSFETs with gate lengths below than $0.5\mu\text{m}$, have various operational problems. Based on the discussion in Chapter 4, V_T decreases with the reduction in channel length or V_T roll-down as it approached the L_g of $0.35\mu\text{m}$ and this will leads to the increment in drain bias or the so called Drain Induced Barrier Lowering (DIBL) effect. On the other hand, the $I_{D\text{sat}}$ is roll-up as it reached the L_g of $0.35\mu\text{m}$ to $0.30\mu\text{m}$. Collectively, threshold voltage roll-down and subthreshold swing roll-up are commonly known as the short-channel effects (SCEs). The S_t was roll-up as it reached the L_g of $0.4\mu\text{m}$. When the channel length gets smaller, the values of $I_{D\text{st}}$ becomes larger, and this effect is believed to be the result of the gate inability to control the electrostatic potential and free carrier distribution within the device channel [26]. Lastly, the I_{off} is shown to roll-up when L_g approached $0.35\mu\text{m}$. I_{off} should be optimized and it is mainly due to diffusion current, which increases with decreasing feature sizes. As a conclusion, the study proved that producing MOSFET with channel lengths much smaller

than a micrometer is a challenge due to the short channel effect occurrence. Some of the research of scaling the MOSFET is still under study to overcome the short channel effect. The explanations of the research as depicted in Appendix B.

Albeit with all the demonstrated negative effects, smaller MOSFETs are still desirable for several reasons. First smaller MOSFETs may allow more current to pass, due to their shorter length dimension: conceptually, MOSFETs are like resistors in the on-state, and shorter resistors have less resistance; however, they may also have smaller widths, leading to proportionally higher resistance, so the real issue is whether the ohms per square is reduced. Second smaller MOSFETs have smaller gate areas, and thus lower gate capacitance. Scaled MOSFETs also have thinner gate dielectric, which reduces the on-state ohms per square but makes the gate capacitance per unit area higher; nevertheless, these effects still both go in the right direction. These first two factors contribute to lower switching times, and thus higher processing speeds, and lower energy per switching event. A third reason for MOSFET scaling is reduced area, leading to reduced cost. Smaller MOSFETs can be packed more densely, resulting in either smaller chips or chips with more computing power in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip.

5.2 Recommendation for future project

Due to the constraint in both time and related equipment, the project could not be implemented as planned. The cleanroom can provide the best equipment for the fabrication process, but the device fabrication could not be executed without a considerable mask making facility, especially for the nano-scale design. Further investigation could be extended to evaluate the result from the fabrication process so that a comparison between the fabrication result and other established sources where similar work can be done. This study could be more profoundly implemented if the sample is fabricated internally, so that

the effect from the fabrication process parameters can easily be correlated to the device problems encountered. In addition, the effect of the channel width could also be investigated, since it is widely believed that this factor has a nontrivial impact on the critical device parameters.