THE STUDY OF THE EFFECT OF MOS TRANSISTOR SCALING ON THE CRITICAL DEVICE PARAMETERS

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THE STUDY OF THE EFFECT OF MOS TRANSISTOR SCALING ON THE CRITICAL DEVICE PARAMETERS

by

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APPROVAL AND DECLARATION SHEET

This project report titled The Study of the Effect of MOS Transistor Scaling on the Critical Device Parameters was prepared and submitted by Zazurina Abd Rahman (Matrix Number: 031010540) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Microelectronic Engineering) in Universiti Malaysia Perlis (UniMAP).

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KAJIAN KESAN PENSKALAAN TRANSISTOR MOS TERHADAP PARAMETER KRITIKAL PERANTI

ABSTRAK

Sejak rekaan transistor kira-kira 30 tahun dahulu,peranti CMOS telah diskala rendahkan secara agresif dalam setiap generasi teknologi untuk mencapai kepadatan dan prestasi integrasi yang tinggi. Penyusutan peranti membenarkan litar menjadi padat, lebih banyak fungsi per ruang, rekabentuk integrasi yang lebih rumit, berkelajuan tinggi, bekalan voltan rendah, yang mana berkisar tentang teknologi informasi dan komunikasi. Laporan ini menerangkan satu penyelidikan tentang kajian kesan penskalaan transistor MOS terhadap parameter kritikal peranti. Parameter peranti yang dikaji ialah voltan ambang, keadaan arus bocor berpanjangan dan putus, dan kesan saluran pendek pada pencirian hampir ambang, yang mana mempunyai kaitan terus kepada prestasi litar terkamir. Kajian awal mendapati antara parameter proses yang terlibat di dalam pembuatan peranti, panjang get memberi kesan kepada parameter peranti. Kajian ini menunjukkan, MOSFET dengan panjang get di bawah yang kesepuluh mikro meter, mempunyai masalah operasi. Kajian juga membuktikan bahawa, menghasilkan MOSFET dengan saluran panjang lebih kecil dari mikro meter adalah satu cabaran, dan kesukaran fabrikasi peranti semikonduktor selalunya menjadi faktor pembatas dalam memajukan teknologi litar bersepadu.

THE EFFECT OF MOS TRANSISTOR SCALING ON THE CRITICAL DEVICE PARAMETERS

ABSTRACT

Since the invention of transistors some 30 years ago, CMOS devices have been scale down aggressively in each technology generations to achieve higher integration density and performance. The device shrinkage allow denser circuits, more functions per floor space, more complicated and integrated design, higher speed, lower supply voltage, which revolutionized the information and communication (ICT) technology. This report presents an investigation into the study of the effect of MOS transistor scaling on the critical device parameters. The parameters understudy are threshold voltage, on and off state leakage current, and short channel effect on sub-threshold characteristics, that have a direct influence on the integrated circuit (ICs) performance. An initial research found that, among the process parameters involved in the manufacture of devices, gate length has the most influential effect on those parameters. This study showed, for the MOSFET with gate length below one-tenths of a micrometer, has an operational problems. The study also proved that, producing MOSFET with channel lengths much smaller than a micrometer is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology.

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LIST OF SYMBOLS, ABBREVIATIONS OR NOMENCLATURE

φ	Work function difference between the gate
κ	Kappa
ε_o	Permittivity in vacuum
q	Elementary charge
k	Boltzmann constant
T	Absolute temperature