CHAPTER 5

CONCLUSION

5.1 Summary

This final year project which is carried out through two semester needs a lot of researches on its theory and algorithm of Modified Baugh-Wooley Multiplier. Before that, researches on several high speed multipliers are done in order to select the best high speed performance among it. The speed of the multiplier is determined by both architecture and circuit. The speed can be expressed by the number of the cell delays along the critical path on the architecture level of the multiplier. The cell delay, which is normally the delay of the adder, is determined by the design of the circuit of the cell.

It is essential to understand the concepts of the product generation and partial product accumulation in order to design Modified Baugh-Wooley multiplier. Form result and discussion, it is proved that Modified Baugh–Wooley multiplier that has been designed in this project is functioning correctly. In this project, several approaches have been applied to speed up multiplication: reduce the number of the partial products, accelerate the accumulation and pipelining. There are two methods used in this Modified Baugh-Wooley multiplier to reduce the time needed to accelerate the accumulation. First is using Half Adder instead of Full Adder and use faster adder which is Carry Save Adder. Pipelining approach applied to Modified Baugh-Wooley multiplier has not been able to produce the expected result yet. . Pipelining approach applied to Modified Baugh-Wooley Two's Complement Signed Multiplier has not been able to produce the expected result yet, might be due to improper of placing pipeline register (D Flip-flop) in the schematic. This is because, some of the D Flip-flops must even be placed in data paths in which no work has been done.

From result and discussion, the performance of Modified Baugh-Wooley Two's Complement Signed Multiplier can be summarized as below in Table 5.1.

Performance	**Modified Baugh-Wooley Two's Complement Signed Multiplier**
Functional	✓
Speed	20.33MHz

Table 5.1 : Performance of Modified Baugh-Wooley Two's Complement Signed Mutiplier

5.2 Recommendation for Future Project

Hopefully, for the future project, pipelining approach to this Modified Baugh-Wooley Two's Complement Signed Multiplier can be design successfully and produce the expected result. Pipelining can be used to speed up the processing of the data in the circuit by partition it into segments. It is essential to ensure correct timing because some pipeline registers must even be placed in data paths in which no work has been done. This is the biggest challenge to apply pipelining because any misplace of pipeline register, would not produce correct output for multiplier. Pipelining approach applied to Modified Baugh-Wooley Two's Complement Signed Multiplier has not been able to produce the expected result yet, might be due to improper of placing pipeline register (D Flip-flop) in the schematic. This is because, some of the D Flip-flops must even be placed in data paths in which no work has been done. More study and research on that matter has to be done in order to make it successful.