CHAPTER 3

EXPERIMENTAL SETUP

In this project, the experimental setup comprised of both hardware and software. Hardware components comprised of Altera Education Kit, capacitor and speaker. While software used in this project is Quartus II (Figure 3.0).

3.1 Software

3.1.1 Design Flow for Using Quartus II Graphical User Interface [5]



Figure 3.0: Quartus II Software [5].

The following steps describe the basic design flow for using the Quartus II graphical user interface:

1. From the main menu, File \rightarrow New Project Wizard is selected. Refer Figure 3.1.

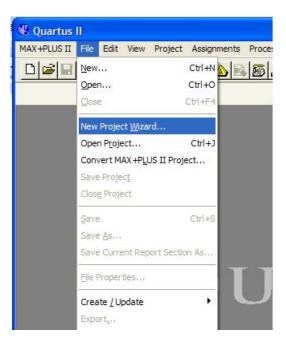


Figure 3.1: New Project Wizard popup window.

2. The New Project Wizard popup window will appear.

i) Introduction No changes done. \rightarrow Click Next.

ii) Directory, Name, Top-Level Entity [page 1 of 5]The Working Directory, Project Name and Top-Level Design appear as inFigure 3.2:

iii) Click Next (Click Yes if required to create a new directory)

	win1			- 1
D:\Altera\max\mu	SICT			
What is the name of	of this project?			
music1				
What is the name of and must exactly m			name is case s	ensitive
music1				
Use Existing Proj	ect Settings			

Figure 3.2: Directory, Name, Top-level Entity.

- 3. Add Files [page 2 of 5]
 i) No changes done. → Click Next.
- Family & Device Settings [page 3of 5]
 i) The device family is "MAX7000S" and the device type is "EPM7128S100-7"
 ii) Click Next (Figure 3.3).

amily: MAX7000S				
		<u> </u>		
Target device				
C Auto device selected b	y the Fitter from the	'Available devices' l	ist	
Specific device selecte	ed in 'Available devi	ces' list		
Available devices:		- Filters		
EPM7128SQC100-6		~		_
EPM7128SQC100-7 EPM7128SQC100-10		Package:	Any	-
EPM7128SQI100-10		Pin count:	Any	-
EPM7128SQC100-15		T IT COURT.	1.40	
EPM7128SQC160-6		Speed grade:	Any	-
EPM7128SQC160-7				_
EPM7128SQC160-10		Core voltage:	5.0V	
EPM7128SQI160-10 EPM7128SQC160-15		Show Adv	anced Devices	
EPM7128STC100-6				
EPM7128STC100-7		Companion d	evice	
EPM7128STC100-10				
EPM7128STI100-10		HardCopy II:	,	
EPM7128STC100-15		Limit DSF		
EPM7160SLC84-6		device re		

Figure 3.3: Family and device settings.

- 5. EDA Tool Settings [page 4 of 5]i) No changes done. → Click Next.
- 6. Summary [page 5of 5]i) Click Finish. (Refer Figure 3.4)

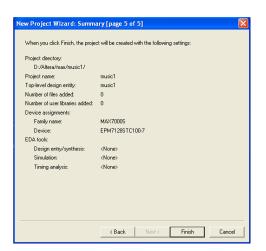


Figure 3.4: Summary.

From the main menu again, File→New is selected. The New popup window appears.
 VERILOG HDL File is chosen and clicks OK. Refer Figure 3.5.

New	×
Device Design Files Software Files Other Files AHDL File Block Diagram/Schematic File EDIF File SOPC Builder System Verlog HOL File VHDL File	
OK Cancel	

Figure 3.5: Device design files.

- 8. Begin the VERILOG design entry for the music1 entity.
- 9. Save the VERILOG file. Make sure that the Add file to current project is checked. Refer to Figure 3.6.

<pre>module music1 (clk,q); input clk; output q; reg [15:0] counter;</pre>	
always 0(posedge clk) counter <= counter	+ 15'b1;
assign q = counter[15];	Save As
endmodule	Save in: 🦳 music1 🗨 🗭 🏦 📅 📰 •
	File name: music1 Save Save as type: Verilog HDL File (*.v;*.vlg;*.vh;*.verilog) ▼ Cancel ▼ Add file to current project

Figure 3.6: Save as popup window.

- 10. Now the design is ready for compilation. To begin compilation, three ways can be accessed :
 - a. Press CTRL+L.
 - ii) At the main menu, select Processing \rightarrow Start Compilation, or
 - iii) Use the icon compilation.

The compiler will begin compiler at once. When full compilation is completed, a popup window message will appear. Click OK to close the window. Refer Figure 3.7.

M	0 97	Thusic I. Y		· · · · ·		,
Module	Progress %	Compilation Report	E	low Summary		
Full Compilation	100 %			ion Saminary		
- Analysis & Synthesis	100 %	🛛 🚑 🖹 Legal Notice				
		Flow Summary				
- Fitter	100 %	Flow Settings				
- Assembler	100 %	Flow Elapsed Time				
Timing Analyzer	100 %	Flow Log				
rinning Andiyzor	100 %					
		🗄 🎒 Analysis & Synthesis				
		🗄 🎒 🔁 Fitter				
		🗄 🎒 📄 Assembler				
		🗄 🗃 🛅 Timing Analyzer				
					E 0 1	
					Flow Status	Successful - Sun Apr 29 21:06:05 2007
						5.1 Build 176 10/26/2005 SJ Web Edition
			Quartu	s II	×	music1
						music1
				Full Compilation w	vas successful (2 warnings)	MAX7000S
			\checkmark			EPM7128STC100-7
				ОК		Final
					is	Yes
			_		l otal macrocells	16/128(13%)
					Total pins	6/84(7%)

Figure 3.7: Full compilation popup window message.

12. Now in the main menu, Tools \rightarrow Simulator Tool is selected. The popup window will appear as shown in Figure 3.8.

Simulation mode: Fund	ctional 🗾	Generate Functional Simulation Netlist					
Simulation input: D:VA	ltera\max\music1\music1.vwf						
Simulation period Run simulation unl End simulation at: Simulation options	til all vector stimuli are used						
· ·	pins to simulation output wavefor	ms					
Check outputs	Waveform Compare Settings						
🔲 Setup and hold tim	ne violation detection						
Glitch detection:	1.0 ns 💌						
Verwrite simulation	on input file with simulation results						
🔲 Generate Signal A	ctivity File:						
0 % 00:00:00							
≿ Start	T Stop	🗘 Open Report					

Figure 3.8: Simulator Tool popup window.

- a. The simulation mode is Functional
- ii) Click on Open. This will generate an empty vector waveform file (*.vwf).

iii) Double-click in the Name area. An Insert Node or Bus popup window will appear:

- Insert the input/output nodes one at a time and click OK every time a node is entered.
- Readjust the input waveforms to the desired value levels of 2ⁿ where n is the number of input nodes in use.
- Save as *.vwf file as music1.vwf.
- Return to the Simulator Tool window and assign the correct *.vwf to the Simulation Input in the Simulator Tool window (Refer Figure 3.9).
- Click on Generate Functional Simulation Netlist. Click OK once finished.
- Click the Start button to begin the simulation.
- The simulation is done and the output waveform is observed.

Simulation mode: Functional Generate Functional Simulation Netlist							
Simulation input: D:\Altera\max\music1\music1.vwf							
Simulation period Run simulation until all vector stimuli are used End simulation at: 100 Ins							
Simulator was successful Simulator was successful Simulator was successful Simulator was successful Cox Cox Cox Cox Cox Cox Cox Cox							
,							
≿ Start 🛛 🐨 Stop 😲 Open 🥋 Report							

Figure 3.9: Simulator Tool window.

13. After finish the Simulation, Pin Planner is selected. The popup window will appear as Figure 3.10 and Figure 3.11.



Figure 3.10: Top view of device pins.

Name	1: *	•			All Pins		Fi	Iter: Pins: all
		Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1		TCK	Input	PIN_62			TTL (default)	
2		TDI	Input	PIN_4			TTL (default)	
3	0	TDO	Output	PIN_73			TTL (default)	
4		TMS	Input	PIN_15			TTL (default)	
5		clk	Input	PIN_87			TTL (default)	
6	•	q	Output	PIN_13			TTL (default)	

Figure 3.11: Pin location.

14. After complete the pins selection, the last step is loading the program in to the UP2 board. Refer to Figure 3.12.

i) Mode JTAG is selected.

- ii) Make sure the Hardware Setup is ByteBlaster[LPT1].
- iii) Press Start to start loading program.
- iv) The program is loaded into UP2 board and it can be tested.

abc music1.v	🛛 🕘 Compilation Report.	🛛 📇 Simulator Tool	🛛 🖸 mus	sic1.vwf	🛛 😻 Pin Pl	anner	
🔔 Hardware Setup	ByteBlaster [LPT1]		Mode	: JTAG			ress:
Enable real-time I	SP to allow background program	ming (for MAX II devices)				
🏓 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blar Che
- Rice	music1.pof	EPM7128ST100	001CAF0D	0000FFFF			

Figure 3.12: Programmer setting.

- 15. The steps are repeated for music2, music3, music4 and music5.
- 3.2 Hardware
- 3.2.1 Hardware Setup

At this project, speaker, Pluto Board, capacitor, ByteBlaster II (all show in Figure 3.13) and Altera Education Kit (Figure 3.14) will be used. The oscillator provides a fixed frequency to the FPGA. The FPGA divides the fixed frequency to drive an IO. The IO is connected to a speaker through a capacitor. By changing the IO frequency, the FPGA produces different sounds.



Figure 3.13: Speaker, ByteBlaster II, Pluto Board and Capacitor

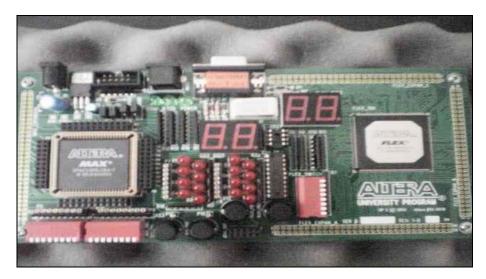


Figure 3.14: Altera Education Board (UP2 Board)

3.2.2 UP2 Education Board Programming or Configuring Devices

Programming or configuring the devices on the UP2 Education Board requires setting the on-board jumpers and the JTAG programming options in the Quartus II software, and connecting the ByteBlaster II download cable to the PC's parallel port and to the JTAG_IN connector on the UP2 Education Board. This section describes how to set these options [2][3].

- Program only the EPM7128S device
- Configure only the EPF10K70 device

3.2.2.1 EPM7128S Programming

This section describes the procedures for programming only EPM7128S devices, (i.e., how to set the on-board jumpers, connect the ByteBlaster II download cable, and set options in the Quartus II software). *Setting the On-Board Jumpers for EPM7128S*

Programming. To program only the EPM7128S device in a JTAG chain, set the jumpers TDI, TDO, DEVICE, and BOARD as shown in Figure 3.15.

_	TDI	_	TDO	D	EVICE	= 6	BOARD	2
	C1		C1		C1		C1	
	C2		C2		C2		C2	
	C3		C3		C3	[]	C3	

Figure 3.15: Jumper Settings for Programming Only the EPM7128S Device [3].

Attach the ByteBlaster II cable directly to the PC's parallel port and to the JTAG_IN connector on the board. For more information on setting up the ByteBlaster II cable, go to the ByteBlaster II Parallel Port Download Cable Data Sheet. The following steps describe how to use the Quartus II software to program the EPM7128S device in a JTAG chain [2][3].

- 1. The Multi-Device JTAG Chain command (JTAG menu) in the Quartus II Programmer is turned on to program a device. This procedure has to be followed even if only programming on one device.
- 2. Multi-Device JTAG Chain Setup (JTAG menu) is chosen.
- 3. EPM7128S in the Device Name list in the Multi-Device JTAG Chain Setup dialog box is selected.
- 4. The name of the programming file for the EPM7128S device is typed in the Programming File Name box. The Select Programming File button can be used to browse a computer's directory structure to locate the appropriate programming file.

- 5. Add is clicked to add the device and associated programming file to the Device Names and Programming File Names box. The number to the left of the device name shows the order of the device in the JTAG chain. The device's associated programming file is displayed on the same line as the device name. If no programming file is associated with a device, "<none>" is displayed next to the device name.
- 6. Detect JTAG Chain Info is clicked to have the ByteBlaster II cable check the device count, JTAG ID code, and total instruction length of the JTAG chain. A message just above the Detect JTAG Chain Info button reports the information detected by the ByteBlaster II cable. This message must be manually verified to match the information in the Device Names & Programming File Names box.
- 7. Save JCF is clicked. In the Save JCF dialog box, the name of the file is typed in the File Name box and then selects the desired directory in the Directories box to save the current settings to a JTAG Chain File (.jcf) for future use. OK is clicked.
- 8. OK is clicked to save changes.
- 9. Program in the Quartus II Programmer is clicked.

3.2.2.2 EPF10K70 Configuration

This section describes the procedures for configuring the EPF10K70 device (i.e., how to set the on-board jumpers, connect the ByteBlaster II download cable, and set options in the Quartus II software). To configure the EPF10K70 device in a JTAG chain, set the jumpers TDI, TDO, DEVICE, and BOARD as shown in Figure 3.16.

т	ы	TDO	D	EVICE	E	BOARD	þ
C	21	C1		C1		C1	
C	2	C2		C2		C2	
c	3	сз		C3		СЗ	

Figure 3.16: Jumper Settings for Configuring Only the FLEX 10K Device [3]

Connecting the ByteBlaster II Download Cable for the EPF10K70 Configuration. Attach the ByteBlaster II cable directly to the PC's parallel port and to the JTAG_IN connector on the UP2 Education Board. The following steps describe how to use the Quartus II software to configure the EPF10K70 device in a JTAG chain [2][3].

- 1. The Multi-Device JTAG Chain command (JTAG menu) in the Quartus II Programmer is turned on to configure the EPF10K70 device. This step is followed even if only programming one device.
- 2. Multi-Device JTAG Chain Setup (JTAG menu) is chosen.
- 3. EPF10K70 in the Device Name list in the Multi-Device JTAG Chain Setup dialog box is selected.
- 4. The name of the programming file for the EPF10K70 device is typed in the Programming File Name box. The Select Programming File button can be used to browse your computer's directory structure to locate the appropriate programming file.
- 5. Add is clicked to add the device and associated programming file to the Device Names and Programming File Names box. The number to the left of the device name shows the order of the device in the JTAG chain. The device's associated programming file is displayed on the same line as the device name. If no programming file is associated with a device, "<none>" is displayed next to the device name.

- 6. Detect JTAG Chain Info is clicked to have the ByteBlaster II cable check the device count, JTAG ID code, and total instruction length of the JTAG chain. A message just above the Detect JTAG Chain Info button reports the information detected by the ByteBlaster II cable. This message must be manually verified that matches the information in the Device Names & Programming File Names box.
- Save JCF is clicked to save the current settings to a JCF for future use. The name of the file is typed in the File Name box and then selects the desired directory in the Directories box in the Save JCF dialog box. OK is clicked.
- 8. OK is clicked to save the changes.

3.3 Summary

This chapter presented both hardware and software setup used in the project. In order to get good results, the setting for device and pin planner is very important. Therefore all settings have to be done carefully and correctly. These setting will be used and tested in Chapter 4 Results and Discussion.