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High Speed And Low Power Devices : Bulk Silicon Versus SOI

Introduction

Chips are made of millions of metal-oxide semiconductor (MOS) transistors. New technique is needed to make chips smaller and faster. One technique to speed up the chip is to use an alternative faster semiconductor. One faster semiconductor that has been under consideration for the last three decades has been silicon-on-insulator (SOI). Silicon-on-insulator (SOI) is a recent breakthrough in semiconductor technology that is advanced chip manufacturing of conventional bulk silicon. It uses a thin layer of silicon on top of an insulator as semiconductor substrate instead of whole thick silicon, by which the capacitance of the transistor will be greatly reduced [1,2,3]. SOI technology extends the operating region of CMOS circuits to lower voltages without sacrificing performance.

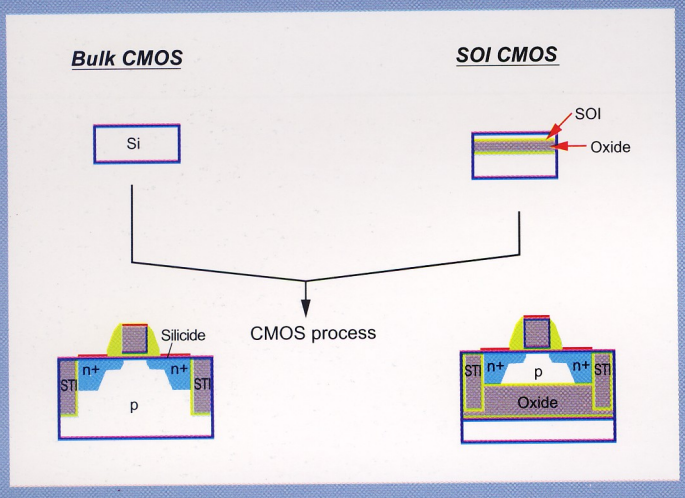

Figure 1: Bulk and SOI CMOS *(Adapted from Ref [1])*

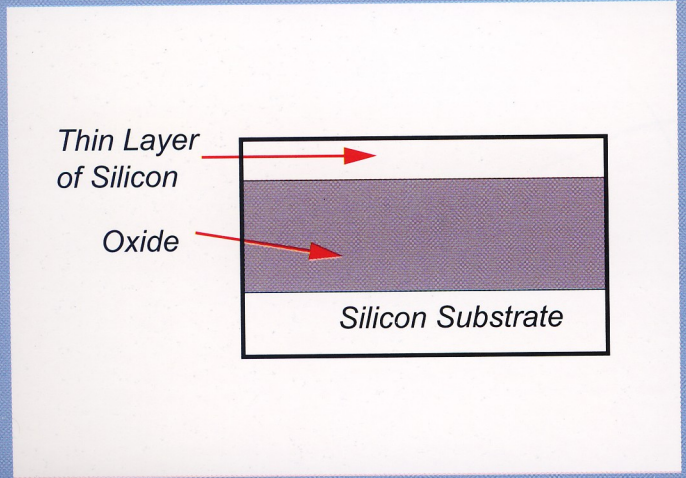

Figure 2 : Basic structure of SOI *(Adapted from Ref [2])*

Silicon-on-insulator differs from CMOS by placing the transistorís silicon junction area on top of an electrical insulator. SOI refers to place a thin layer of silicon on top of insulator such as silicon oxide or glass. Transistors then will built on top of this thin layer of silicon on insulator. The basic idea of SOI technology is to reduce the capacitance of transistor, so it will operate faster [1,2,3].

With the SOI technique, the gate area can be assured of minimal capacitance, which is a measure of ability to store an electrical charge. Any medium that can conduct electricity has some degree of capacitance [2]. Technically, a MOS transistor is regarded as a capacitive circuit. This implies that the MOS circuit must completely charge to full capacitance to activate its switching capability. The process of discharging and recharging the transistor requires a relatively long amount of time in contrast to the time it requires to actually switch the voltage state of the transistorís metal layer. SOI attempts to eliminate this capacitance, as a low capacitance circuit will allow faster transistor operation. As transistor latency drops, the ability to process more instructions in a given time rises.

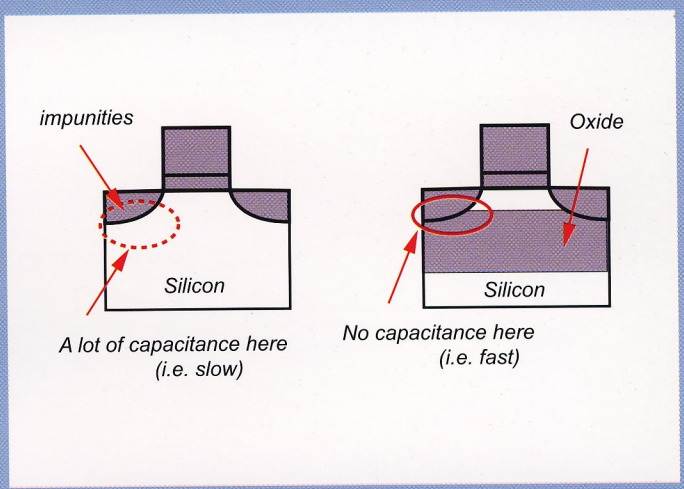

Figure 3 : A MOS circuit (left) compared to an SOI circuit (right) *(Adapted from Ref [2])*

The MOS circuit is slower because a capacitance develops between the impurity layers and the silicon substrate [2]. This boundary area is known as the junction capacitance layer. As noted earlier, a MOS circuit must spend a large amount of its operational time discharging and recharging this capacitance. In comparison, the SOI circuit employs silicon oxide layered over the pure silicon substrate. The SOI circuitís capacitance will be negligible since the silicon oxide provides an efficient insulation barrier. The junction capacitance area is eliminated by SOI, thus the transistor will be able to operate faster since the charging process is eliminated.

SOI technology is also attractive because it involves less processing steps than bulk MOS technology. And also it has excellent capability as a low power technology because SOI circuits operate at low voltage with same performance as a bulk MOS technology at high voltage [3]. When considering SOI, there are three factors that define the performance requirements of the technology: *speed, power consumption, and cost* [3].

SOI Fabrication and Manufacturing

The difference between conventional MOS and Silicon-on-insulator (SOI) construction is a layer of insulating material separating the transistorís silicon junction area and the bulk silicon [1].

Many techniques have been developed for producing SOI materials. Some of them are based on the epitaxial growth of silicon either from seeding window on a silicon wafer covered with an insulator or on single crystalline insulator. Some are based on the crystallization of a thin silicon layer from the melted, such as laser recrystallization, e-beam recrystallization and zone-melting recrytallization [3]. In principle, there are two basic methods of making SOI wafers with required layer thickness less than 0.5 μm (thin film SOI). One mature technique for CMOS application is the use of oxygen implantation and high temperature annealing. This technology is referred to as Separation by Implanted Oxygen (SIMOX). Another approach involves bonding of two wafers with intermediate oxide layer, and subsequent removal of over 99.9% of one the two bonded wafers. This technique is called as wafer bonding. SIMOX is ideal candidate for CMOS application, while wafer bonding is more adapted to bipolar and power applications.

Characterization of SOI Materials

As SOI technology is moving into larger volume commercial product applications, particularly for high speed and low power thin film SOI (silicon-on-insulator) CMOS circuits. High quality, low cost and higher volume availability of SOI wafers are all vital to the continuing growth of the technology. It is important to characterize the SOI wafer in terms of quality after it has been produced. The most critical parameters are the film thickness of silicon layer and BOX layer, Si crystal quality, the concentration of impurities and electrical characteristics.

Benefit of SOI

The major benefits of SOI over bulk silicon transistors are :

1) Substantial reduction of the effective capacitance between the diffusion junction and the substrate and between neighboring devices by shallow-trench isolation. The area where the impurities are added and the pure silicon holds a charge that cause delay in the switching, the process of turning the transistor on and off. An insulator layer between the two areas eliminates the interface and reduces the junction capacitance. The switching speed is to 20% to 30% faster because less charge is needed [1].

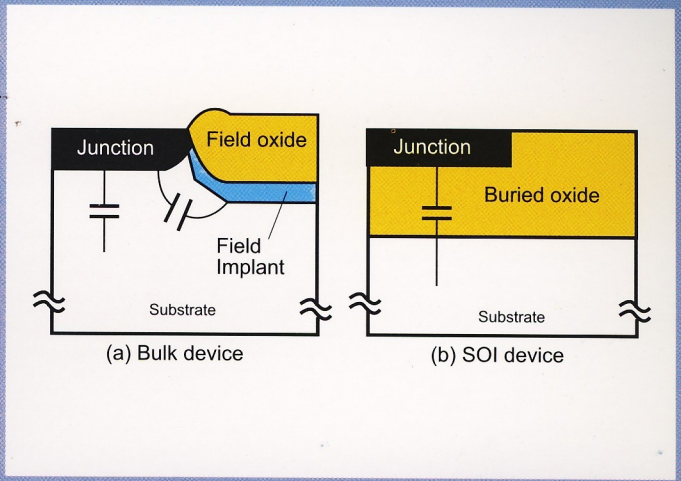

Figure 10 : Parasitic junction capacitances: (a) Capacitance between a junction and the substrate and between the junction and the field in a bulk device; (b) Capacitance between a junction and the substrate *(Adapted from Ref [3])*

2) Electrical performance improvement in the circuit. Because the transistor channel is disconnected from the substrate, the resulting floating-body effect is used to lower the threshold voltage in n-type devices, reduce threshold variation during switching in stacked-transistor logic application [1].

3) Improved latch up immunity and lower RF substrate parasitic when circuit design is properly optimized [1].

4) Reduced soft-error sensitivity: Charge collection volumes are limited in SOI by the BOX layer, reducing soft-error sensitivity. This is important in high performance applications, and is more significant as voltages (noise margin) and device dimensions (critical charges) are correspondingly reduced [1,3].

Future of SOI

SOI offers the opportunity for the use of very-high-resistivity substrates to achieve low-loss passive elements. This capability, along with SOI n-FETs with an f_T of >150GHz, opens exciting opportunities for low-power RF circuits. The ability to integrate vertical SiGe-base bipolar with SOI CMOS will open new application areas for SOI [4].

Bringing SOI into the mainstream of Si technology has been challenging. However, as we move to the 45 nm generation and beyond, SOI offers the total solution, and it will be the technology of choice.

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