Silicon Carbide (SiC) as Non-Volatile Random Access Memory (NVRAM) Material

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ABSTRACT

The extraordinary intrinsic properties of silicon carbide (SiC) have made this material a suitable choice to use in high temperature, high frequency, and high voltage applications. In addition to this, SiC could be employed as the base material for nonvolatile Random Access Memory, mainly due to its extremely low thermal-generation rate at room temperature. In this paper, the reasons of using this material in this particular application are presented and the development of the application over the past fifteen years is reviewed.

Keywords: Metal-Oxide Semiconductor (MOS), Nitrided Gate Oxide, Silicon Carbide (SiC), Nonvolatile Random-Access Memory

A. Introduction

Data in the form of binary digits (bit), **1** or **0**, are stored and manipulated in logic devices called memories. They are two-dimensional arrays of storage elements, controlled either by a bipolar transistor or a metal–oxide–semiconductor field-effect transistor (MOSFET). Since the first semiconductor memory was successfully used in computers in 1969 **[1]**, **[2]**, great interest has been given to this device due to its faster access time, higher packing density, and lower power consumption than non-semiconductor based memories, such as magnetic-based memories. Generally, semiconductor memories can be divided into two broad categories: (1) volatile and (2) nonvolatile.

According to its name, volatile memory does not retain its charge after the power supply is switched off. The main representative of this type of memory is random-access-memory (RAM), whereby it is able to randomly retrieve information without starting from the beginning. Nonvolatile memory enables data to be retained even when power is interrupted. The data storage mode is either permanent or reprogrammable, depending on the technology, and it is normally referred to as Read-Only-Memory (ROM). Since the first appearance of ROM in 1967, this device has evolved rapidly into many different forms **[3]**. Depending on the usage and the flexibility to manipulate storage data, ROM can be sub-classified into four groups: (1) programmable ROM (PROM), (2) erasable or ultra-violet erasable programmable ROM (EPROM or UV-EPROM), (3) electrically erasable programmable ROM (EEPROM or E^{2}PROM), and (4) Flash EEPROM or simply termed as Flash Memory.

The demand for nonvolatile memory in the global market is increasing, mainly due to the growing number of portable, compact, and light-weight electronic appliances **[4]**. Nonvolatile memory, having the ability to retain stored information for longer than 10 years at temperatures as high as 80˚C even without power supplied, is the main requirement for a permanent or semi-permanent storage medium in the above-mentioned devices/systems.

The silicon (Si)-based nonvolatile memories are only associated with ROM technology. These devices, such as Flash Memory, can only withstand limited operation cycles, with too long charging/discharging times to allow for their use in RAM applications **[4]**. RAMs such as dynamic RAM (DRAM) use metal–oxide–semiconductor (MOS) or metal–insulator–metal capacitors (Figure 1) as storage elements. They respond very quickly (nanoseconds) during charging/discharging cycles, but they are *volatile* and need refreshing in order to maintain the stored data. This is a major disadvantage of the above-mentioned gadgets. As a result, many researchers are motivated to find ways and means to develop a next generation nonvolatile memory. SiC has superb intrinsic properties **[5]**, **[6]** and it is possible to fabricate acceptable quality MOS capacitors on it **[7]**, theoretically enabling *nonvolatile random-access memory* (NVRAM) – memory elements with access characteristics of Si RAMs

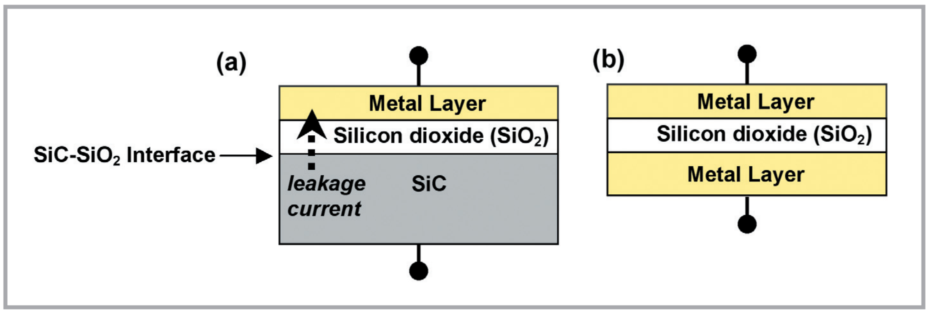

Figure 1 : A (a) metal-oxide-semiconductor (MOS) structure, having the possibility of leakage current through gate oxide and metal-oxide-metal structure [32]

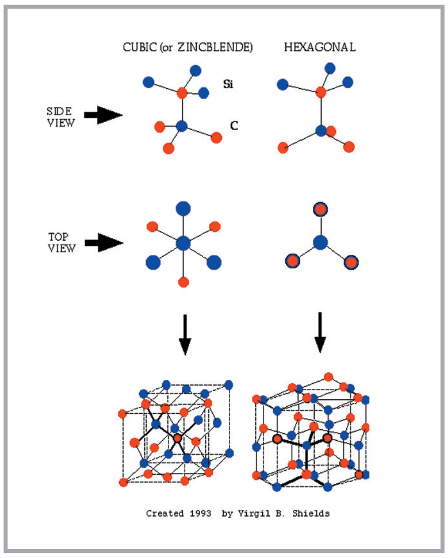

Figure 2: Side and top view along the stacking direction of a cubic (C) and a hexagonal (H) type of SiC [8]

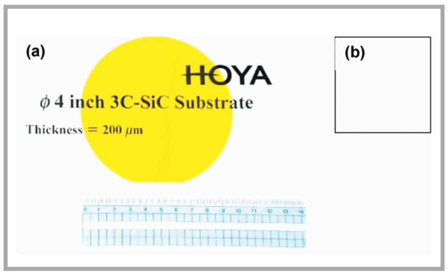

Figure 3: Physical appearance of a (a) 3C SiC and (b) 4H SiC substrates. They are produced by Hoya Advanced Semiconductor Technologies, Japan (www.hast.co.jp/e/index.html) and CREE Inc., USA (www.cree.com), respectively.

and with retention characteristics of Si ROMs – to be made. Although this great concept has been known back in the 90s, the development of this type of device is relatively slow and the SiC research community has less interest in this application compared to other applications, such as power devices. The aim of this paper is to review the development of SiC as the base material in a nonvolatile-memory device, over the past fifteen years, and to introduce the advantages of using SiC for this special application.

B. The Advantages of SiC as Nonvolatile Random-Access Memory Material

SiC was initially discovered by Jöns Jacob Berzelius in 1824 **[8]**. It is a IVB-IVB semiconductor, which has been identified as one of the emerging wide bandgap semiconductors that can revolutionise electronic devices. Even William Shockley, convinced by its unmet electrical and physical properties compared to Si, predicted in 1950s that SiC would replace Si in the near future **[9]**.

A basic structural unit of SiC consists of a Si tetrahedrally bonded with C (Figure 2). It forms over 170 polytypes **[10]**, which means the chemical contents of the polytypes are the same and only the stacking sequence of the tetrahedrally bonded Si–C bilayers changes along the c-axis of the lattice. Generally they can either be classified into zinc-blend [or cubic (C)], wurtzite [or hexagonal (H)] (Figure 2), or combination of those structures. The greater the wurtzite (hexagonal) component is, the larger the bandgap. A more common and convenient way to differentiate these polytypes is by Ramsdell notation **[11]**, which consists of a number followed by a letter. The number represents the number of bilayers in stacking sequence, whereas the letter represents crystal structure. Approximately 95% of all publications on SiC research are about the three main polytypes: 3C, 4H, and 6H **[12]**. Figure 3 shows the difference physical appearance of 3C and 4H SiC substrates.

SiC with its large bandgap, high breakdown field, comparable thermal conductivity to copper, high saturation electron velocity, tremendously low intrinsic carrier concentration, just to name a few properties, has provided much attention to researchers and manufacturers. These superb properties have been reviewed and noted by Harris **[11]**, Goldberg *et al.* **[12]**, Neudeck **[5]**, and Choyke and Pensl **[13]**. These impressive properties are able to fill the needs unmet by other semiconductors, such as Si, in high-temperature, high-frequency, high-power, and nonvolatile-memory applications **[14]**–**[20]**. The revolution in SiC stems primarily from the exploitation of the unique properties offered by SiC compared to Si, GaN, and GaAs and these properties are summarised in Table 1.

SiC exhibits unique material properties, having four promising features to enable it to be considered as the next generation nonvolatile-memory material, namely (1) large bandgap with extremely low intrinsic-carrier concentration, n_i, (2) ability to withstand a harsh environment, such as high temperatures, (3) ability to thermally grow native oxide (SiO_2) on SiC as gate dielectric, and (4) the developed planar

TABLE 1

Comparison of the properties for selected important semiconductors at 300 K [12], [13].

ELECTRICAL AND PHYSICAL PROPERTY	**Si**	**GaN**	**GaAs**	**SiC**		
				4H	**6H**	**3C**
Bandgap (eV)	1.12	3.39	1.42	3.26	3.02	2.39
Relative dielectric constant	11.9	9.0	13.1	9.7	9.7	9.7
Intrinsic carrier concentration (cm^{-3})	10^{10}	$\sim 10^{-5}$	1.8×10^{6}	$\sim 10^{-7}$	$\sim 10^{-5}$	$\sim 10^{-1}$
Breakdown field (MV/cm) @ $N_D = 10^{17}$ cm^{-3}	0.6	5	0.6	3.0	3.2	>1.5
Saturated electron velocity (10^7cm/s)	1.0	2.7	1.2	2.0	2.0	2.5
Electron mobility (cm^2/V-s) @ $N_D = 10^{16}$ cm^{-3}	1200	900	6500	800^A 800^B	60^A 400^B	750^A
Hole mobility (cm^2/V-s) @ $N_A = 10^{16}$ cm^{-3}	420	150	320	115	90	40
Thermal conductivity (W/cm-K)	1.5	1.3	0.5	3 – 5	3 – 5	3 – 5
Melting Point (K)	1690	2773	1510	~3100	~3100	~3100
TECHNOLOGICAL PROPERTY						
Native oxide	Yes	No	No	⟵ Yes ⟶		
Complementary device	Yes	No	No	⟵ Possible ⟶		

^{A} parallel to c-axis
^{B} perpendicular to c-axis

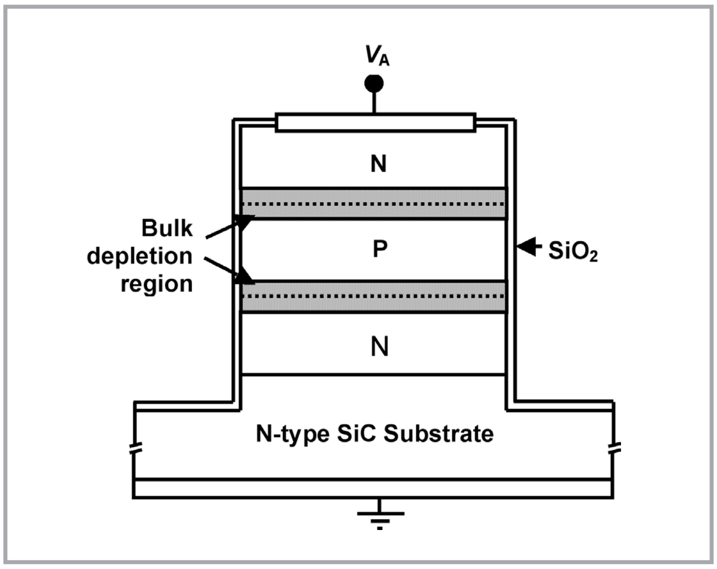

Figure 4: Schematic cross section of a SiC npn charge storage capacitor [32]

technology for Si can be used with little modification for SiC.

Since there are numerous polytypes of SiC, the overview of the advantages of SiC as nonvolatile random-access memory substrate is only focused on the most popular and most widely reported polytypes. They are 3C, 4H, and 6H SiC. The bandgaps of these polytypes are 2 to 3 times larger than the Si (1.12 eV) **[5]**. The larger the bandgap is, the lower the n_i should be. Intrinsic carrier density of a semiconductor defines the number of mobile carriers (that is able to conduct electrically) inherently available in a unit volume of a semiconductor. For example, n_i for 4H SiC is in the order of 10^{-7} cm^{-3} at room temperature. It is approximately 17 orders of magnitude lower than in Si. Given that the rate of thermal generation of minority carriers is proportional to n_i, the thermal generation rate in 4H SiC should be 17 orders of magnitude lower than in Si. Theoretically, the thermal generation rate at room temperature is negligible. Thus, the unintentional change of logical states (**1** or **0**) due to thermal-generation process should be insignificant in a SiC-based memory device.

The applicability of SiC for harsh environment applications, such as high temperature, has long been recognised. Recently, Li *et al.* **[21]** reported a Flash-Memory-like structure on 6H SiC as a nonvolatile memory that is able to withstand temperatures as high as 200ºC.

The remaining two features are related to device-fabrication technology. It is possible to grow thermally stable SiO_2 layer on SiC with the commercially available equipment from standard Si planar technology. Unlike other wide-bandgap materials, SiC is the only material that can oxidise thermally to form SiO_2, which is an important component in a MOS-based device. Oxidation technology seems to play a major role in determining the quality of the SiC–SiO_2 interface and subsequently the charge-retention time of a memory device **[22]**.

C. The Development of SiC-based Nonvolatile Memories

Fifteen years ago, researchers from Purdue University successfully developed and patented the first SiC bipolar-based nonvolatile memory **[19]**, **[20]**, **[23]**, **[24]**, which consisted of a bipolar transistor as a switch to control charges and a *pn* junction diode as a storage element (Figure 4). In this *npn* structure on 6H SiC, Gardner *et al.* **[19]** reported charge-retention time at room temperature of ~3x10^6 years. In that study, the length of charge-retention time was reduced to ~10^6s by using dry SiO_2 as the terminal-junction passivation layer compared to using a wet oxidised passivation layer. The authors concluded that the effect of surface passivation at the surrounding devices plays a major role. Using the same structure but fabricated on 4H SiC, charge-retention time in the range of 21-43 years was reported **[20]**. In comparison, the charge-retention time for devices fabricated from 4H SiC is shorter than from 6H SiC. Wang *et al.* **[20]** have attributed this effect to the quality of the substrate or/and epilayer. There are a few disadvantages in using bipolar structure as storage elements, namely, low packing density **[25]** and high power consumption, approximately 2-3 times more power is consumed in a bipolar structure than in a MOS structure **[25]**.

Based on studies in Si, the problems in using a bipolar structure as nonvolatile memory can be solved using a MOS capacitor, such as in the structure of a Si-based one-transistor one-capacitor (1T–1C) DRAM. In the case of MOS capacitor as storage element, the charge is stored in a potential well created by surface-band bending due to applied gate voltage. Cooper *et al.* and Agarwal *et al.* **[23]** reported this conceptual idea, however, this idea was not supported by any experimental result. This is because the measurements of non-equilibrium charge characteristics in SiC-based MOS capacitors were impossible to do at that time. The main reason behind this is probably because of the difficulty in finding a right process to obtain an acceptable quality of SiC–SiO_2 interface that prevents the charge from leaking through the oxide (Figure 1a). Recently, a high-quality SiC–SiO_2 interface, with an acceptable level of SiC–SiO_2 interface-trap density was reported using a nitridation process **[7]**, **[20]**. Utilising this process to grow gate oxide, the nonvolatile-memory characteristics of MOS capacitor on SiC are achievable and are reported for the first time **[6]**, **[24]**, **[26]-[29]**. The proposed nonvolatile-memory device has a similar structure and operation mechanism as Si-based 1T–1C DRAM. Given that the volatile characteristics of Si-based DRAMs are due to several severe leakage paths, the identification and examination of these leakage mechanisms in a SiC-based 1T–1C NVRAM is necessary. The possible leakage mechanisms, causing unintentional change of logical states in the memory, consist of six different paths. They are **[30]** (Figure 5): (1) leakage through

TABLE 2: *Estimated room-temperature charge-retention times deduced from different leakage paths*

Leakage Path	Charge-retention time (s)	
	N-type 4H SiC	P-type 4H SiC[1]
1[2]	8×10^{12}	3×10^{12}
2	1×10^{17}	1×10^{16}
3[3]	1×10^{19}	2×10^{18}

[1] *a positive voltage is applied to the surrounding of the capacitors (MOS capacitor with a shielding ring) [26].*

[2] *measured by floating-gate technique [29].*

[3] *mathematical analysis introduced in Ref. [32]*

dielectric of a storage MOS capacitor, (2) electron-hole generation in depleted region of a storage MOS capacitor, (3) junction leakage due to electron-hole generation in depletion layer surrounding the drain region of a select MOSFET, (4) tunneling current through gate dielectric of a select MOSFET, (5) leakage through the select MOSFET due to its subthreshold current, and (6) band-to-band tunneling at the edge of the select MOSFET.

The potential of developing a 1T–1C NVRAM on 4H, and 6H SiC has been experimentally investigated **[6]**, **[24]**, **[26]-[29]**. From literature, the investigations were only concentrated on three possible leakage paths [(1) to (3)]. There was no report on the remaining leakage paths. MOS capacitors fabricated on SiC with nitrided oxide-semiconductor interfaces **[31]** were used in the investigations, either as memory elements themselves or as test structures to determine the junction leakage in select MOSFETs, which is connected to the memory elements. Charge leakage through the gate oxide (path 1) has been identified as a main technological issue for the development of the memory elements. Using nitrided SiC–SiO_2 interface, this problem can be minimised. Leakages due to electron-hole generation in depletion regions (path 2) of both the MOS capacitor and of the reverse-biased *pn* junction surrounding the drain region of a select MOSFET (path 3), do not have a significant effect on the nonvolatile characteristics of the proposed device. Table 2 summarises the charge-retention times of the three possible leakage paths **[6]**, **[24]**, **[26]-[29]**, investigated independently.

D. Conclusion

The advantages of SiC as nonvolatile memory material and the development of this material in this particular application have been systematically reviewed. From the scare knowledge accumulated so far, the leakage path via the capacitor's oxide remains a crucial factor for the development of the device. ■

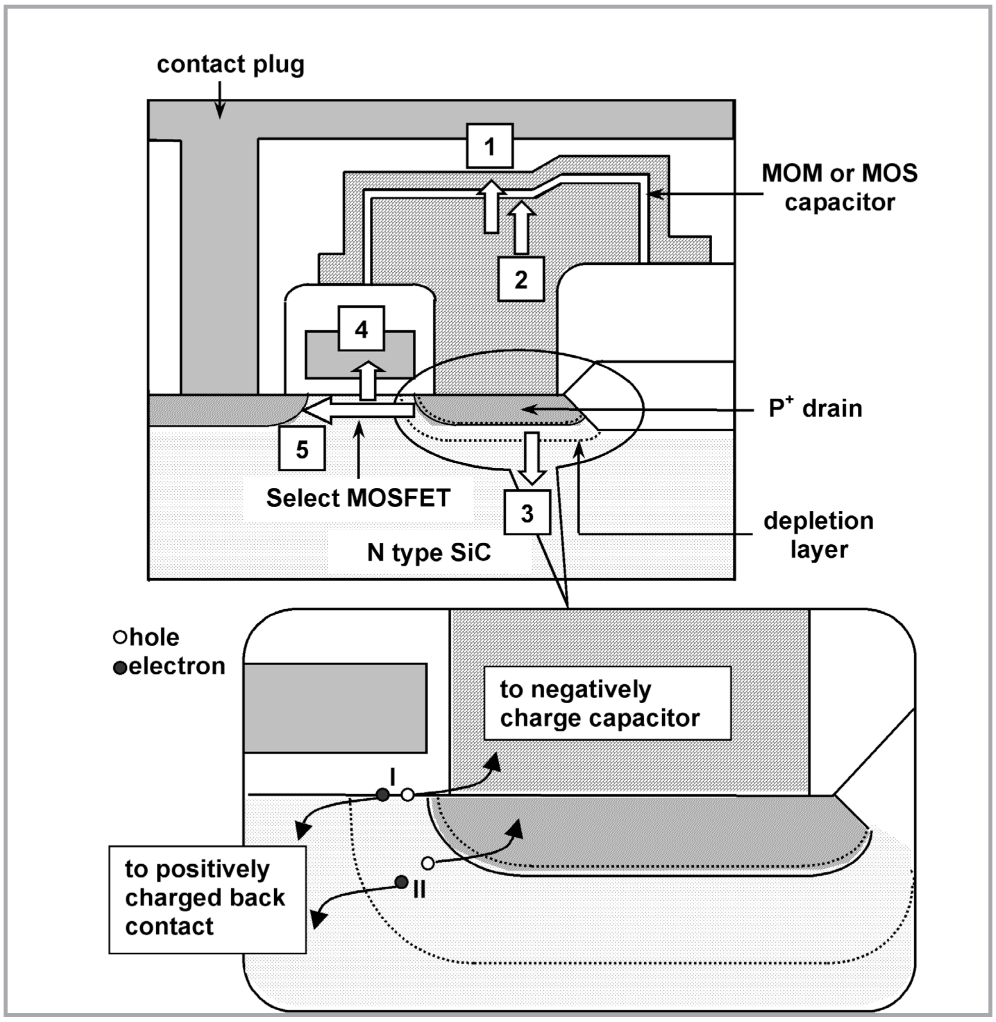

Figure 5: Various possible leakage mechanisms in a proposed SiC-based 1T-1C NVRAM cell: (1) leakage through capacitor dielectric, (2) electron-hole generation in a depleted region of capacitor, (3) junction leakage, (4) tunnel current through gate dielectric of select transistor, and (5) leakage through select transistor subthreshold current. Gate induced drain leakage (GIDL) is not illustrated. The numbers I and II indicate generation of electron-hole from SiC–SiO2 interface and from bulk of a depletion layer in the SiC, respectively. The capacitor is made of metal–oxide–semiconductor (MOS) or metal–dielectric–metal (MOM). If MOM is used, mechanism (2) would not happen [32]

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