CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

This chapter will discuss the theories of ion implantation and diffusion as stated in chapter 1. Since this project is focusing on these two important processes, an understanding in the theories involved is very critical before an analysis can be made hence a realistic good performance device can be fabricated. This chapter will also discuss on point defect such as interstitial and vacancies that are generated during the ion implantation process, the ion projected mechanisms of the ion movement, thermal diffusion and transient enhanced diffusion. The theories that discuss in this chapter is a importance fact and key point for this project.

2.1 Diffusion

The diffusion is the physical phenomenon that material moves from high concentration region to low concentration region, driven by thermal motion of the molecules. Diffusion process happens anywhere and anytime. Perfume is a good example of diffusion in air, sugar, salt and ink of diffusion in liquid; wood soaking in water or oil of diffusion in a solid. Diffusion doping process was widely used in the early years of the IC industry. By introducing high concentration of dopant on the silicon surface with high

temperature, dopants can be diffused into the silicon substrate, which change the conductivity of the semiconductor. Compared with the ion implantation doping process, the diffusion process cannot control the dopant concentration and junction depth. Diffusion is an isotropic process, thus, when used in small feature size, it can cause the neighboring junction short. Therefore, the ion implantation now is mostly replace the diffusion process for small device [3].

Diffusion of impurity is typically done by placing semiconductor wafers in a carefully controlled high temperature quartz-tube furnace and passing a gas mixture that contains the desired dopant through it. The number of dopant atoms that diffuse into the semiconductor is related to the partial pressure of the dopant impurity in the gas mixture. For diffusion in silicon, boron is the popular dopant for introducing a p-type impurity, whereas arsenic and phosphorus are used extensively as n-type dopants. These three elements are highly soluble in silicon, as they have solubility above $5x10^{20}cm^{-3}$ in the diffusion temperature range. Diffusion in a semiconductor can be visualized as atomic movement of the diffusant (dopant atoms) in the crystal lattice by vacancies or interstitials [1].

The basic diffusion process of impurity atoms is similar to that of charge carriers (electrons and holes). Accordingly, we define a flux F as the number of dopant atoms passing through a unit area in a unit time and C as the dopant concentration per unit volume. The equation is shown below:-

$$F = -D\frac{\partial C}{\partial x} \tag{1}$$

where we have substituted C for the carrier concentration and the proportionality constant D is the diffusion coefficient or diffusivity. Note that the basic driving force of the diffusion process is the concentration gradient dC/dx. The flux is proportional to the concentration gradient and the dopant atoms will move (diffuse) away from a high concentration region toward a lower concentration region [1].

If we substitute Equation 1 into the one-dimensional continuity under the condition that no material are formed or consumed in the host semiconductor (i.e., Gn=Rn=0), we obtain

$$\frac{\partial C}{\partial t} = -\frac{\partial F}{\partial x} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x} \right) \tag{2}$$

Continuity equation:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial Jp}{\partial x} + \left(Gn - Rn \right) \tag{3}$$

when the concentration of the dopant atom is low, the diffusion coefficient can be considered to be independent of doping concentration and equation 2 becomes

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \tag{4}$$

The equation 4 is often referred to as fick's diffusion equation. The diffusion coefficient can be expressed as below when implies over the temperature range [1]: -

$$D = Do\exp\left(\frac{-Ea}{kT} \right) \tag{5}$$

where Do is the diffusion coefficient in cm^2/s extrapolated to infinite temperature and Ea is the activation energy in eV. For the interstitial diffusion model, Ea is related to the energies required to move dopant atoms from one interstitial site to another. The values of Ea are found to be between 0.5 and 2 eV in both silicon and gallium arsenide. For the vacancy diffusion model, Ea is related to both the energies of motion and the energies of formation of vacancies. Thus, Ea for vacancy diffusion is larger than that for interstitial diffusion, usually between 3 and 5 eV [1].

The diffusion profile of the dopant atoms is dependent on the initial and boundary condition. In this subsection we consider two importance cases, namely constant-surface concentration diffusion and constant–total-dopant diffusion. In the first case, impurity

atoms are transported from a vapor source on to the semiconductor surface and diffused into the semiconductor wafer. The vapor source maintains a constant level of surface concentration during the entire diffusion period. In the second case, a fixed amount of dopant is deposited onto the semiconductor surface and is subsequently diffused into the wafer. The junction depth is defined as the point where the diffused dopant concentration equals the substrate dopant concentration [1].

When a host atom requires sufficient energy from the lattice vibration to leave its lattice site, a vacancy is created. Depending on the charges associated with a vacancy, we can have a neutral vacancy V^0, an acceptor vacancy V^-, a double charge acceptor vacancy V^{2-}, a donor vacancy V^+ and so forth. We expect that the vacancy density of a given charge state (i.e. the number of vacancies per unit volume Cv has a temperature dependence similar to that of the carrier density that is)

$$Cv = Ci \exp\left(\frac{Ef - Ei}{kT}\right) \tag{6}$$

where Ci is the intrinsic vacancy density, Ef is the Fermi level, and Ei is the intrinsic Fermi level [1].

If the dopant diffusion is dominated by the vacancy mechanism, the diffusion coefficient is expected to be proportional to the vacancy density. At low doping concentration (n<ni), the Fermi level coincides with the intrinsic Fermi level (Ef = Ei). The vacancy density is equal to Ci and is independent of doping concentration. The diffusion coefficient, which is proportional to Ci also, is independent of doping concentration. At high concentration (n>ni). The Fermi level will move toward the conduction band edge (for donor-type vacancies) and the term (exp (Ef-Ei)/kT) becomes larger than unity. This causes Cv to increase, which in turns causes the diffusion coefficient to increase. When the diffusion coefficient varies with dopant concentration the equation can be written as

$$D = Ds\left(\frac{C}{Cs}\right)^{\gamma} \tag{7}$$

Where Cs is the surface concentration, Ds is the diffusion coefficient as the surface and γ is a parameter to describe the concentration dependence. For such a case, we can write the diffusion equation 2 states above as an ordinary differential equation and solve it numerically [1].

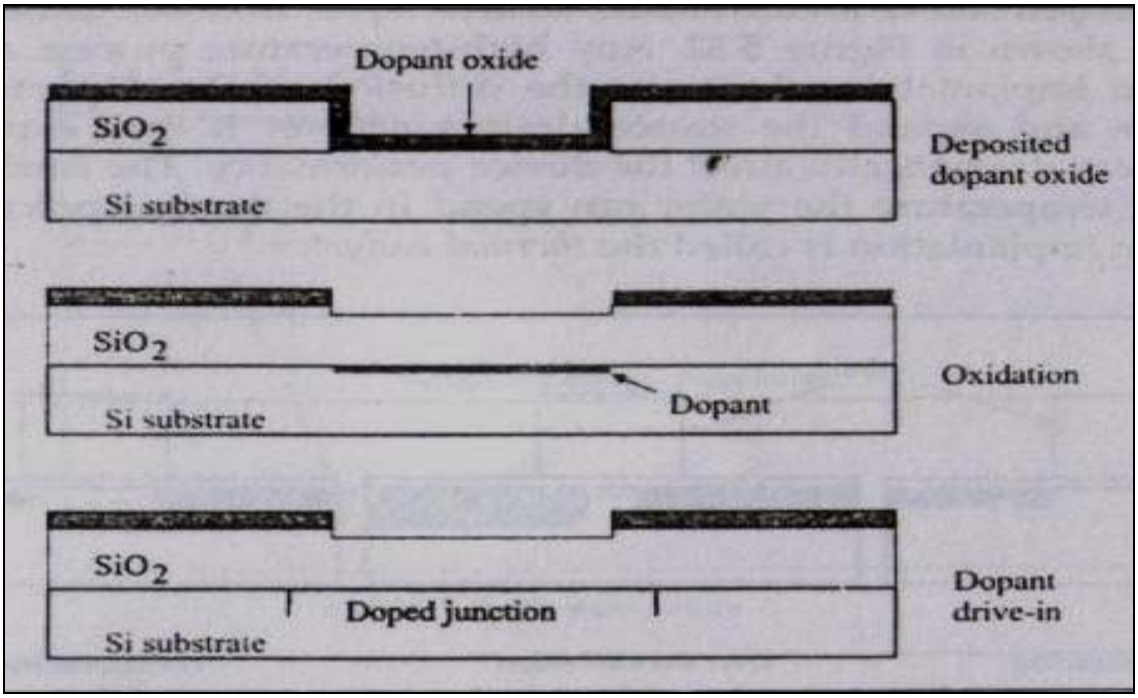

Figure 2.0: Diffusion doping process sequence [3]

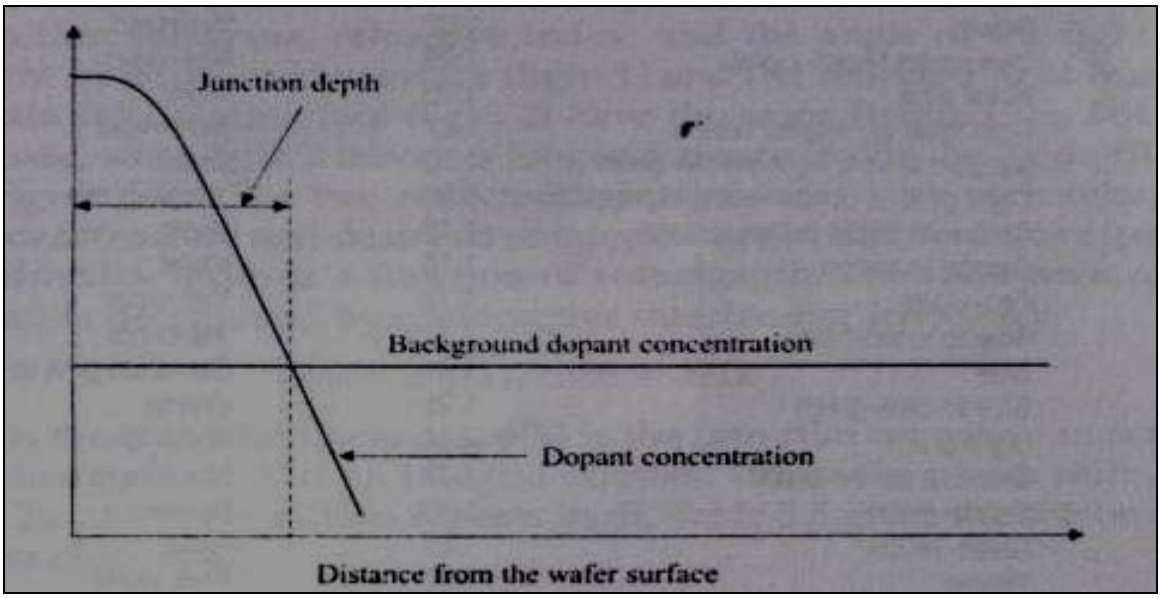

Figure 2.1: Definition of the junction depth [3]

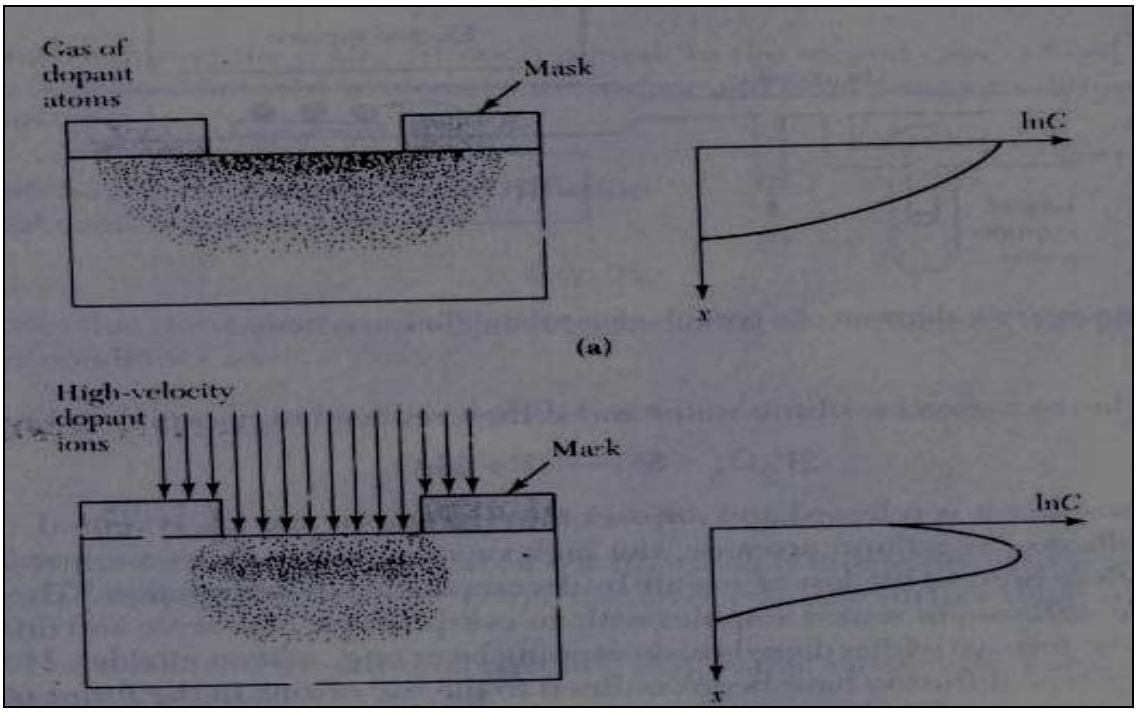

Figure 2.2: Comparison of diffusion and (below (a)) ion implantation technique for the selective introduction of dopant into semiconductor substrate [3]

2.2 Interstitial, Vacancy & Dislocation

Like anything else in this world, crystals inherently possess imperfections, or what is often refered to as 'crystalline defects'. The presence of most of these crystalline defects is undesirable in silicon wafers, although certain types of 'defects' are essential in semiconductor manufacturing. Engineers in the semiconductor industry must be aware of, if not knowledgeable on, the various types of silicon crystal defects, since these defects can affect various aspects of semiconductor manufacturing - from production yields to product reliability [7].

Crystalline defects may be classified into four categories according to their geometry. These categories are: zero-dimensional or ‘point’ defects; one-dimensional or ‘line’ defects; two-dimensional or ‘area’ defects; and three-dimensional or ‘volume’ defects. Table 2.0 presents the commonly-encountered defects under each of these categories [7].

There are many forms of crystal point defects. A defect where in silicon atom is missing from one of these sites is known as a 'vacancy' defect. Lattice from one atom atomic site to another if there is enough activation energy provided by the thermal vibration of the atoms and if there are vacancies or other crystal defects in the lattice for atoms to move in. Vacancies in metals and alloys are equilibrium defects and therefore some are always present to enable substitution diffusion of atoms take place. As the temperature of the metal increase, more vacancies are present and more thermal energy is available and so the diffusion rate is higher at higher temperature. During self-diffusion or substitution solid-state diffusion, atoms must break the original bonds among atoms and replace these with new bonds. This process is assisted by having vacancies present and thus it can occur at lower activation energies. Diffusion can also occur by the vacancy mechanism in solid solutions. Atomic size difference and bonding energy differences between the atoms are factors that affect the diffusion rate [7, 8].

If an atom is located in a non-lattice site within the crystal, then it is said to be an 'interstitial' defect. The interstitial diffusion of atoms in crystal lattices takes place when atom moves from one interstitial site to another neighboring interstitial site without permanently displacing any of the atoms in the matrix crystal lattice. For the interstitial mechanism to be operative the size of the diffusing atoms must be relatively small compared to the matrix atoms [7, 8].

If the interstitial defect involves a silicon atom at an interstitial site within a silicon crystal, then it is referred to as a 'self-interstitial' defect. Vacancies and self-interstitial defects are classified as intrinsic point defects [2].

If an atom leaves its site in the lattice (thereby creating a vacancy) and then moves to the surface of the crystal, then it becomes a 'Schottky' defect. On the other hand, an atom that vacates its position in the lattice and transfers to an interstitial position in the crystal is known as a 'Frenkel' defect. The formation of a Frenkel defect therefore produces two defects within the lattice - a vacancy and the interstitial defect, while the formation of a Schottky defect leaves only one defect within the lattice, i.e., a vacancy. Aside from the formation of Schottky and Frenkel defects, there's a third mechanism by which an intrinsic point defect may be formed, i.e., the movement of a surface atom into an interstitial site [7, 8].

Extrinsic point defects, which are point defects involving foreign atoms, are even more critical than intrinsic point defects. When a non-silicon atom moves into a lattice site normally occupied by a silicon atom, then it becomes a 'substitution impurity.' If a non-silicon atom occupies a non-lattice site, then it is referred to as an 'interstitial impurity.' Foreign atoms involved in the formation of extrinsic defects usually come from dopants, oxygen, carbon, and metals [7].

The presence of point defects is important in the kinetics of diffusion and oxidation. The rate at which diffusion of dopants occurs is dependent on the concentration of vacancies. This is also true for oxidation of silicon [7].

Table 2.0: Examples of Crystalline Defects [7]

Defect Type	Examples
Point or Zero-Dimensional Defects	Vacancy Defects Interstitial Defects Frenkel Defects Extrinsic Defects
Line or One-Dimensional Defects	Straight Dislocations (edge or screw) Dislocation Loops
Area or Two-Dimensional Defects	Stacking Faults Twins Grain Boundaries
Volume or Three-Dimensional Defects	Precipitates Voids

Crystal line defects are also known as 'dislocations', which can be classified as one of the following: edge dislocation; screw dislocation; or mixed dislocation, which contains both edge and screw dislocation components [7].

An edge dislocation may be described as an extra plane of atoms squeezed into a part of the crystal lattice, resulting in that part of the lattice containing extra atoms and the rest of the lattice containing the correct number of atoms. The part with extra atoms would therefore be under compressive stresses, while the part with the correct number of atoms would be under tensile stresses. The dislocation line of an edge dislocation is the line connecting all the atoms at the end of the extra plane [7].

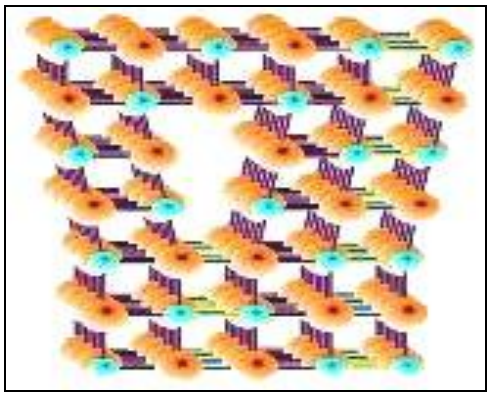

Figure 2.3: An edge dislocation; note the insertion of atoms in the upper part of the lattice [7]

If the dislocation is such that a step or ramp is formed by the displacement of atoms in a plane in the crystal, then it is referred to as a 'screw dislocation.' The screw basically forms the boundary between the slipped and unslipped atoms in the crystal. Thus, if one were to trace the periphery of a crystal with a screw dislocation, the end point would be displaced from the starting point by one lattice space. The dislocation line of a screw dislocation is the axis of the screw [7, 9].

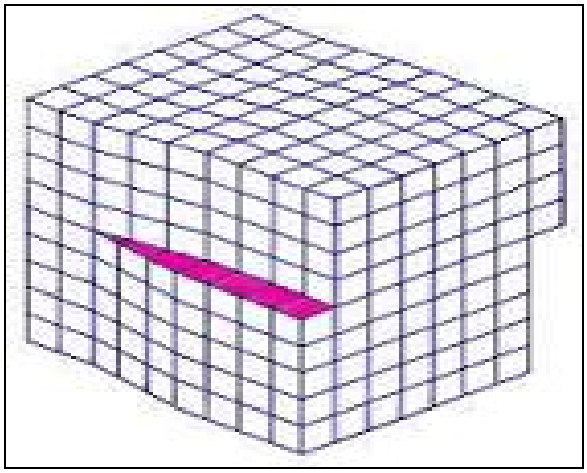

Figure 2.4: A screw dislocation; note the screw-like 'slip' of atoms in the upper part of the lattice [7].

If the dislocation consists of an extra plane of atoms (or a missing plane of atoms) lying entirely within the crystal, then the dislocation is known as a 'dislocation loop.' The dislocation line of a dislocation loop forms a closed curve that is usually circular in shape, since this shape results in the lowest dislocation energy [7, 9]

Dislocations are generally undesirable in silicon wafers because they serve as sinks for metallic impurities as well as disrupt diffusion profiles. However, the ability of dislocations to sink impurities may be engineered into a wafer fabrication advantage. i.e., it may be used in the removal of impurities from the wafer, a technique known as ‘gettering’ [7, 9].

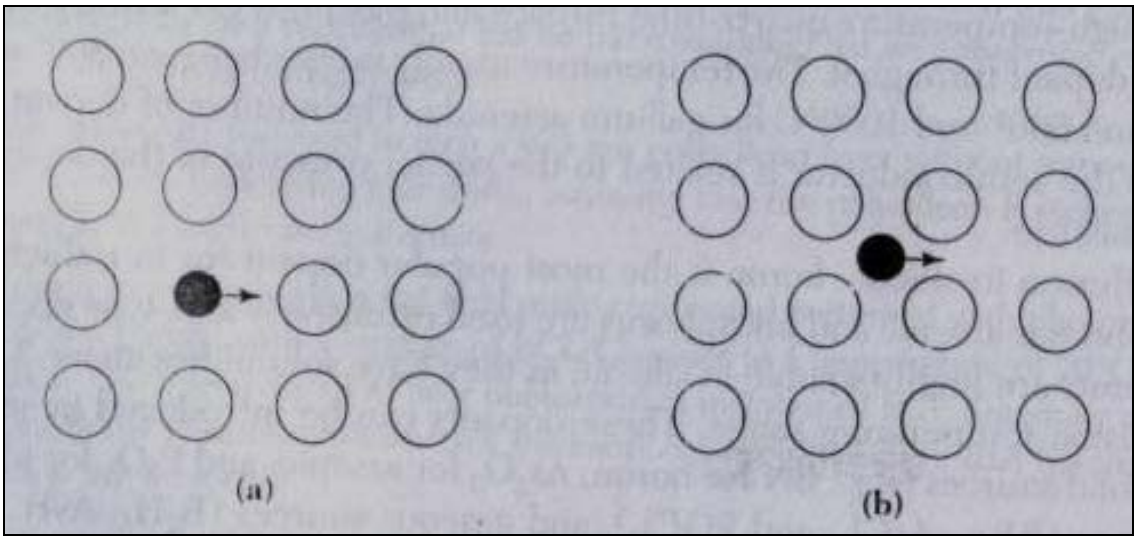

Figure 2.5: Atomic diffusion mechanism for a two-dimensional lattice. (a) Vacancy mechanism; (b) interstitial mechanism [1].

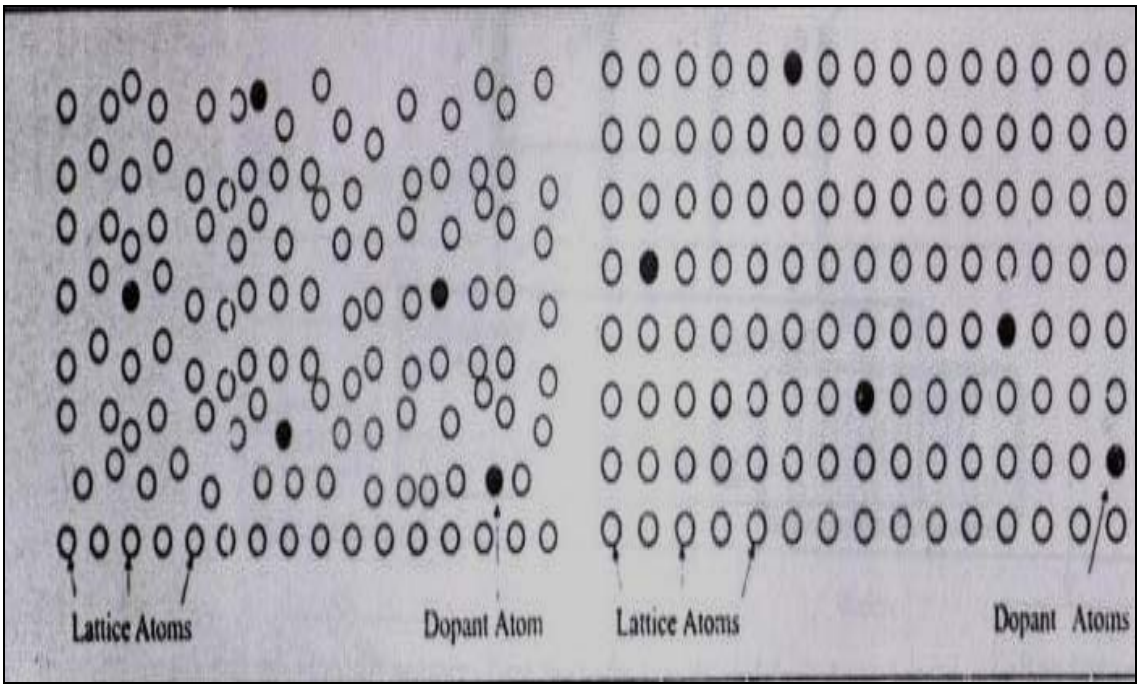

Figure 2.6: Crystal damage (left) & annealing process (right) [1]

2.3 Ion Implantation

Ion implantation is an adding process by which dopant atoms are forcefully added into the semiconductor in the form of energetic ion beam injection. It is the dominant doping method in the semiconductor industry and is commonly used for various doping processes in IC fabrication [3].

Pure single-crystal silicon has a high receptivity; the purer the crystal, the higher the receptivity. Its conductivity can be improved by adding dopants, such as boron, phosphorus, arsenic or antimony. Boron is a p-type dopant with only three electrons in the outermost orbit (the valence shell). It provides a hole when a boron atom is replacing a silicon atom in single-crystal silicon lattice. Phosphorus, arsenic and antimony atoms have five electrons in the valence shell, so they can provide electrons in the single-crystal silicon to conduct electrical current. Because an electron is a negative charge, phosphorus, arsenic and antimony are called n-type dopants and semiconductors with these dopants are called n-type semiconductors [3].

The ion implantation process provides much better control of doping than the diffusion process. For example, the dopant concentration and junction depth cannot be independently controlled in the diffusion process because both are related to the diffusion temperature and time. Ion implantation can independently control both dopant concentration and junction depth. Dopant concentration can be controlled by the combination of ion beam current and implantation time and junction depth can be control by the ion energy. The ion implantation process can dope with the wide range of dopant concentration from 10^{11} to 10^{17} atom/cm^2. ion implantation is a room temperature process and a thick layer of photoresist can block the energetic dopant ions. Ion implantation can used photoresist as the patterning mask and does not need to grow and etch silicon oxide to form the hard mask as the diffusion doping process does [3].

The main application for ion implantation is doping the semiconductor substrate. A silicon wafer needs to be doped to change its conductivity in designated areas to form

junctions, such as wells and source/drain for a CMOS IC. For the bipolar IC, doped junctions are needed to form the buried layer, emitter, collector and base. Other applications for ion implantation are ore amorphous implantation and buried layer implantation. The preamorphous implantation with silicon or germanium creates an amorphous layer on the substrate surface. It allows easier junction depth and profile control in the subsequent dopant implantation process [3].

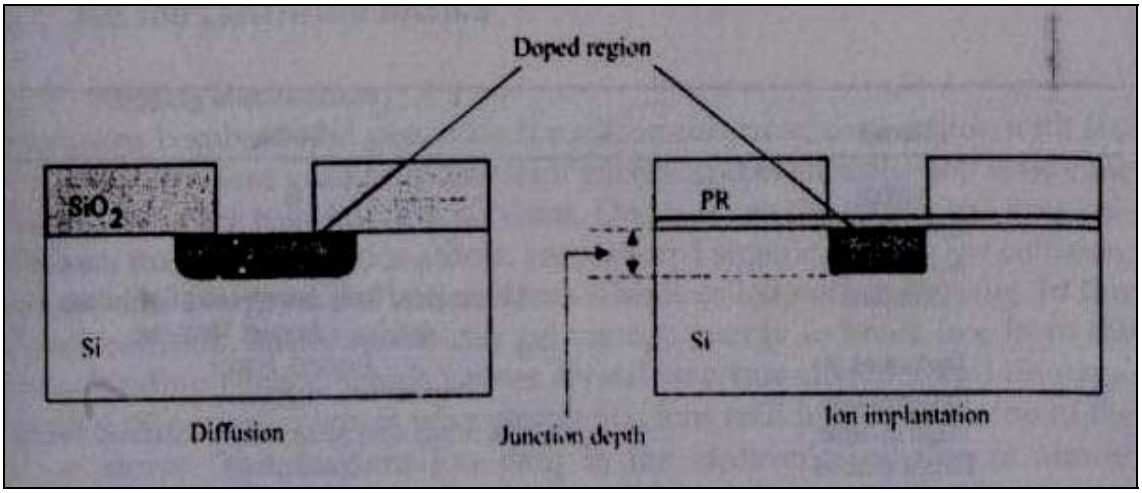

Figure 2.7: Comparison of ion implantation and diffusion doping profile [3]

When ion bombard and penetrate the silicon substrate, they collide with lattice atoms. The ion gradually loses their energy and eventually stops inside the silicon. There are two stop mechanisms. One is when implanted ions collide with nuclei of the lattice atoms, are scattered significantly by the collision and transfer energy to the lattice atoms. This is called nuclear stopping. In this ‘hard’ collision, lattice atoms can get enough energy to break free from the lattice binding energy, which causes crystal structure disorder and damage. Another stop mechanism is when incidental ions collide with electrons of the lattice atoms. The incident ion path in the electronic collision is almost unchanged, energy transfer is very small and crystal structure damage is negligible. This ‘soft’ collision is called electronic stopping. The total stopping power, which is the energy loss of the ion per

unit distance it travels inside the substrate, can be expressed as: $S_{total} = S_n + S_e$. Here S_n is the nuclear stopping power and S_e is the electronic stopping power [3].

The average rate of energy loss with distance is given by a superposition of the above two stopping mechanisms:

$$\frac{dE}{dx} = Sn(E) + Se(E) \tag{8}$$

Where $Sn(E)$ electronic stopping is power and $Se(E)$ is nuclear stopping power [1].

If the total distance traveled by the ion before coming to rest is R, then

$$R = \int_0^R dx = \int_0^{E_0} \frac{dE}{Sn(E) + Se(E)} \tag{9}$$

Where E_0 is the initial ion energy. The quantity R has been defined previously as the range [1].

We can visualize the nuclear stopping process by considering the elastic collision between an incoming hard sphere (energy E_0 and mass M_1) and a target hard sphere (initial energy zero and mass M_2) [1].

Energetic ions penetrate the target, gradually lose their energy through collisions with the atoms in the substrate and eventually rest inside the substrate. Figure 2.9 shows the trajectory of an ion inside the substrate and the definition of the ion projected [3].

Generally, the higher the ion energy, the deeper it can penetrate into the substrate. However, even with the same implantation energy, ions do not stop exactly at the same depth in the substrate, because each ion has different collisions with different atoms. The projected ion range always has a distribution, as illustrated in figure 2.10 [3].

Higher energy ion beam can penetrate deeper into the substrate and therefore have a longer projected ion range. Since smaller ions have smaller collision cross sections, smaller ions at the same energy level can penetrate deeper into the substrate and the mask material.

Figure 2.11 illustrates the projected range at different energy level for boron, phosphorus, and arsenic and antimony ion in the silicon substrate [3].

Projected ion range is an importance parameter for ion implantation because it indicates the ion energy needed for certain dopant junction depth. It also gives information on the required implantation barriers thickness for the ion implantation process. Figure 2.12 shows the require thickness of different barriers material for 200-kev dopant ion. We can see that for ion energy of 200 kev, boron ion require the thickest masking layer. This is because boron has the lowest atomic number, smallest size and longest projection range, so it can penetrate more deeply into the materials than any other dopant ions. For the low atomic number atoms, such as boron, the main stopping mechanisms is electronic stopping at high-energy level, whereas nuclear stopping is the main stopping mechanism for the high atomic number dopant atoms. Similarly, the dopant ion with highest atomic number, antimony, has the highest stooping power and shortest projection range, therefore requires thinnest masking material [3].

The projected range of an ion in an amorphous material always follows Gaussian distribution also called normal distribution. In single crystal silicon, the lattice atoms have orderly arrangement and lots of channels can be seen at certain angles. If ion with the right implantation angle enters the channel, it can travel a long distance with very little energy loss [3].

The exponential tail is related to the ion channeling effect. Channeling occurs when incident ions align with a major crystallographic direction and are guided between rows of atoms in a crystal. Channeling can be minimized by several techniques: a block amorphous surface layer, misorientation of the wafer and creating a damaging layer in the wafer surface. The usual blocking amorphous layer is simply a thin layer of growth silicon dioxide. The layer randomizes the direction of the ion beam so that the ions enter the wafer at different angles and not directly down the crystal channels. Misorientation of the wafers 5^{o}-10^{o} off the major plane also has the effect of preventing the ions from entering the channels. With this method, most implantation machines tilt the wafer by 7^{o} and then apply

a 22^{o} twist from the flat to prevent channeling. Pre damaging the wafer surface with a heavy silicon or germanium implant creates a randomizing layer in the wafer surface. This method however increases the use of the expensive ion implanters [1, 3].

In an ion implantation process, ion gradually loses their energy by colliding with lattice atoms, transferring their energy to these atoms in the process. The transferred energy is high enough for these atoms to break free from the lattice binding energy, typically 25 ev. These freed atoms also collide with other lattice atoms while traveling inside the substrate and knock them free from the lattice by transferring enough energy to free other lattice atoms [1, 3].

One energetic ion can cause thousands of displacements of lattice atoms. The damage created by one ion can be quickly self annealed by the thermal movement of the atoms inside the substrate at the room temperature. However, in an ion implantation process, the amount of ions is so large that it always causes such substantial lattice damage in the single-crystal substrate that the layer close to the surface becomes amorphous and the self-annealing process can't repair the crystal damage in a short time. The damage effect is related to the dose, energy and mass of the ion species; it increase when dose and ion energy increase. If the implantation dose is high enough, the substrate crystal structure can be completely destroyed and become amorphous near the substrate surface within the ion range. To achieve device requirement, the lattice damage must be repaired in an annealing process to restore the single-crystal structure and activate the dopant. Only when dopant atoms are at the single-crystal lattices can they effectively provide electrons or holes as the majority carriers for electric current [1, 3].

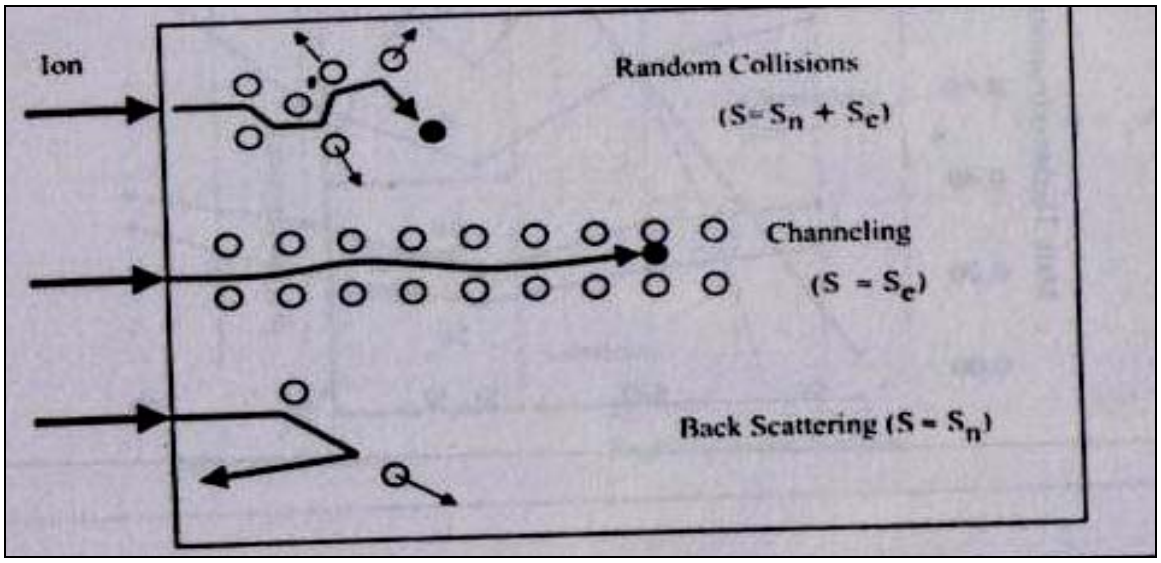

Figure 2.8: Different stopping mechanism [3]

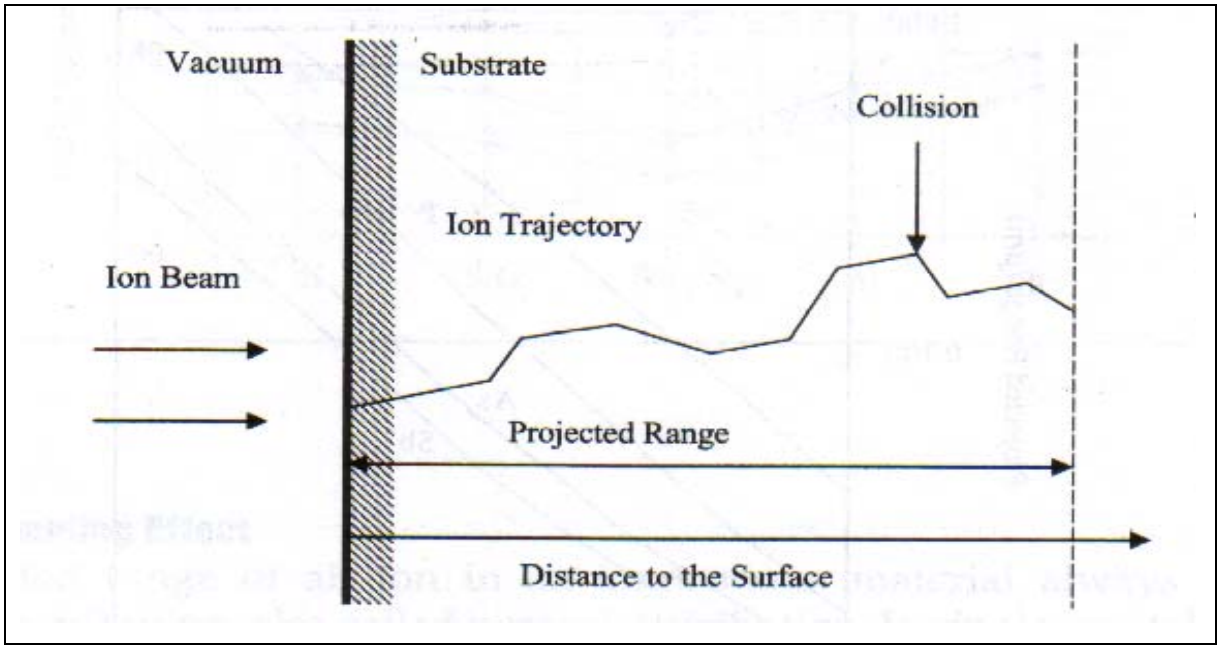

Figure 2.9: Ion trajectory and projected ion [3]

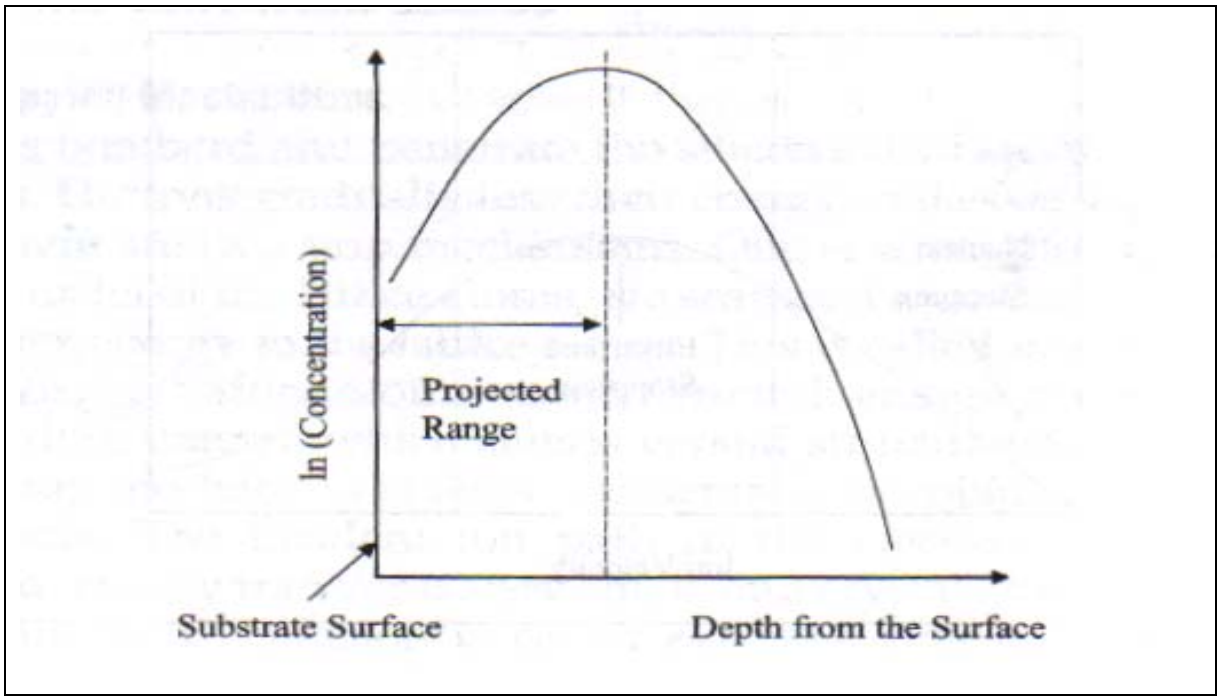

Figure 2.10: Distribution of the projected ion range [3]

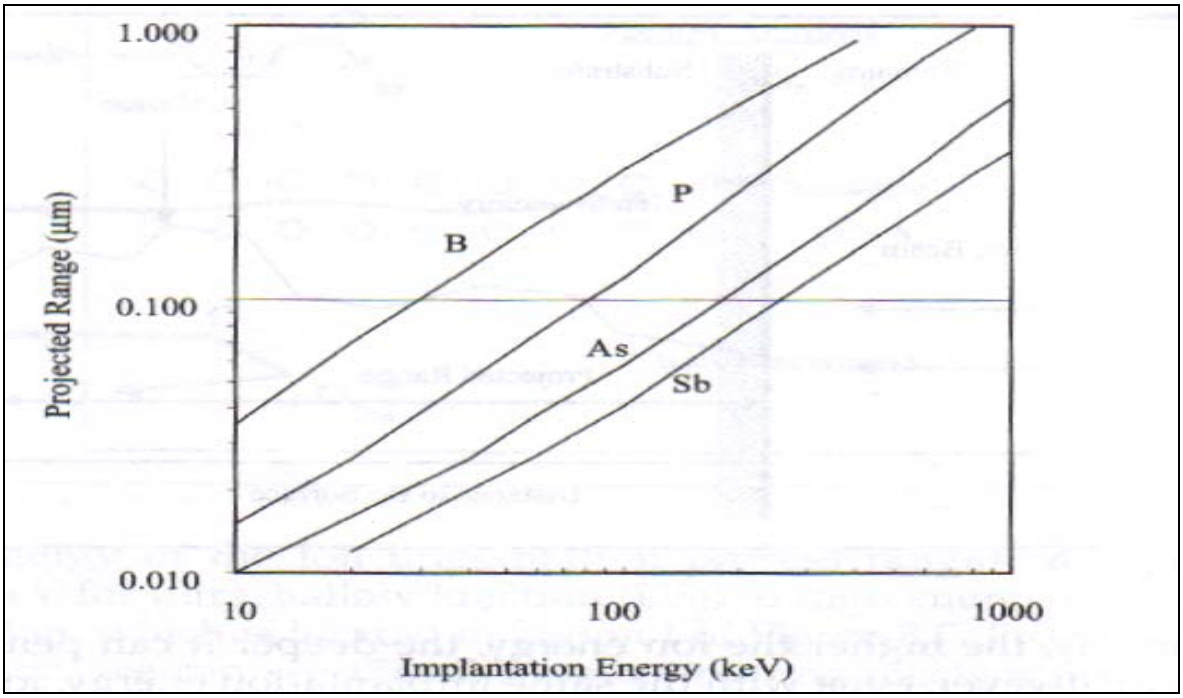

Figure 2.11: Projected range of dopant ions in silicon [3]

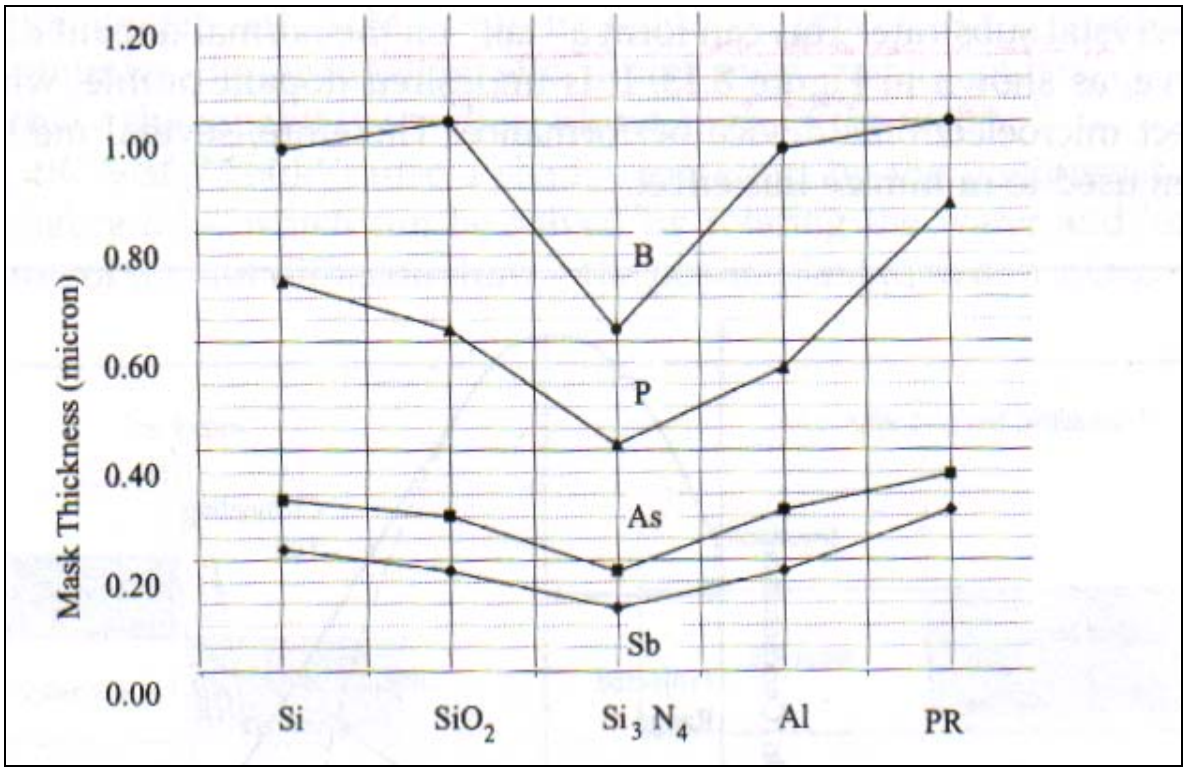

Figure 2.12: Required barrier thickness for 200-kev dopant ion [3]

2.4 Transient Enhanced Diffusion (TED) & Boron Thermal Diffusion

The minimization of boron diffusion is vitally important in metal-oxide-semiconductor (MOS) transistors for the control of short channel effects, and in bipolar transistors for achieving narrow base widths and hence high values of cutoff frequency. However, this is difficult to achieve in practice because of both boron thermal diffusion and transient, enhanced diffusion due to damage created during ion implantation [10].

Recently, there has been considerable interest in the use of fluorine to suppress transient enhanced boron diffusion (TEBD) in silicon. Early work showed that reduced TEBD was obtained when BF_2^+ was implanted instead of B^+. In a later work, Ohyu et al implanted F^+ separately and showed that the fluorine implant reduced TEBD and increased the boron activity. However, there have also been contradictory reports in the literature, which showed that fluorine implants had little or no effect on boron diffusion and even enhanced boron diffusion in amorphous silicon, while there has been considerable research on the effect of fluorine on TEBD, little has been published on the effects of fluorine on the thermal diffusion of boron. In this letter, a study is made of the effect of fluorine on the diffusion of boron in buried marker layers. Samples with and without a P^+ implant is studied so that the effect of fluorine on both TEBD and thermal diffusion can be separately characterized. It is shown that fluorine not only eliminates TEBD, but also dramatically reduces boron thermal diffusion [10]

Understanding and quantifying the phenomenon of transient enhanced diffusion (TED) of dopants is one of the central challenges of ion implantation research and development. There is now a consistent framework describing the underlying physical processes in which silicon interstitials produced by the ion implantation damage interact with dopants, such as boron, causing their enhanced diffusion. Within this framework, however, there are considerable gaps in our basic knowledge of some of the critical phenomena: for example. The source and emission mechanisms of the silicon interstitials and their diffusion mechanisms. These phenomena must be identified and quantified for

realistic modeling of the enhanced diffusion process. Here we describe our experimental and theoretical investigations addressing these issues [11].

The transient enhanced diffusion (TED) of dopants in silicon is a central issue in silicon device processing because TED is a limiting factor for shallow junction formation. It is generally accepted that the large super saturation of silicon self-interstitials produced by ion implantation damage causes TED. A recent study showed that {3 1 1 } self-interstitial clusters are the source of the self interstitials for TED , and a kinetic equation has been proposed to describe the time evolution of the cluster [12].

However, to the author's knowledge, there have been no simulation results that quantitatively fit the time dependent profiles of TED, mainly due to the difficulty in modeling the cluster evolution because of the need to take into account the decrease in the evolution rate with elapsed time as small clusters grow into larger ones (Ostwald ripening). This paper describes a simulation based on the cluster evolution and the kick-out mechanism for B diffusion and that takes into account the decrease in cluster evolution rate with time due to Ostwald ripening. The time evolution of the experimental boron TED data induced by silicon implantation with different doses and energy was successfully fitted using a unified set of parameters [12].

Transient enhanced diffusion (TED) occurs when ion-implanted boron atoms in crystalline silicon are subjected to thermal annealing. The boron diffusivity is enhanced by many orders of magnitude greater than boron diffusivity in a thermal equilibrium for a transient period of time [13].

The scaling down of CMOS device channel length requires a reduction in the source/drain extension junction depth to minimize the short channel effects. This is one of the major challenges in the fabrication of shallow p/n junctions. Although boron is used frequently for this application, its beam current at low energies can be a limiting factor on throughout in device production. An alternative is to implant molecular species such as BF_2^+**.** Despite the effort in achieving shallow "as-implanted" profiles by reducing the

implant energy of B^+ implants, boron transient enhanced diffusion (TED) limits the final junction depth after post-implantation annealing [14].

It was found that boron junction depth after annealing is shallower in BF_2^+ implant than in equivalent energy B^+ implant. This has been attributed to the presence of fluorine in BF_2^+ implants. However, it is still unclear whether this behavior originates from the physical damage or from the chemical effect of fluorine. Understanding the mechanism is important to further investigation of shallow junction formation [14].

The inherent damage produced by ion implantation results in a large super saturation of silicon self-interstitials during post-implantation annealing. This interstitial super saturation leads to an increase in the diffusivity of dopant such as boron, phosphorus, and arsenic during the initial stages of annealing, a phenomenon commonly known as transient enhanced diffusion (TED). In sub-keV boron implants, since the final junction depth is dominated by boron diffusion that occurs during the activation anneal. The formation of ultra shallow, low receptivity junctions in the source and drain extension regions of transistors is hindered by TED [15].

In previous studies, fluorine has been co-implanted with boron, mainly in the form of a BF_2^+ molecular implant, to determine its effect on the characteristics of implanted boron. Many important observations have been brought forth by these previous investigations. One of the most noteworthy conclusions of these studies was that a BF_2^+ molecular implant produced a shallower junction than a B^+ implant with equivalent energy for the boron ion. These results were promising, however some ambiguity remained. This is due to the fact that crossing the amorphization threshold in silicon leads to significant changes in the point defect population and impurity diffusion characteristics during post-implantation annealing. Since BF_2^+ implantation typically leads to amorphization and B^+ implantation generally does not, in many cases it was difficult to separate certain intervening variables from the chemical species effect of fluorine. **A** recent study by Downey et al has conclusively shown that the reduction in boron TED is a chemical species effect. The exact nature of this effect remains unknown [15]

Scaling of MOS devices requires a decrease in lateral dimensions as well as a decrease in junction depths. Current projections call for junction depths in the 300A range in order to reduce the short-channel effects of 0.07micro.meter gate-length technologies. The key limiting factors in boron doped junctions are the Transient Enhanced Diffusion (TED) and the more recent concept of Boron Enhanced Diffusion (BED). Typically, in the creation of shallow junctions, a high temperature spike anneal is used [16].

The annealing process has the side effect of Transient Enhanced Diffusion.{311} crystalline defects provide interstitials which cause enhanced dopant diffusion. The result is **a** short period of highly increased diffusivity that can be several thousand times higher than standard boron diffusion with no crystal damage present. Other studies have shown that TED is not the only limiting factor in the creation of ultra-shallow junctions. High concentration of boron in the absence of damage also enhances boron diffusivity termed as Boron Enhanced Diffusion, and is present during spike anneals of 1050°C [16].

As higher gate densities and higher frequencies are required for silicon integrated circuits, smaller device dimensions, both laterally and in depth, are required. Manufacturing of shallow P^+N junctions, using boron implantation, presents many difficulties. This is due to the large range of projection for B^+, the high diffusivity and the transient enhanced diffusion (TED) of boron implanted in silicon. The implantation of BF_2^+ molecular ions into silicon has been reported to have the advantages of higher electrical activation and lower leakage current for P/N junctions compared with B^+ implantation. In addition, the energy partition for the boron ions in the BF_2^+ implantation is only 22%. Consequently, BF_2^+ produces a shallower as-implanted profile, which is attributed to a reduction in channeling using BF_2^+. Much more significant reductions in the depth of annealed profiles are also observed. Hence, BF_2^+provides less TED than B^+. The F implanted ions along with boron are well known to affect the redistribution of boron during the thermal annealing process. Krasnobaev et al. have suggested three effects of fluorine on the boron redistribution [16]

One effect is due to free point defects, a second one due to complex defects that becomes electrically active and the last one supposes the formation of B–F complexes. Park

et al. have studied the reaction of interstitial silicon with F. In the present work, we suggest that the presence of F could act as sinks for interstitial boron which has been taken into account in our model. We have simulated boron (BF_2^+) diffusion implanted in crystalline and germanium morphine silicon by using a wide range of germanium preamorphization energies. Hence, the behaviors of fluorine and the influence on boron diffusion have been explained for different amorphization conditions and compared with nonamorphized cases [17].

The transient enhanced diffusion (TED) of ion-implanted boron in silicon is a major problem in the fabrication of ultra shallow junctions (USJs) for advanced integrated circuits (ICs). It is now well established that boron diffuses by a kick-out mechanism in silicon. During the post implantation annealing, the transient enhanced diffusion will occur and it may increase the junction depth. In addition, high-concentration B^+ will lead to B^+ clustering and B^+ precipitation, which reduce electrical activation. Furthermore, the diffusion behaviors of boron implanted into silicon with ultra low- energy represents another type of anomalous diffusion phenomenon now known as the boride enhanced diffusion (BED). BED is attributed to a silicon boride phase that injects silicon interstitials during annealing. Several advantages can be gained using BF_2^+ ion implantation instead of boron implantation. The main advantage is the effective boron implant energy, which is reduced to nearly a quarter of the acceleration potential. These characteristics have made BF_2^+ implants attractive for shallow PN junction formation. Several effects of fluorine on the boron redistribution have been suggested. One effect is due to free point defects, a second one due to complex defects that becomes electrically active and the last one supposes the formation of B–F complexes [18].