DESIGN AND SIMULATION OF CMOS OPERATIONAL AMPLIFIER USING MENTOR GRAPHICS TOOL

by

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APPROVAL AND DECLARATION SHEET

This project report titled Design and Simulation of CMOS Operational Amplifier using Mentor Graphics Tool was prepared and submitted by Jegatheesan Sri Ramalu (Matrix Number: 031030140) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in University Malaysia Perlis (UniMAP).

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REKABENTUK DAN SIMULASI PENGUAT OPERASI CMOS DENGAN PERISIAN MENTOR GRAPHICS

ABSTRAK

Perkembangan semasa dalam industri semikonduktor menunjukkan kewujudan dan keperluan bagi komponen-komponen electronik untuk beroperasi dalam voltan rendah terutamanya bagi komponen yang banyak digunakan seperti penguat operasi. Keperluan komponen untuk beroperasi dalam voltan rendah, menyebabkan penurunan dalam bekalan voltan yang dibekalkan kepada komponen tersebut serta saiz komponen yang semakin mengecil. Alternatif yang paling berkesan dalam memenuhi keperluan ini adalah dengan beralih kepada CMOS (Complementary Metal Oxide Semikonduktor) yang menawarkan komponen dengan keperluan kuasa yang rendah dan kecil dari segi saiz. Dalam projek ini, rekabentuk dan simulasi penguat operasi CMOS yang mempunyai ciri-ciri kuasa yang rendah dan gandaan yang sederhana serta terdiri daripada dua peringkat telah diimplikasikan. Rekabentuk ini dipraktiskan dalam persian Mentor Graphics dengan teknologi 0.35μ TSMC untuk simulasi dan analisis. Seterusnya, bentangan bagi penguat operasi yang direkabentuk dilukis dalam stesen litar terkamir untuk simulasi semakan peraturan rekabentuk serta untuk membandingkan lakaran skematik dengan bentangan. Penguat operasi CMOS yang direkabentuk, pada asasnya memenuhi sebahagian daripada spesifikasi-spesifikasi yang ditetapkan walaupun beberapa spesifikasi tidak dapat dipenuhi. Antaranya ialah nilai rangkuman voltan output iaitu +/- 1.81V serta nilai CMR (common mode range) iaitu + 1.08V dan -1.81V. Perbezaan antara nilai yang dikira dengan simulasi adalah disebabkan oleh kesan “short channel”. Akhir sekali penguat operasi yang direkabentuk beroperasi dengan sempurna dalam voltan operasi 2.5V.

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ABSTRACT

Today's atmosphere and demands continue to drive operating voltages down, especially for widely used components such as the Operational Amplifier. Some of the motivations driving the market are integration, battery operated components, and biomedical instrumentation. The increased packaging densities require reduction in feature size that, in turn, reduces breakdown voltages thereby limiting the power supply. In order to ascertain low voltage and smaller in size operational amplifier, CMOS operational amplifier is preferred. In this project, the design and simulation of low power, moderate gain, and fast settling time CMOS operational amplifier consisting of three stages is implemented. The design was implemented in Mentor Graphics employing 0.35μ TSMC process technology for simulation and analysis. Finally the layout of the amplifier designed in mentor graphics IC station to perform DRC and LVS simulation. The design resulted in a complete CMOS operational amplifier that at least met and, in a few cases, exceeded the design objectives by a large margin. The notable performance areas were the output swing of +/- 1.81V, and the common mode input range of + 1.08V and -1.81V. The deviation with the calculated values is because of short channel effects. The CMOS operational amplifier is working properly within the operating voltage 2.5V.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS, ABBREVIATIONS OR NOMENCLATURE

K	transconductance parameter (in saturation).
γ	bulk threshold parameter.
V_T	Threshold voltage.
λ	channel length modulation parameter.
gm	tranconductance.
fu	unity gain frequency.
V_{DSAT}	saturation voltage.
V_{GS}	gate to source voltage.
GBW	gain bandwidth.
W	width.
L	length.
DRC	design rule check.
LVS	layout versus schematic.