CHAPTER 1

INTRODUCTION

1.1   Introduction

The goal of this project is to give an opportunity to practice designing and implementing a sequential machine in this case, a traffic light controller. In this project, Quartus 11 Software was chosen to design a gate logic circuit using Schematic Edit and write a coding using Verilog HDL (Hardware Description Language) for traffic light controller. The purpose of this project is to design a safe and efficient traffic flow and to assign the right way and minimize the delay or waiting times in road. This project it was needed to design a logic gate of traffic control signals and implement in hardware to ensure whether this circuits is functioning or not and the simulation timing diagram is using Verilog HDL . This project will can detect the pre source of car and the green light time depend the waiting cars in road. From that, decrease a waiting time in road can reduce traffic jam in road. The expected results of this project are three lanes can green and the other lanes are red at the same time. The result of this project can implement with led.

1.2   Background of Project

Actually, a systems traffic light at Jalan Alor Setar – Kangar (Bukit Lagi, Kangar) is a constant counting timer for green light at main road and side road. From observation, the main road is from 'The Store' to Alor Setar or to Kuala Perlis. The non

busy is from the side road, roundabout at Jalan Bukit Lagi and from Jalan Hospital, Kangar. Now, this traffic system cannot detect number of vehicles at a busy road. The counting times are set and the flow direction was specified. The maximum time is 28s for green light and the short timer for green light is 16s. In addition, Friday noon the road is busy because all of male Muslim will perform their Friday Prayer. This junction also has a river below it, so the stopping in at middle of junction cannot be design because it can crash the bridge.

According to this project, the quality movement of traffic signals can be improving to reduce a traffic jam in road. So, the new controller for traffic signals is designed to minimize a traffic jam in road. From this project, green times for busy road will be longer and it continues change the color when the maximum times are stop. In this project, consider the long time is 40s and the short timer is 20s for the green light.

1.3   Objective of Project

The main objective for this project is to design a program of intelligent traffic light system to the real life. This project also to design a safe and efficient traffic flow, to assign the right way and minimizes the delay or waiting time at road. The traffic jam will be reducing by increase the green time on busy road and decrease the green time in non busy road. Other objective/aims are lists above:

    I. To design and implement the finite state machine of an intelligent traffic light controller on hardware.

   II. To give an opportunity to practice designing and implementing a finite state machine in this case, a traffic light controller

  III. Design and implement enhancement to this system that currently in use

  IV. Learn practical issues related to timing and testing of finite state machine

   V. To demonstrate the ability to evaluate critically

      a. To understand the problem and issues

      b. Appreciation of different approaches and techniques