

HARDWARE IMPLEMENTATION OF INTELLIGENT
TRAFFIC LIGHT CONTROLLER

NOORRASHIKIN BINTI JAAFAR

SCHOOL OF MICROELECTRONIC ENGINEERING
UNIVERSITI MALAYSIA PERLIS

2007

HARDWARE IMPLEMENTATION OF INTELLIGENT TRAFFIC
LIGHT CONTROLLER

by

NOORRASHIKIN BINTI JAAFAR

Report submitted in partial fulfillment
of the requirements for the degree
of Bachelor of Engineering



UⁿⁱMAP

MAY 2007

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to my parents for their support and love which has motivate me through out these hard time. Not forgetting to my adviser, Mr Muammar Mohamad Isa from School of Microelectronics Engineering. They have been a great mentor with their management skills and enthusiasm. They also have been an exceptional role model of life. They have done their best to help relieve concerns that their advisees have. It has been memorable that they encouraged and supported me while I was in deep depression and while I faced problems in completing this project.

Inclined to forget, my special thanks goes to my coordinator project of Electronic Engineering, Mr. Rizalafande Bin Che Ismail who had helped me a lot. Comprehend of his demanding jobs, but he still consumes his times to devote concerned and attention for me.

I also would like thanking to Mr. Ir Shaharuddin Bin Othman, manager of JKR Electric Department and to my entire friend for the knowledge and caring during to finish this project. Not forgetting also to my housemate for their support and commitment.

Lastly I'm also would like to make an apology if during to finish my final project, I have hurts someone's feelings. I am really sorry for any mistakes. Last but not least, I hope UniMAP will become one of the most illustrious universities in the world. Wish all the best to all of you.

APPROVAL AND DECLARATION SHEET

This project report titled Hardware Implementation of Intelligent Traffic Light Controller was prepared and submitted by Noorrashikin Bt Jaafar (Matrix Number: 031030353) and has been found satisfactory in terms of scope, quality and presentation as partial fulfillment of the requirement for the Bachelor of Engineering (Electronic Engineering) in Universiti Malaysia Perlis (UniMAP).

Checked and Approved by

(MR. MUAMMAR MOHAMAD ISA)

Project Supervisor

School of Microelectronic Engineering

Universiti Malaysia Perlis

MAY 2007

MENGAPLIKASIKAN PERKAKASAN PENGAWAL LAMPU ISYARAT PINTAR

ABSTRAK

Lampu isyarat pintar pengawal memainkan peranan yang sangat penting dalam pengurusan dan mengawal isyarat dalam bandar bagi mengurangkan kesesakan dan kemalangan di jalan raya. Ia adalah contoh terbaik untuk mengatasi masalah di jalan raya pada masa kini. Kawalan lampu isyarat pintar adalah mesin jujukan yang boleh digunakan untuk menganalisis dan mengaturlara melalui pelbagai proses. Peranti-peranti yang terdapat dalam analisis ini adalah merangkumi mesin berjujukan untuk mengawal turutan lampu isyarat, masa yang segerak dan pengenalan kepada operasi sintesis kerlipan lampu isyarat jujukan. Kaedah yang digunakan dalam projek ini adalah melukis litar, menulis kod aturcara, menganalisis, sintesis dan mengaplikasikan menggunakan perkakasan. Dalam projek ini, perisian QuartussII telah dipilih untuk merekabentuk skematik menggunakan fail skematik, tulis satu pengekodan menggunakan Verilog HDL (Bahasa penggambaran perkakasan) teks dan mengaplikasikan litar menggunakan get logik.

HARDWARE IMPLEMENTATION OF INTELLIGENT TRAFFIC LIGHT CONTROLLER

ABSTRACT

Traffic signal controller is playing more and more important roles in modern management and controls of urban traffic to reduce the accident and traffic jam in road. The traffic light controller is a sequential machine to be analyzed and programmed through a multi step process. The device that involves a analysis of existing sequential machines in traffic lights controllers, timing and syhronization and introduction of operation and flashing light synthesis sequence. The methods that are used in this project are design the circuit, write a coding, simulation, synthesis and implement in hardware. In this project, QuartussII Software was chosen to design a schematic using schematic edit, writes a coding using Verilog HDL (Hardware Description Language) text editor and implements the circuit using gate logic.

TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENT	i
APPROVAL AND DECLARATION SHEET	ii
ABSTRAK	iii
ABSTRACT	iv
TABLE OF CONTENTS	v
LIST OF TABLES	viii
LIST OF FIGURES	ix
LIST OF SYMBOLS, ABBREVIATIONS OR NOMENCLATURE	xi
CHAPTER 1 INTRODUCTION	
1.1 Overview	1
1.2 Background of Project	1
1.3 Objective of Project	2
CHAPTER 2 LITERATURE REVIEW	
2.1 Introduction	3
2.2 Traffic Light Systems	3
2.3 Benefit of Traffic Light Controller	4
2.4 Types of Traffic Signals and Operation	5
2.5 State Machine Design	6
2.6 Explanation about Software and Hardware	6
2.6.1 Quartuss II Software	6
2.6.2 Benefit of Using Verilog HDL (Hardware Description Language)	8

CHAPTER 3 METHODOLOGY

3.1	Introduction	9
3.2	Developing a Block Diagram and Interface Signal of Traffic Light Systems	10
3.3	Possible Direction of Intelligent Traffic Light Controller	11
3.4	State Diagram of Traffic Light Controller	15
3.5	The Combinational Logic	17
	3.5.1 Implementing the Decoder Logic	18
	3.5.2 Implementing the Light Output Logic	20
	3.5.3 Implementing the Trigger Logic	21
3.6	Timing Circuits Requirement	25
3.7	Sequential Logic	27

CHAPTER 4 RESULTS AND DISCUSSION

4.1	Introduction	32
4.2	Result of Combinational Logic	32
	4.2.1 Result for State Decoder	32
	4.2.2 Result for Output Logic	34
	4.2.3 Result for Trigger Logic	36
	4.2.4 Result of Complete Combinational Logic	37
4.3	Result of Sequential Logic	39
	4.3.1 Result for D-flipflop module	39
	4.3.2 Result for Input Logic module	40
	4.3.3 Result of Complete Sequential Logic	41
	4.3.4 The combination of combinational logic and sequence logic	42
4.4	Complete Combination of Traffic Light Controller	44
4.4	Discussion	45

CHAPTER 5 CONCLUSION

5.1	Summary	47
5.2	Recommendation For Future Project	48

5.3	Commercialization Potential	48
-----	-----------------------------	----

REFERENCES		51
-------------------	--	-----------

APPENDICES

Appendix A	Inverter/Not (74LS04) data sheet	53
Appendix B	3-to-8 Line Decoder (74LS138) data sheet	55
Appendix C	2-input OR (74LS32) data sheet	59
Appendix D	555 Timer data sheet	64
Appendix E	2-input AND (74LS08/74LS09) data sheet	74
Appendix F	3-input AND (74F11) data sheet	76
Appendix G	Exclusive – OR (74LS86) data sheet	78
Appendix H	Dual flip-flop (74LS74) data sheet	81
Appendix I	The complete program	82

LIST OF TABLE

Tables No.		Page
3.0	Interface Signal Description For Traffic Light Controller	10
3.1	Truth table for the state decoder logic	19
3.2	Truth table for the output logic	23
3.3	Truth table for the trigger logic	23
3.4	Next-state table for the sequential logic functions	29

LIST OF FIGURE

Figures No.		Page
2.0	QuartusII Design Flow [2]	7
3.0	Flow Chart of traffic light controller program	9
3.1	Traffic light control system block diagram	11
3.2	Diagram showing an interchange junction traffic light	12
3.3	Diagram showing possible pass situation whereby lanes A1,A2,D1 is green	13
3.4	Diagram showing possible pass situation whereby lanes B1, A1, B2 is green	13
3.5	Diagram showing possible pass situation whereby lanes B1, C1, C2 is green	14
3.6	Diagram showing possible pass situation whereby lanes C1, D1, D2 is green	14
3.7	State diagram showing the 3-bit code sequence	17
3.8	Block diagram of the combinational logic	18
3.9	Gate logic diagram for state decoder	20
3.10	The gate logic diagram for Output Logic	22
3.11	The gate logic for timing trigger	24
3.12	The complete combinational logic gate	24
3.13	Combinational logic gate circuit	25
3.14	Block diagram of the timing circuits	25
3.15	Timing circuit	26

3.16	Block diagram of the sequential logic	27
3.17	Sequence logic diagram	29
3.18	Sequential logic gate circuit	30
3.19	The complete combination	30
3.20	The sequential logic gate	31
4.0	Diagram showing simulation result of module state_decoder	33
4.1	Diagram showing simulation result of module output_logic	35
4.2	Diagram showing simulation result of module trigger_logic	36
4.3	Diagram showing simulation result of module combinational_logic	38
4.4	Diagram showing simulation result of module D-flipflop	40
4.5	Diagram showing simulation result of module input_logic	41
4.6	Diagram showing simulation result of module sequential_logic	42
4.7	Combination of combinational logic and sequence logic	43
4.8	Signal light function for state 6	44
4.9	Signal light function for state 8	45

LIST OF SYMBOLS, ABBREVIATIONS OR NOMENCLATURE

T_w	Time width
R	Resistance
C	Capacitance
HDL	Hardware Description Language
FPGA	Field Programmable Gate Array
SOPC	system-on-a-programmable-chip
AHDL	Altera Hardware Description Language
VHDL	(VHSIC – Very High Speed Integrated Circuit Hardware Description Language)
IC	Integrated Circuit