Postgraduate Studies

Face Emotion Recognition using Artificial Intelligence Techniques

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There has been tremendous growth in the area of Human Computer Interaction (HCI)with numerous applications documented, and Face Emotion Recognition (FER) is well known. Seven face emotions are considered universally in FER research: happy, sad, angry, fear, surprise, disgust and neutral. FER can find applications in hospitals, and for senior citizens, bed ridden persons and severely injured patients as well as in analyzing personal emotion psychology. FER comes with various approaches and methods to extract a good recognition package. However, there are various reasons for failures in the packages such as aging, color, mental state and individual face expressions.

In this research, focus is in personalized face emotion and some studies are extended for better emotion recognition. FER is achieved in two parts, namely image processing and classification. The first part investigates a set of image processing methods suitable for recognizing the facial emotion where acquired images undergo a few preprocesses. Application of edge detection has to be successful even with uneven light intensities for which a histogram equalized image is split into two regions of interest (ROI) – eye and lip. Both regions are subjected to the same preprocessing methods but with different threshold values. The human eye and lip are elliptical, and with the objective of finding the changes in eye and lip areas, a set of new forms for ellipse fitness function is proposed. This fitness functions find changes in the minor axes of both eye and lip images. These are then utilized by genetic algorithm (GA) to find the optimized values of the minor axes.

Three fitness functions are developed, for the eye, upper lip and lower lip, respectively. Observation of various emotions of three subjects leads to unique characteristics of eye and lip. It is found, from the optimized data, that there is no common pattern to recognize emotions among the three subjects. The absence of common patterns leads to studies ethnocentric emotions. In understanding ethnocentric facial emotion recognition, the developed fitness functions are applied on two local subjects. However, emotion ranges overlapped and to circumvent this, two Artificial Intelligence (AI) classification techniques, neural network and fuzzy clustering, are employed. It is concluded that the analysis of personalized emotion through facial features of two subjects indicate a higher rate of success compared to a generalized analysis as applied to various ethnic personalities.

A Novel Large-Bit Single Architecture and Microarchitecture for the Implementation of Superscalar Pipeline VLIW Microprocessors

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Microprocessors have grown tremendously in computing and data crunching capabilities. Most microprocessors in the market currently are at 32 bits, while the latest microprocessors from IBM, Intel and AMD are at 64 bits. There are two possible paths to further enhance the computational capabilities of a microprocessor, which is to either increase the bit size of the microprocessor to 128/256/512 bits or implement multiple microprocessor cores in a single die. Larger bit sizes allow more simultaneous data crunching. Multiple cores, especially, quad cores are configured as pseudo-quad core or full quad core within a single microprocessor unit. A pseudo-quad core has two silicon dies, each with a dual core microprocessor. A full quad core consists of four microprocessor core on one die.

Both methods have advantages and disadvantages, with different design issues and engineering limitations. This work explores methods of increasing the data bus size from 32/64 bits to 128/256/512 bits to allow for more data crunching capability. A superscalar pipeline 64 bits VLIW microprocessor with 4 stages and 3 parallel pipes is implemented on a TSMC 0.35 micron process. The implementation is then expanded to 128/256/512 bits using the same TSMC 0.35 micron process. In order to prove the concept that such a large bit size VLIW microprocessor can indeed be implemented, the VLIW microprocessor is programmed on an Altera Stratix 2 FPGA and back annotated for verification.

The critical paths of the 128/256/512bit VLIW microprocessor is analyzed with its worst path within the ALU adder in the execute stage. Different adder architectures are investigated for suitability on synthesis implementation of large data bus size adder for efficient usage within the ALU. An adder algorithm using repetitive constructs in a parallel algorithm that allows for efficient and optimal synthesis for large data bus size is proposed as a suitable implementation for the adder within the ALU. The proposed adder architecture synthesis of a large bit size adder provides for an improved performance- gate count-product compared to conventional adder architecture synthesis. A large bit size VLIW microprocessor is possible by implementing a 64/128/256 bits data size on an Altera Stratix 2 FPGA.

Database Encryption for a Web-based Claims System

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The main purpose of this study is to develop a computer system for UniMAP staff to file claims via electronic media, based on the Treasury and other circulars by the Ministry of Finance, Malaysia. Basic important particulars have been built into the system such as salary, grade, entitlement and others. An additional feature included is automatic calculation. It can be equipped with a security tool too, to prevent hackers or unauthorized persons, selected from the results of a security analysis. There are three categories of users involved in the system, being Claimant, Responsibility Centre and Bursary Department. The Responsibility Centre includes all administrative departments and centres of study, where the budget allocation is acquired from. The system development begins with design of the Process Flow Diagrams. All three category of users must follow their flow in the diagrams. Process flow determines the movements of the forms from the moment they are submitted up to the stage where payments are made. This process is followed by Data Flow Diagram design and then the Database.

The former specifies how data flows in the system, whereas the latter is for data storage of data such as login identifications, passwords, staff personal particulars, entitlements etc. The development of the Database comes in four forms namely Entity-Relationship Diagram, Hierarchical Diagram, Relational Database Diagram and Data Dictionary. Of the twenty encryption algorithms available in the Dynamic-Link Library (DLL), five are selected for analytical comparison in terms of its performance and compatibility with the developed system. This Web-based system enables staff to file claims from anywhere and at anytime, which overcomes human errors as well as being efficient, fast and accurate. Hence it saves time, effort, and administrative costs. Active Server Pages (ASP) is chosen to perform the calculations and generate reports. After the system has been developed, a test was conducted using forms that have been simulated manually. The purpose is to enable the researcher to make comparison with the ones made using the developed system in order to detect errors or flaws from the manual simulation in the system. Testing was also done on the encryption algorithms and Web browsers selected by increasing both the text length size and key length size and observed its performances.

Having noted its response times, an analysis was made in order to determine which encryption algorithms' and Web browsers' performances were most suited for the developed system and considered the best, which is lower and able to sustain its response times. The results of this study have shown that this system is able to detect all human errors in the traditional manual claim system, in which claimants have made some mistakes. On the other hand, the analysis of encryption algorithms with Web browsers, the results have shown that Twofish algorithm is best suited to the system that has been developed using ASP Web programming language on Internet Explorer. Hence, it is emphatic that all objectives that had been set at the beginning of this research have been met.

The Effect of Phosphorus Implant in Converting the Enhancement Mode Transistor into Depletion Mode Transistor

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Metal-Oxide-Semiconductor field effect transistors (MOSFET) form the basis of most electronic devices. However, parts of electronic circuitry require use of depletion mode MOSFETs which conduct current at Vg=0V. This transistor is 'normally on' unless a reverse-polarity Vg is applied to switch it off. Hence, investigations on process parameters that affect the performance of depletion mode transistor are studied. Research emphasis is on ion implantation to form the depletion channel.

Design of Experiment (DOE) for ion implantation dose and energy is implemented based on MIMOS' fabrication facility. The 0.5um CMOS process technology was used as a baseline to produce n-type depletion mode MOSFET. Simulations to reduce cost and time of producing experiment wafers are executed too. Comparison between experimental and simulation results are detailed. One of the main issues is on the two-peak point of transconductance curve. According to the experimental results, phosphorus ions with 3.3e12 cm-2 dose and 60 keV energyt should produce good depletion mode MOSFET characteristics with a threshold voltage -0.7 V.

Contact Hole Printing Beyond 190 nm In Photolithography Processing Using Resolution Enhancement Techniques

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The scaling down of complementary metal-oxide-silicon (CMOS) technology using current processing tools and material is a challenging task, especially in photolithography. The objective of this work is to use Resolution Enhancement Techniques (RETs) to print smaller contact holes using binary mask, phase shift mask (PSM) and KrF exposure tools. The baseline experiments evaluated with various parameters is used to identify the smallest printable isolated hole prior to applying RETs. The RETs selected in this work are the Focus Latitude Enhancement Exposure (FLEX) and Thermal Flow (TF) technique. The focal distance is the key parameter evaluated in the FLEX technique. As for the TF technique, the temperature and the pre-shrink dimension are the key parameters. Results from both techniques are compared to baseline condition. The baseline study shows that current tools have the capability to print isolated holes measuring 150 nm with low I-D bias. Conventional illumination with 0.7 NA and 0.6 σ is chosen as the optimum setting. FLEX has the ability to extend the Depth of Focus (DOF) margin in double compared to baseline condition for target CD of 150 nm.

This technique also has a comparable image profile to that of baseline condition. It has been found that the optimum focal distance is 0.75 µm. Thermal flow technique is a chemical shrinking technique that uses a special photoresist. The DOF margin of the post-shrink condition depends on the pre-shrink condition. In addition, extremely high temperatures have an impact on DOF margin as well. Higher temperature or longer bake times will cause smaller shrunk dimensions. The research has found that the final post-shrink dimension with DOF margin similar to that of the pre-shrink condition using a binary mask is 120 nm. The FLEX and TF techniques are seen to be comparable or better than the baseline condition in terms of performance. However, having to apply additional steps and having throughput effects are some of the trade off in these techniques. Further evaluations on through pitch pattern and OPC (Optical Proximity Correction) application for the above techniques should be carried out before they can be applied in the production line.